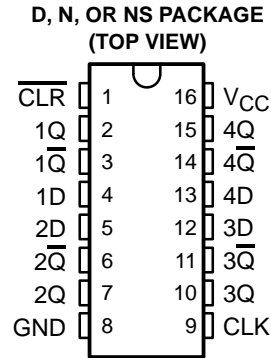


SN74F175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

SDFS058B – D293, MARCH 1987 – REVISED MAY 2002

- Contains Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators



description

This positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear (CLR) input. Information at the data (D) inputs meeting setup-time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F175N	SN74F175N
	SOIC – D	Tube	SN74F175D	F175
		Tape and reel	SN74F175DR	
	SOP – NS	Tape and reel	SN74F175NSR	74F175

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUTS	
CLR	CLK	D	Q	Q̄
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q ₀	Q̄ ₀



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

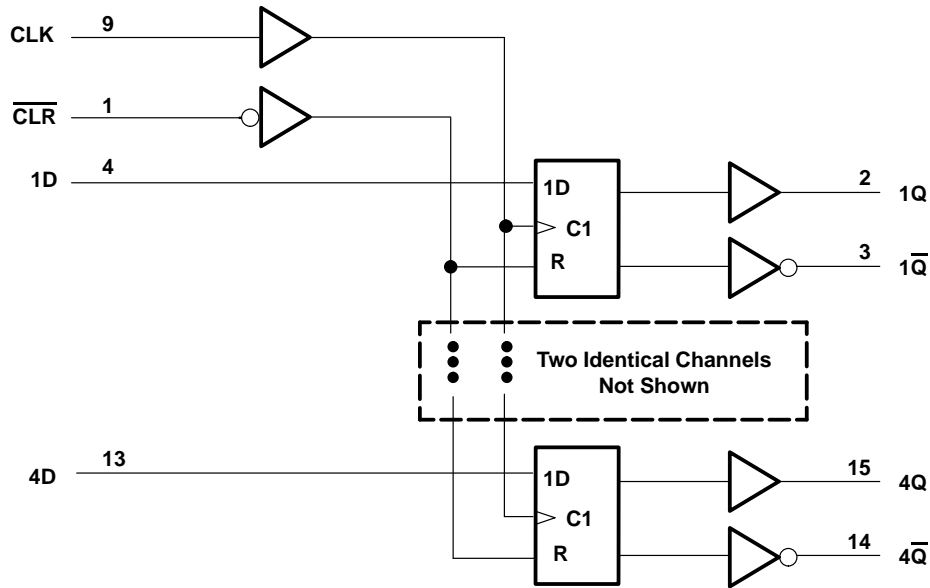
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SN74F175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-1.2 V to 7 V
Input current range	-30 mA to 5 mA
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded if the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN74F175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$,	$I_{OH} = -1\text{ mA}$	2.5	3.4		V
	$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -1\text{ mA}$	2.7			
V_{OL}	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 20\text{ mA}$		0.3	0.5	V
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-0.6	mA
$I_{OS}‡$	$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-60		-150	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$,	See Note 4		22.5	34	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4: I_{CC} is measured with outputs open, with 4.5 V applied to all data inputs after a momentary ground, followed by 4.5 V applied to CLK.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		100			100	MHz
t_w	Pulse duration		CLK high		4	4	ns
			CLK low		5	5	
			CLR low		5	5	
t_{su}	Setup time, data before CLK↑		High or low		3	3	ns
	Setup time, inactive state, data before CLK↑§		CLR high		5	5	
t_h	Hold time, data after CLK↑		High or low		1	1	ns

§ Inactive-state setup time also is referred to as recovery time.

switching characteristics (see Figure 1)

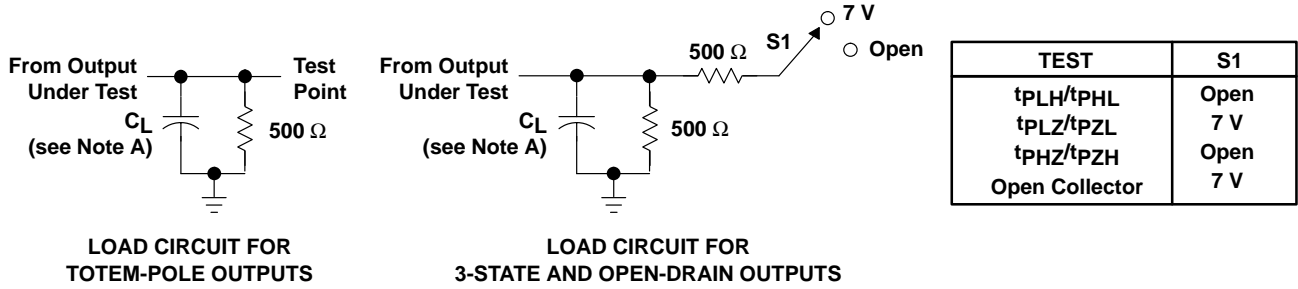
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$			$V_{CC} =$ 4.5 V to 5.5 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	140		100		MHz
t_{PLH}	CLK	Q or \bar{Q}	3.2	4.6	6.5	3.2	7.5	ns
t_{PHL}			3.2	6.1	8.5	3.2	9.5	
t_{PLH}	CLR	\bar{Q}	3.2	6.1	8.5	3.2	9	ns
t_{PHL}		Q	3.7	8.6	11.5	3.7	13	



SN74F175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

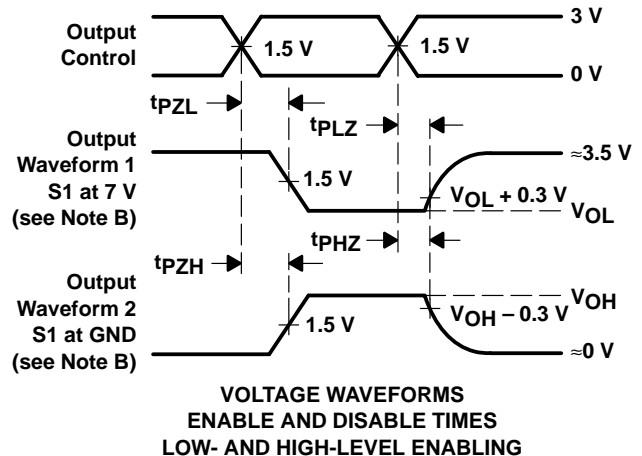
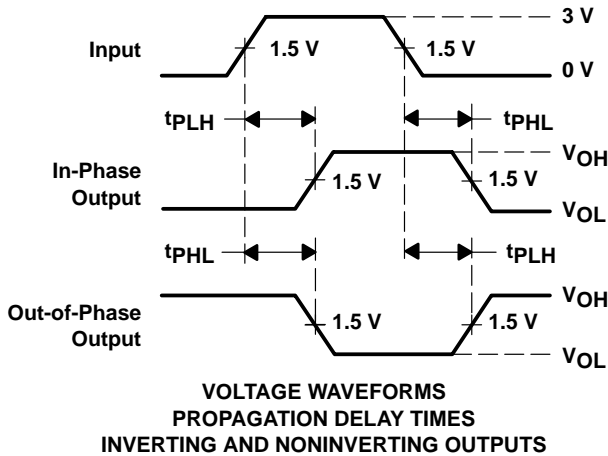
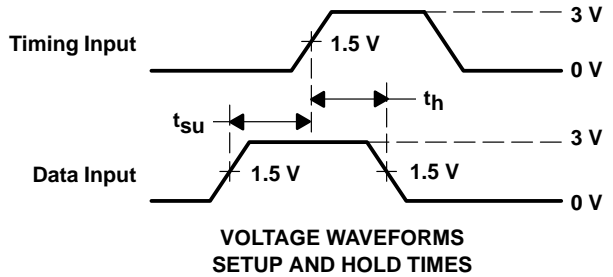
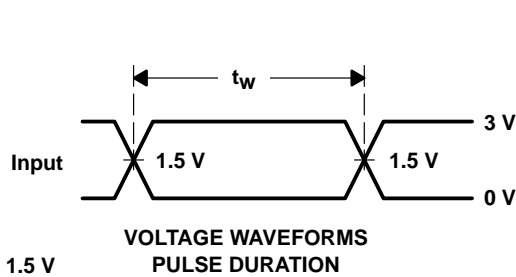
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PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, duty cycle = 50%.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74F175D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F175DR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F175N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74F175N3	OBSOLETE	PDIP	N	16		None	Call TI	Call TI
SN74F175NSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

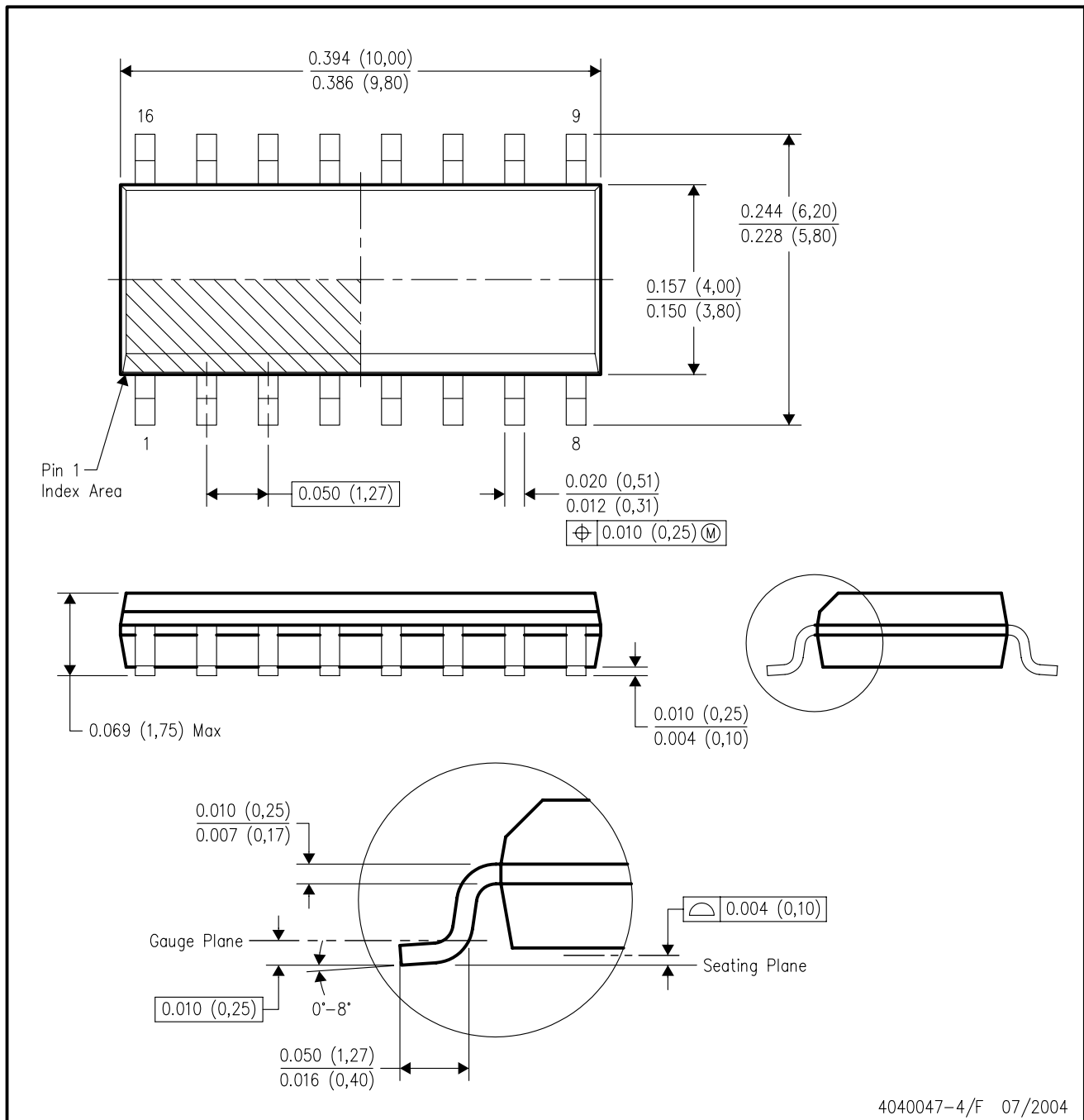


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



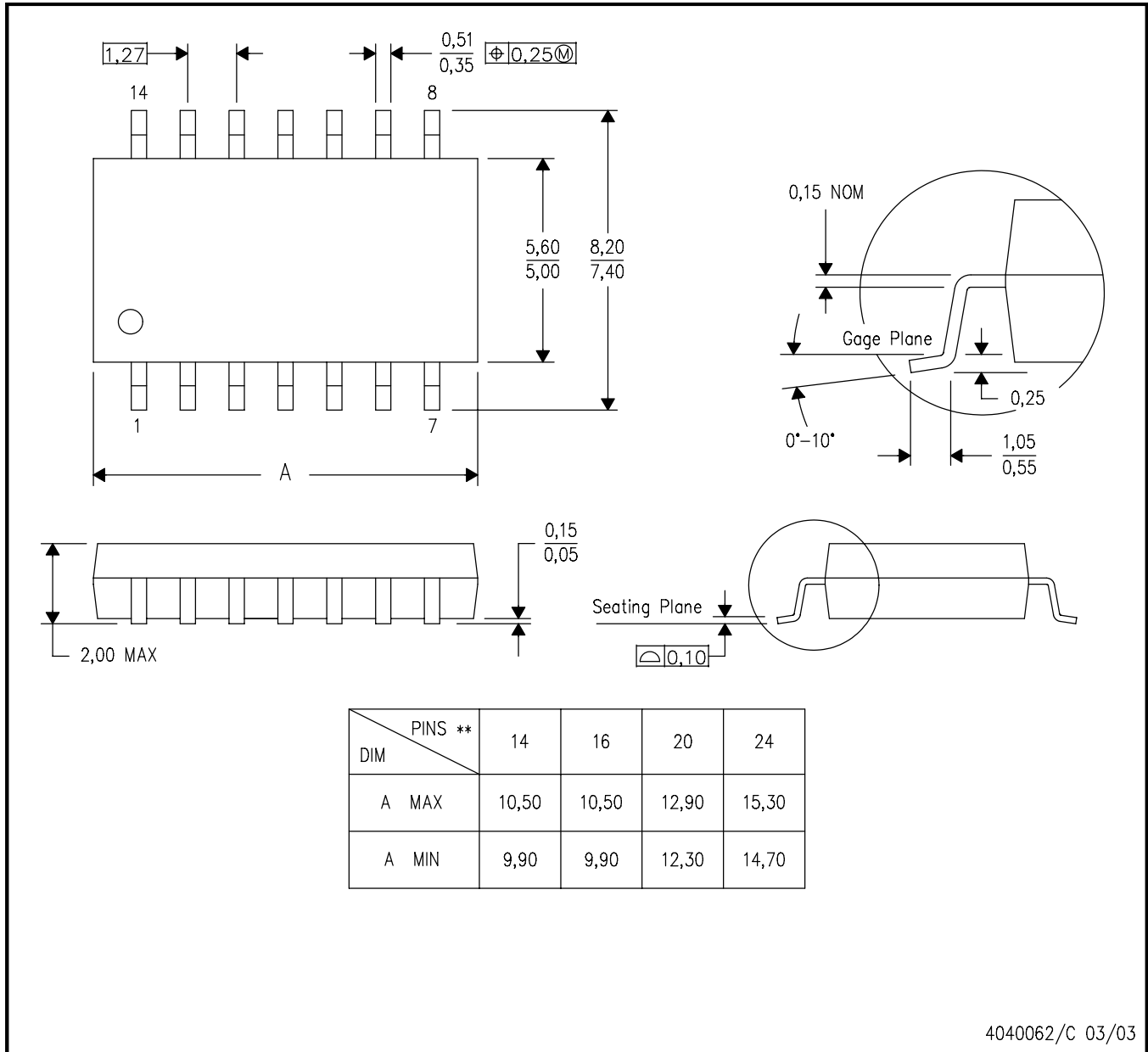
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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