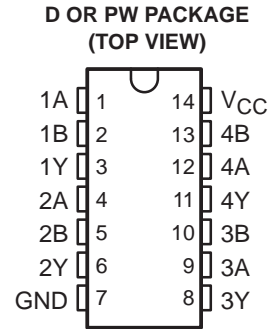


SN74HC08-Q1 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCLS576B – MARCH 2004 – REVISED JUNE 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 40- μ A Max I_{CC}
- Typical $t_{pd} = 8$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max

† Contact factory for details. Q100 qualification data available on request.



description/ordering information

The SN74HC08 device contains four independent 2-input AND gates. They perform the Boolean function $Y = A \cdot B$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

| T_A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| -40°C to 85°C | TSSOP – PW | Tape and reel | SN74HC08IPWRQ1 | HC08I |
| -40°C to 125°C | SOIC – D | Tape and reel | SN74HC08QDRQ1 | HC08Q1 |
| | TSSOP – PW | Tape and reel | SN74HC08QPWRQ1 | HC08Q1 |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN74HC08-Q1

QUADRUPLE 2-INPUT POSITIVE-AND GATE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|---------------------|---------------------------------|------------------|------|----------|------|
| V_{CC} | Supply voltage | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | |
| | | $V_{CC} = 6$ V | 4.2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | I-suffix device | -40 | 85 | °C |
| | | Q-suffix device | -40 | 125 | |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74HC08-Q1 QUADRUPLE 2-INPUT POSITIVE-AND GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN74HC08Q | | SN74HC08I | | UNIT |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 μA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 2 | | 40 | | 20 | μA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN74HC08Q | | SN74HC08I | | UNIT |
|-----------------|--------------|-------------|-----------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | 2 V | | 50 | 100 | | 150 | | 125 | ns |
| | | | 4.5 V | | 10 | 20 | | 30 | | 25 | |
| | | | 6 V | | 8 | 17 | | 25 | | 21 | |
| t _t | | Y | 2 V | | 38 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C _{pd} Power dissipation capacitance per gate | No load | 20 | pF |

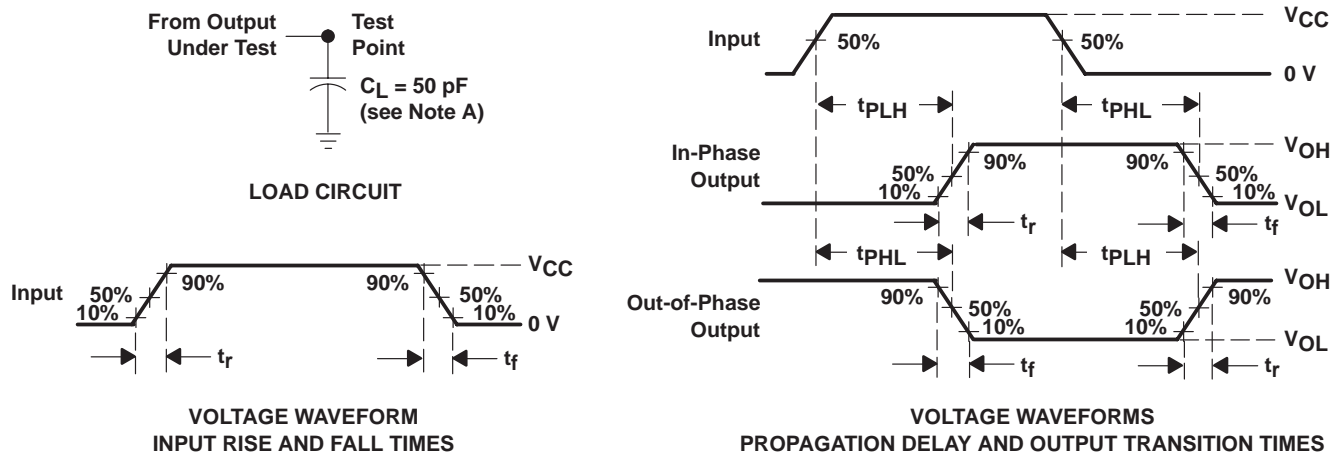


SN74HC08-Q1

QUADRUPLE 2-INPUT POSITIVE-AND GATE

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PARAMETER MEASUREMENT INFORMATION

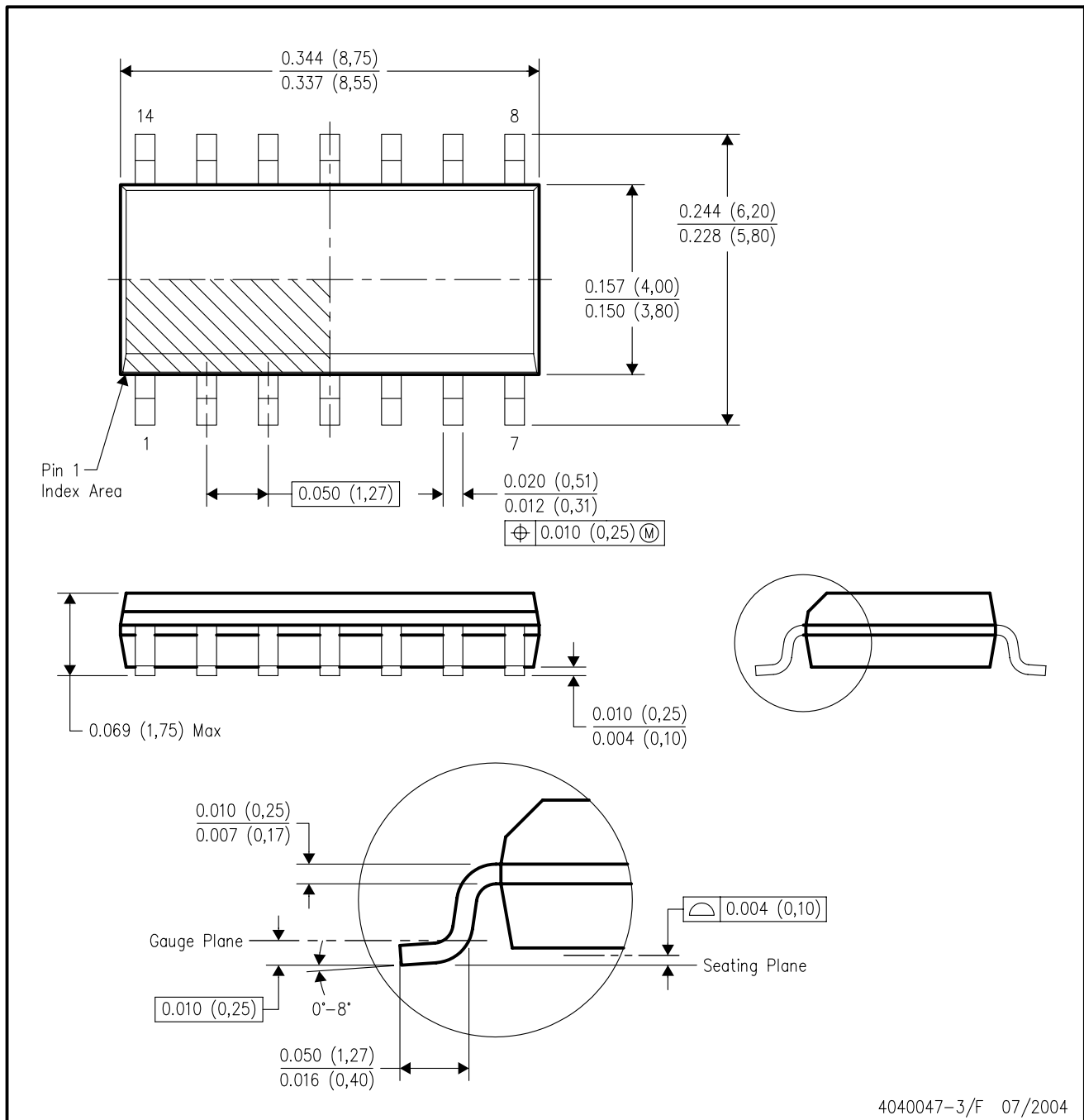


- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time, with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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