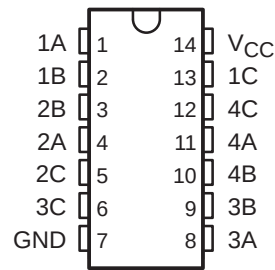


SN74HC4066 QUADRUPLE BILATERAL ANALOG SWITCH

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- High Degree of Linearity
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance —
Typically, $50\ \Omega$ at $V_{CC} = 6\text{ V}$
- Individual Switch Controls
- Extremely Low Input Current
- Package Options Include Plastic Small-Outline (D), Plastic Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (N) 300-mil DIPs

D, DB, PW, OR N PACKAGE
(TOP VIEW)



description

The SN74HC4066 is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

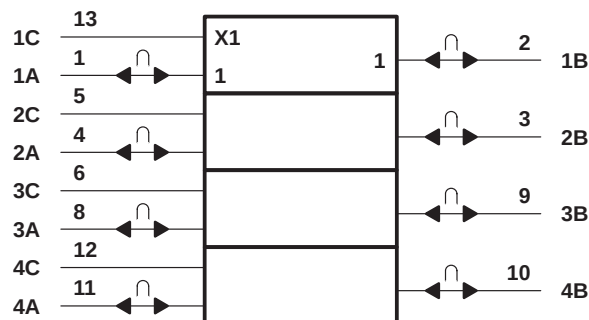
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

The SN74HC4066 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

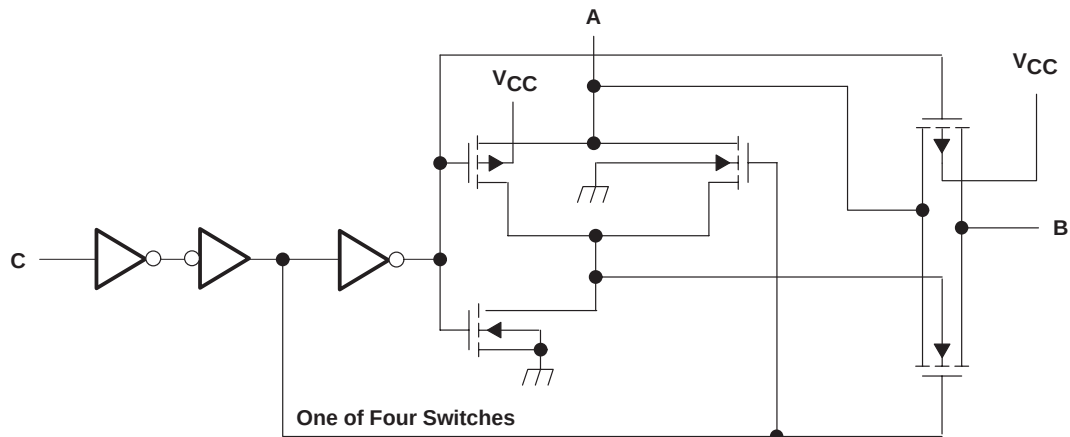
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SN74HC4066
QUADRUPLE BILATERAL ANALOG SWITCH

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logic diagram, each switch (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Control-input diode current, I_I ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
I/O port diode current, I_I ($V_I < 0$ or $V_{I/O} < V_{CC}$)	± 20 mA
On-state switch current ($V_{I/O} = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	127°C/W
DB package	158°C/W
N package	78°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2 [†]	5	6	V
$V_{I/O}$	I/O port voltage		0		V_{CC}	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2\text{ V}$	1.5		V_{CC}	V
		$V_{CC} = 4.5\text{ V}$	3.15		V_{CC}	
		$V_{CC} = 6\text{ V}$	4.2		V_{CC}	
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2\text{ V}$	0		0.3	V
		$V_{CC} = 4.5\text{ V}$	0		0.9	
		$V_{CC} = 6\text{ V}$	0		1.2	
t_t	Input rise/fall time	$V_{CC} = 2\text{ V}$			1000	ns
		$V_{CC} = 4.5\text{ V}$			500	
		$V_{CC} = 6\text{ V}$			400	
T_A	Operating free-air temperature		–40		85	°C

[†] With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
R_{on}	On-state switch resistance	$I_T = -1\text{ mA}$, $V_I = 0\text{ to }V_{CC}$, $V_C = V_{IH}$, (see Figure 1)	2 V		150				Ω
			4.5 V		50	85		106	
			6 V		30				
$R_{on(p)}$	Peak on resistance	$V_I = V_{CC}\text{ or GND}$, $V_C = V_{IH}$, $I_T = -1\text{ mA}$	2 V		320				Ω
			4.5 V		70	170		215	
			6 V		50				
I_I	Control input current	$V_C = 0\text{ or }V_{CC}$	6 V		± 0.1	± 100		± 1000	nA
I_{soff}	Off-state switch leakage current	$V_I = V_{CC}\text{ or }0$, $V_O = V_{CC}\text{ or }0$, $V_C = V_{IL}$, (see Figure 2)	6 V			± 0.1		± 5	μA
I_{son}	On-state switch leakage current	$V_I = V_{CC}\text{ or }0$, $V_C = V_{IH}$, (see Figure 3)	6 V			± 0.1		± 5	μA
I_{CC}	Supply current	$V_I = 0\text{ or }V_{CC}$, $I_O = 0$	6 V			2		20	μA
C_i	Input capacitance	A or B	5 V		9				pF
		C			3	10		10	
C_f	Feedthrough capacitance	A to B			0.5				pF
C_o	Output capacitance	A or B	5 V		9				pF

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switching characteristics over recommended operating free-air temperature range

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t _{PLH} , t _{PHL} Propagation delay time	A or B	B or A	C _L = 50 pF, (see Figure 4)	2 V		10	60		75	ns
				4.5 V		4	12		15	
				6 V		3	10		13	
t _{PZH} , t _{PZL} Switch turn-on time	C	A or B	R _L = 1 kΩ, C _L = 50 pF, (see Figure 5)	2 V		70	180		225	ns
				4.5 V		21	36		45	
				6 V		18	31		38	
t _{PLZ} , t _{PHZ} Switch turn-off time	C	A or B	R _L = 1 kΩ, C _L = 50 pF, (see Figure 5)	2 V		50	200		250	ns
				4.5 V		25	40		50	
				6 V		22	34		43	
f _I Control input frequency	C	A or B	C _L = 15 pF, R _L = 1 kΩ, V _C = V _{CC} or GND, V _O = V _{CC} /2, (see Figure 6)	2 V		15				MHz
				4.5 V		30				
				6 V		30				
Control feedthrough noise	C	A or B	C _L = 50 pF, R _{in} = R _L = 600 Ω, V _C = V _{CC} or GND, f _{in} = 1 MHz, (see Figure 7)	4.5 V		15				mV (rms)
				6 V		20				

operating characteristics, V_{CC} = 4.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	C _L = 50 pF,	f = 1 MHz	45	pF
Minimum through bandwidth, A to B or B to A [†] [20 log (V _O /V _I)] = -3 dB		C _L = 50 pF, V _C = V _{CC} ,	R _L = 600 Ω, (see Figure 8)	30	MHz
Crosstalk between any switches [‡]		C _L = 10 pF, f _{in} = 1 MHz,	R _L = 50 Ω, (see Figure 9)	45	dB
Feedthrough, switch off, A to B or B to A [‡]		C _L = 50 pF, f _{in} = 1 MHz,	R _L = 600 Ω, (see Figure 10)	42	dB
Amplitude distortion rate, A to B or B to A		C _L = 50 pF, f _{in} = 1 kHz,	R _L = 10 kΩ, (see Figure 11)	0.05%	

[†] Adjust the input amplitude for output = 0 dBm at f = 10 kHz. Input signal must be a sine wave.

[‡] Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.



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PARAMETER MEASUREMENT INFORMATION

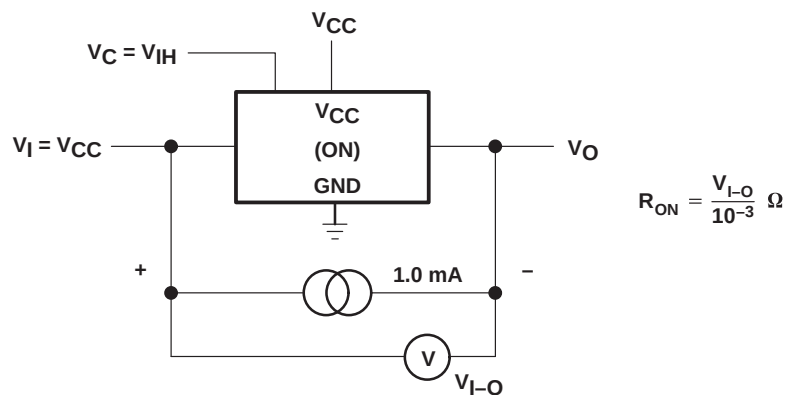


Figure 1. On-State Resistance Test Circuit

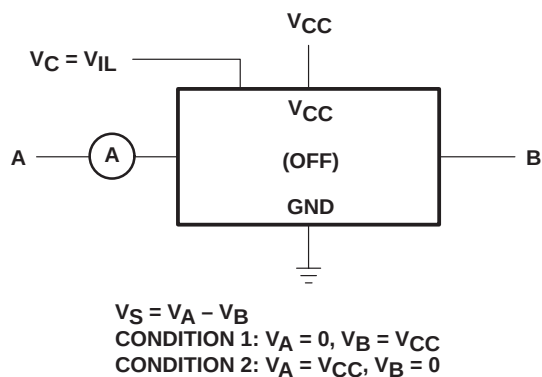


Figure 2. Off-State Switch Leakage Current Test Circuit

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PARAMETER MEASUREMENT INFORMATION

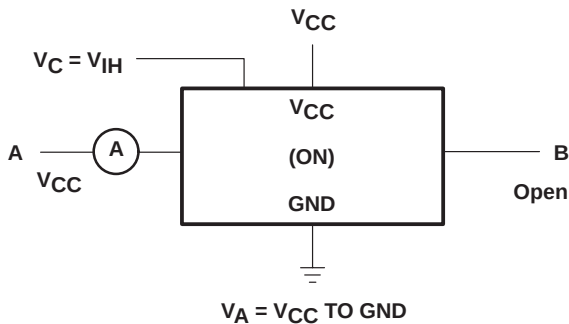


Figure 3. On-State Leakage Current Test Circuit

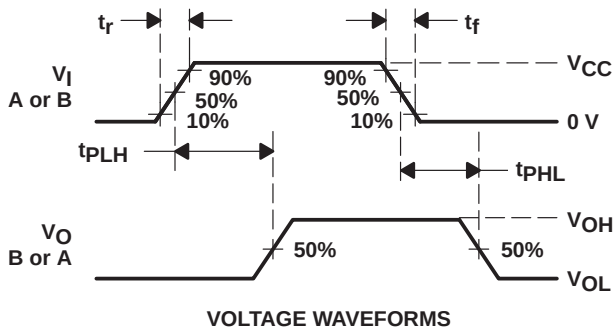
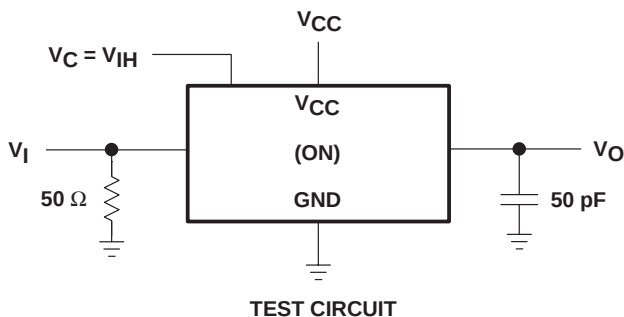
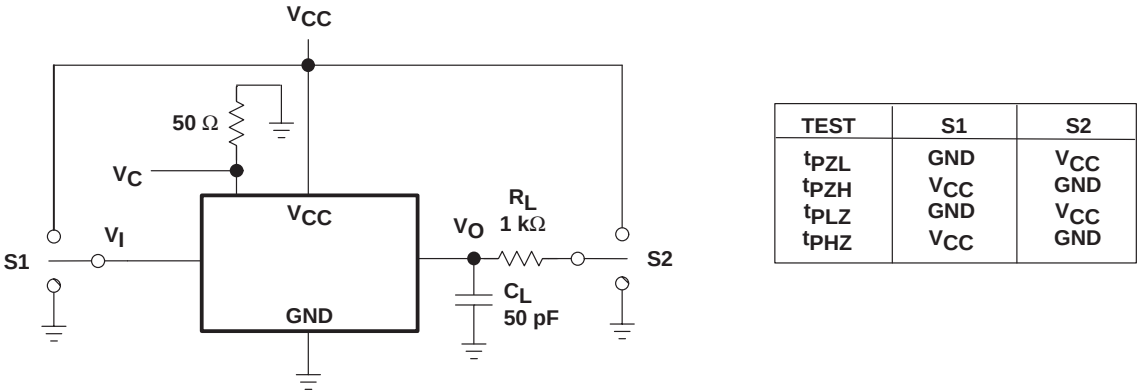
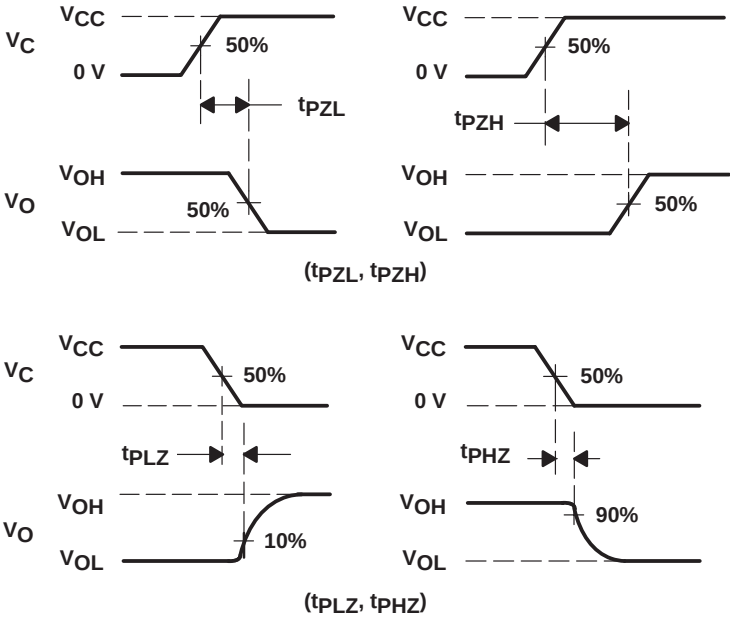


Figure 4. Propagation Delay Time, Signal Input to Signal Output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output

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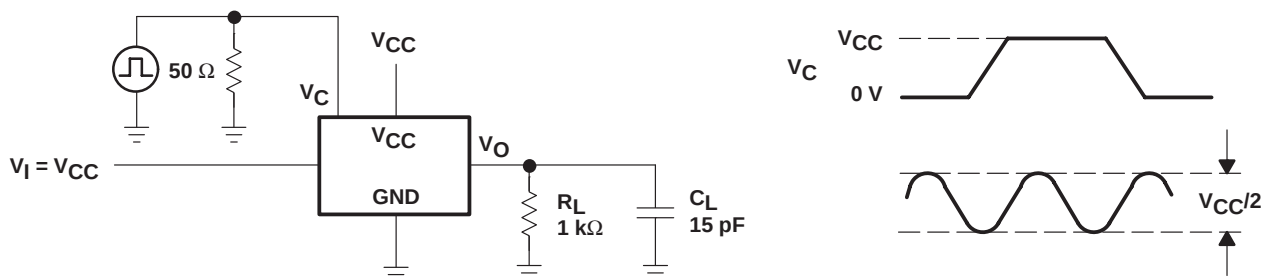


Figure 6. Control Input Frequency

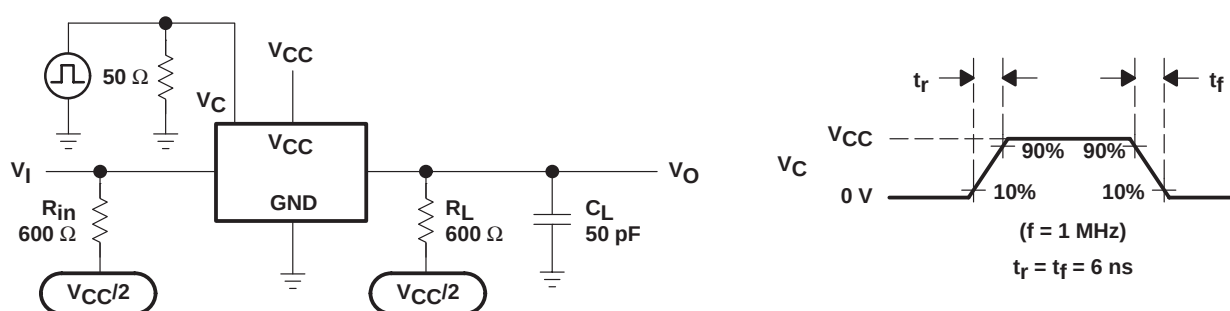


Figure 7. Control Feedthrough Noise

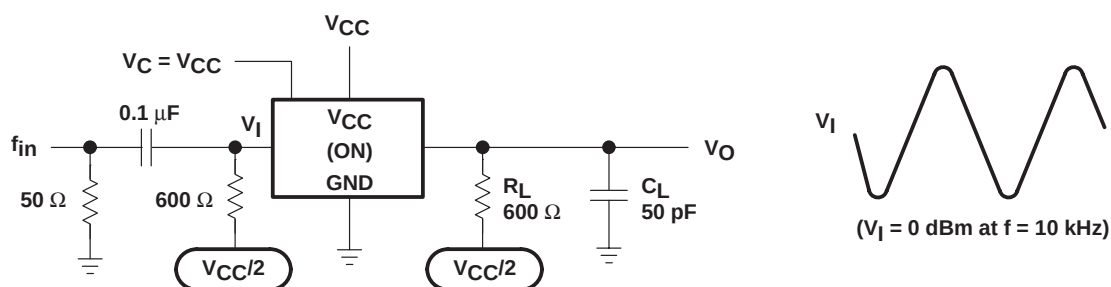


Figure 8. Minimum Through Bandwidth

PARAMETER MEASUREMENT INFORMATION

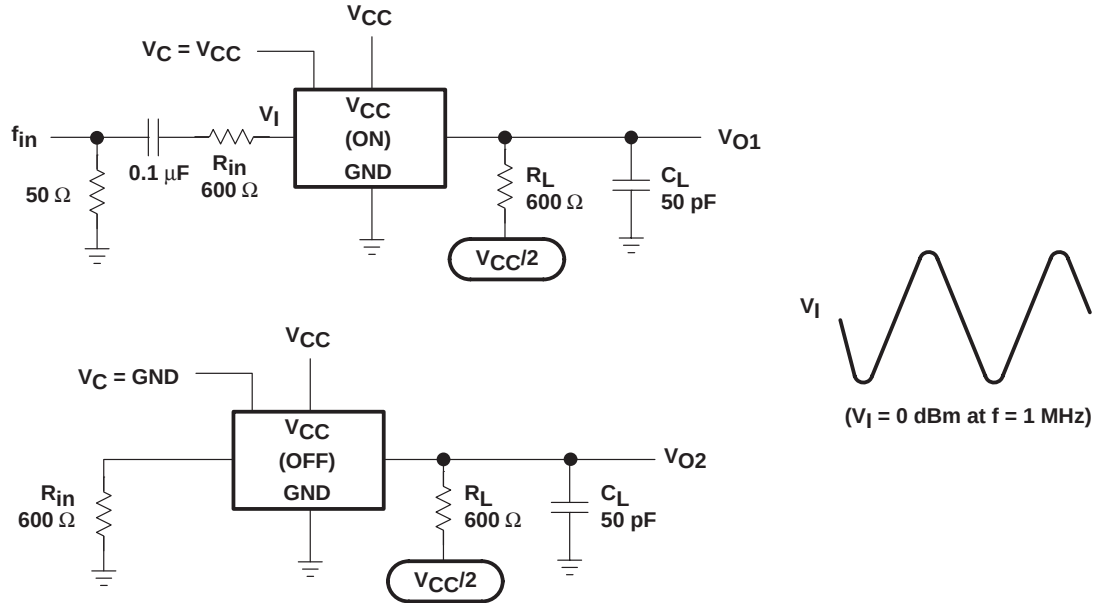


Figure 9. Crosstalk Between Any Two Switches

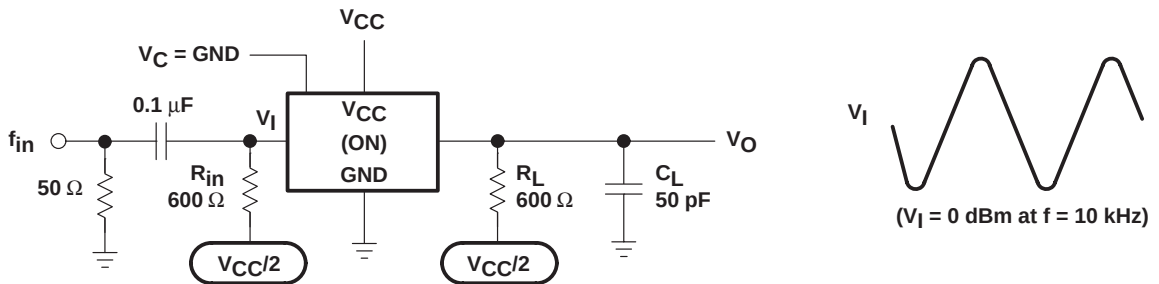


Figure 10. Feedthrough, Switch Off

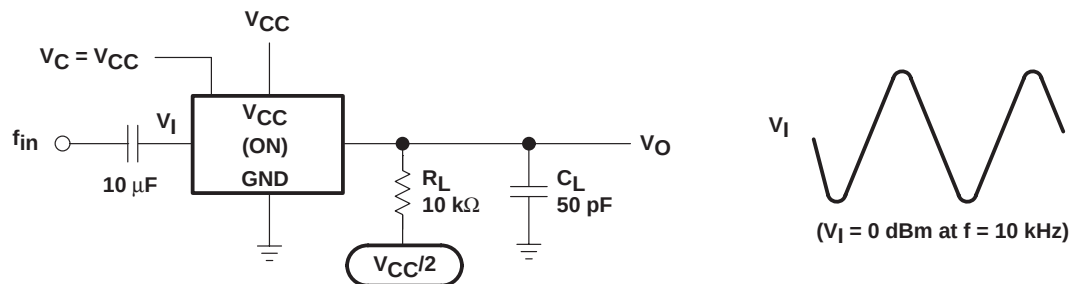


Figure 11. Amplitude Distortion Rate

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