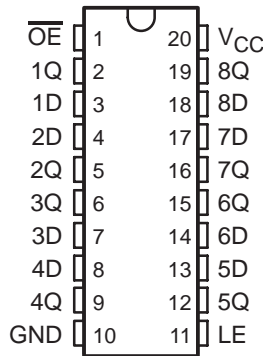


# SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

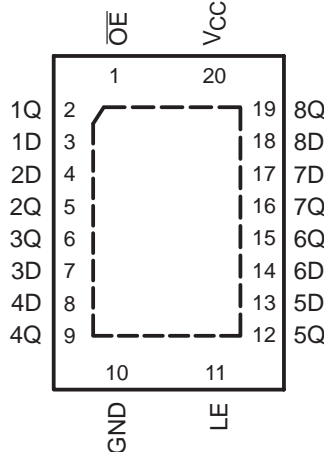
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- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 8.5 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

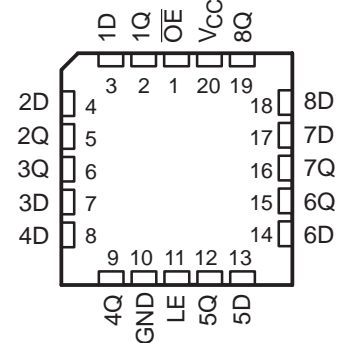
SN54LV373A ... J OR W PACKAGE  
SN74LV373A ... DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LV373A ... RGY PACKAGE  
(TOP VIEW)



SN54LV373A ... FK PACKAGE  
(TOP VIEW)



## description/ordering information

The 'LV373A devices are octal transparent D-type latches designed for 2-V to 5.5-V  $V_{CC}$  operation.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV373ARGYR	LV373A
	SOIC – DW	Tube of 25	SN74LV373ADW	LV373A
		Reel of 2500	SN74LV373ADWR	
	SOP – NS	Reel of 2000	SN74LV373ANSR	74LV373A
	SSOP – DB	Reel of 2000	SN74LV373ADBR	LV373A
	TSSOP – PW	Tube of 70	SN74LV373APW	LV373A
		Reel of 2000	SN74LV373APWR	
		Reel of 250	SN74LV373APWT	
TVSOP – DGV	Reel of 2000	SN74LV373ADGVR	LV373A	
VFBGA – GQN	Reel of 1000	SN74LV373AGQNR	LV373A	
-55°C to 125°C	CDIP – J	Tube of 20	SNJ54LV373AJ	SNJ54LV373AJ
	CFP – W	Tube of 85	SNJ54LV373AW	SNJ54LV373AW
	LCCC – FK	Tube of 55	SNJ54LV373AFK	SNJ54LV373AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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# SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

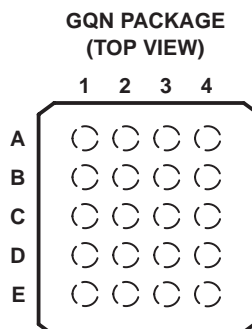
While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.



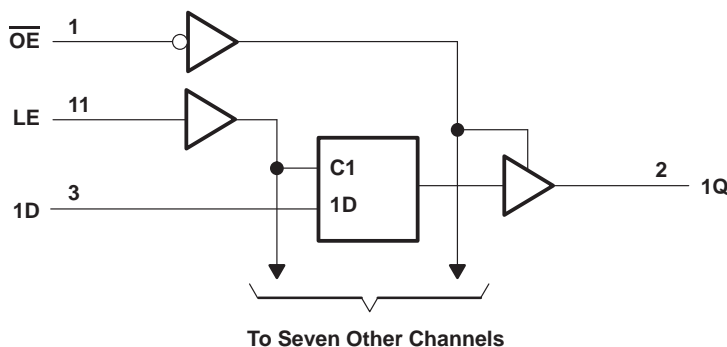
## terminal assignments

	1	2	3	4
A	1Q	$\overline{OE}$	$V_{CC}$	8Q
B	2D	7D	1D	8D
C	3Q	2Q	6Q	7Q
D	4D	5D	3D	6D
E	GND	4Q	LE	5Q

## FUNCTION TABLE (each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

**SN54LV373A, SN74LV373A**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	70°C/W
(see Note 3): DGV package .....	92°C/W
(see Note 3): DW package .....	58°C/W
(see Note 3): GQN package .....	78°C/W
(see Note 3): NS package .....	60°C/W
(see Note 3): PW package .....	83°C/W
(see Note 4): RGY package .....	37°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.  
4. The package thermal impedance is calculated in accordance with JESD 51-5.



# SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 5)

		SN54LV373A		SN74LV373A		UNIT	
		MIN	MAX	MIN	MAX		
$V_{CC}$	Supply voltage	2	5.5	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	0.5		V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$	$V_{CC} \times 0.3$			
$V_I$	Input voltage	0	5.5	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	0	$V_{CC}$	V
		3-state	0	5.5	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$		-50		-50	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		-2		-2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		-8		-8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16		-16	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$		50		50	$\mu\text{A}$
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		2		2	mA
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		8		8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$		200		200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$		100		100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		20		20	
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$	

NOTE 5: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	SN54LV373A			SN74LV373A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			2			
	$I_{OH} = -8\ \text{mA}$	3 V	2.48			2.48			
	$I_{OH} = -16\ \text{mA}$	4.5 V	3.8			3.8			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V				0.1			V
	$I_{OL} = 2\ \text{mA}$	2.3 V				0.4			
	$I_{OL} = 8\ \text{mA}$	3 V				0.44			
	$I_{OL} = 16\ \text{mA}$	4.5 V				0.55			
$I_I$	$V_I = 5.5\ \text{V or GND}$	0 to 5.5 V				$\pm 1$			$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}\ \text{or GND}$	5.5 V				$\pm 5$			$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}\ \text{or GND, } I_O = 0$	5.5 V				20			$\mu\text{A}$
$I_{off}$	$V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$	0				5			$\mu\text{A}$
$C_i$	$V_I = V_{CC}\ \text{or GND}$	3.3 V	2.9			2.9			pF

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# SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54LV373A		SN74LV373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	6		6.5		6.5		ns
$t_{su}$	Setup time, data before LE↓	4.5		5		5		ns
$t_h$	Hold time, data after LE↓	1.5		1.5		1.5		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54LV373A		SN74LV373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	5		5		5		ns
$t_{su}$	Setup time, data before LE↓	4		4		4		ns
$t_h$	Hold time, data after LE↓	1		1		1		ns

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ\text{C}$		SN54LV373A		SN74LV373A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	5		5		5		ns
$t_{su}$	Setup time, data before LE↓	4		4		4		ns
$t_h$	Hold time, data after LE↓	1		1		1		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	8.3*	15.2*	1*	17*	1	17	ns	
	LE	Q		9.1*	15.7*	1*	19*	1	19		
$t_{en}$	$\overline{OE}$	Q		8.9*	15.8*	1*	19*	1	19		
$t_{dis}$	$\overline{OE}$	Q		6.2*	12.6*	1*	15*	1	15		
$t_{pd}$	D	Q	$C_L = 50\text{ pF}$	10.4	18	1	21	1	21	ns	
	LE	Q		11.1	18.6	1	22	1	22		
$t_{en}$	$\overline{OE}$	Q		10.9	18.8	1	22	1	22		
$t_{dis}$	$\overline{OE}$	Q		8.3	17.4	1	19	1	19		
$t_{sk(o)}$						2			2		

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV373A		SN74LV373A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	5.8*	11.4*	1*	13.5*	1	13.5	ns		
	LE	Q		6.4*	11*	1*	13*	1	13			
$t_{en}$	$\overline{OE}$	Q		6.3*	11.4*	1*	13.5*	1	13.5			
$t_{dis}$	$\overline{OE}$	Q		4.7*	10*	1*	12*	1	12			
$t_{pd}$	D	Q		$C_L = 50\text{ pF}$	7.3	14.9	1	17	1		17	ns
	LE	Q			7.8	14.5	1	16.5	1		16.5	
$t_{en}$	$\overline{OE}$	Q			7.7	14.9	1	17	1		17	
$t_{dis}$	$\overline{OE}$	Q			6	13.2	1	15	1		15	
$t_{sk(o)}$					1.5				1.5			

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV373A		SN74LV373A		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	D	Q	$C_L = 15\text{ pF}$	4.1*	7.2*	1*	8.5*	1	8.5	ns		
	LE	Q		4.5*	7.2*	1*	8.5*	1	8.5			
$t_{en}$	$\overline{OE}$	Q		4.5*	8.1*	1*	9.5*	1	9.5			
$t_{dis}$	$\overline{OE}$	Q		3.3*	7.2*	1*	8.5*	1	8.5			
$t_{pd}$	D	Q		$C_L = 50\text{ pF}$	5.1	9.2	1	10.5	1		10.5	ns
	LE	Q			5.5	9.2	1	10.5	1		10.5	
$t_{en}$	$\overline{OE}$	Q			5.5	10.1	1	11.5	1		11.5	
$t_{dis}$	$\overline{OE}$	Q			4	9.2	1	10.5	1		10.5	
$t_{sk(o)}$					1				1			

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 6)

PARAMETER		SN74LV373A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.6	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage		2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance		Outputs enabled	3.3 V	
		$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	5 V	19.5	

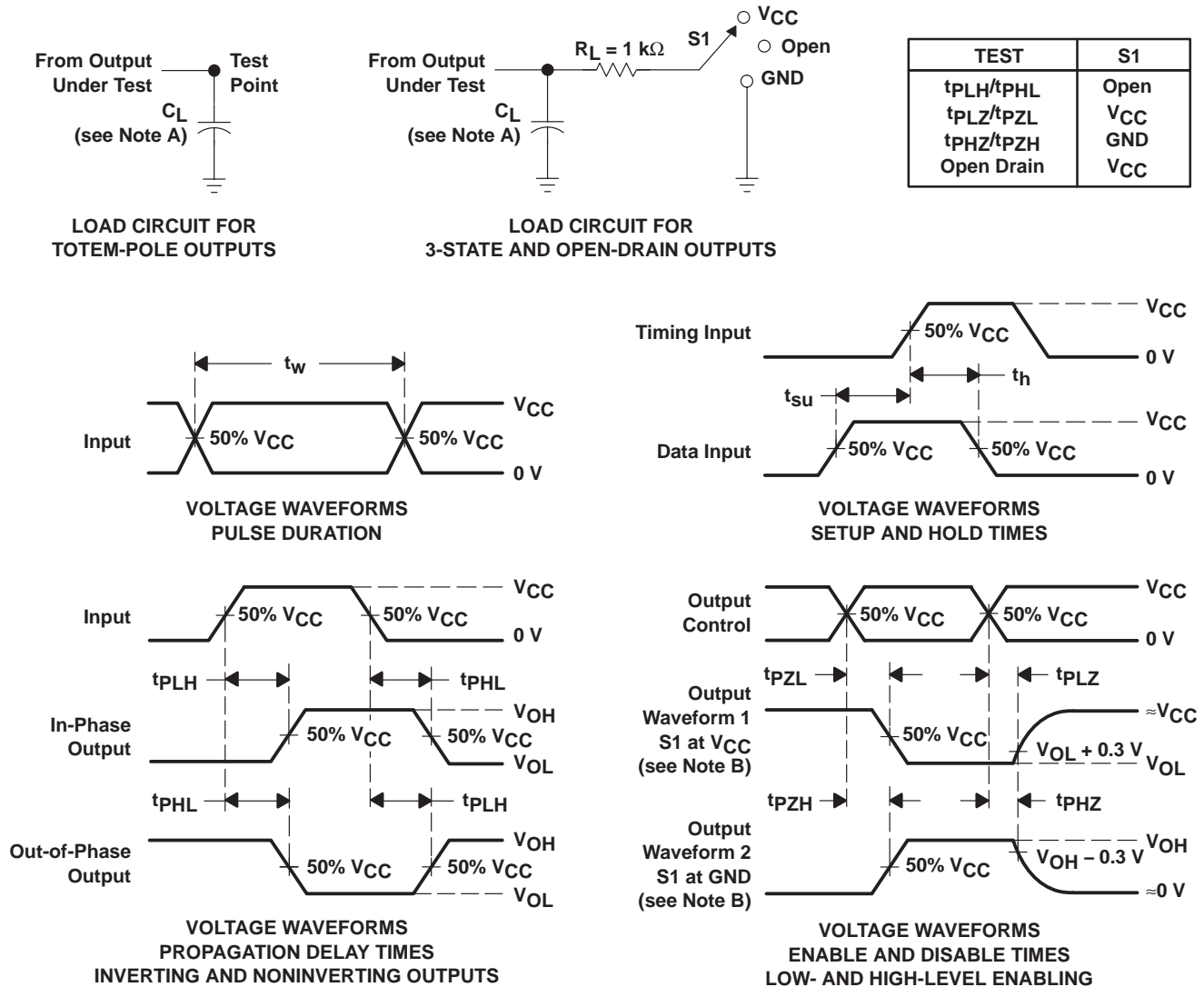
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# SN54LV373A, SN74LV373A OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV373ADBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV373ADGVR	ACTIVE	TVSOP	DGV	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV373ADW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LV373ADWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LV373AGQNR	ACTIVE	VFBGA	GQN	20	1000	None	SNPB	Level-1-240C-UNLIM
SN74LV373ANSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LV373APW	ACTIVE	TSSOP	PW	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV373APWR	ACTIVE	TSSOP	PW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV373APWT	ACTIVE	TSSOP	PW	20	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LV373ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

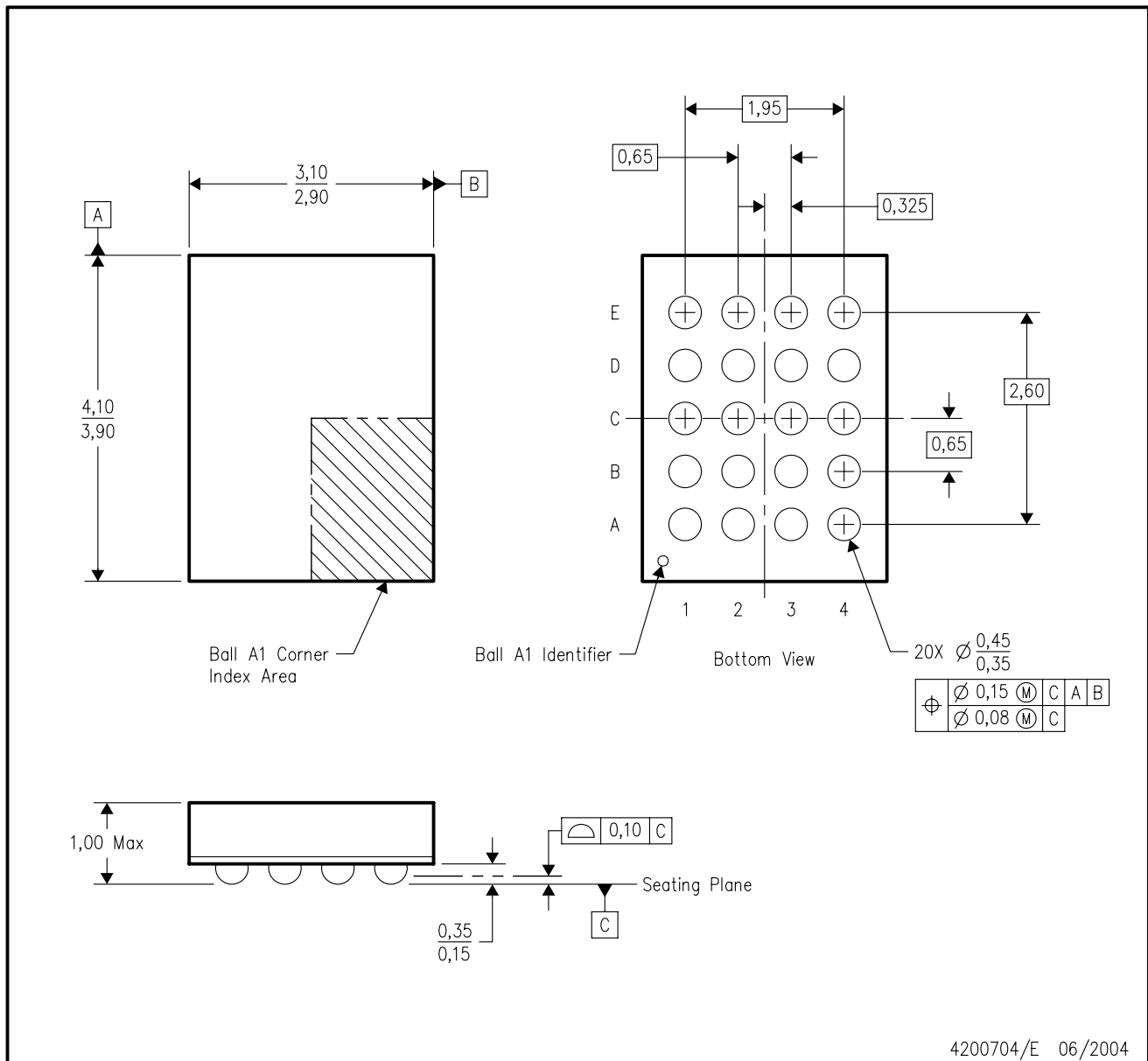
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



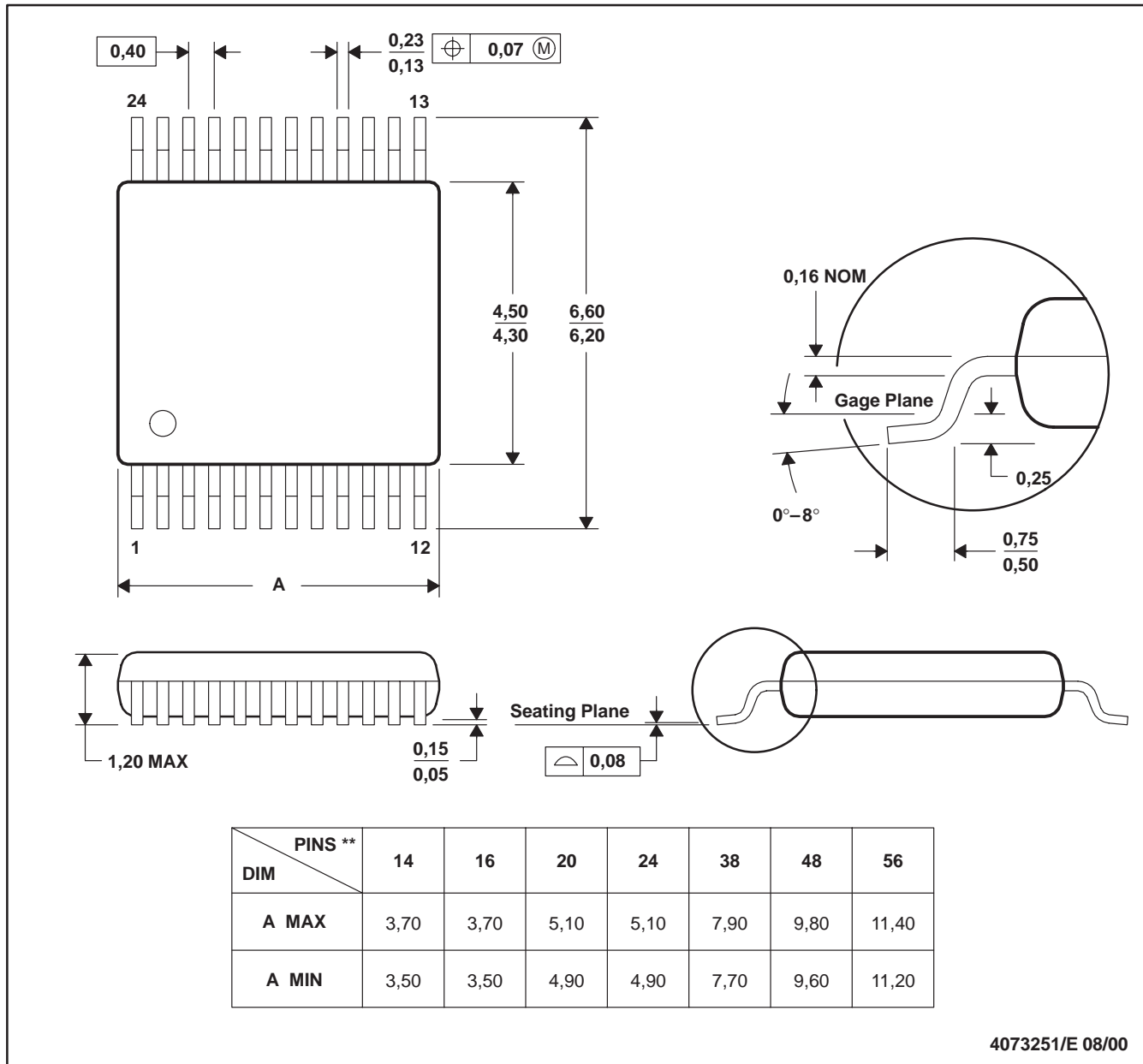
4200704/E 06/2004

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BC.
  - D. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

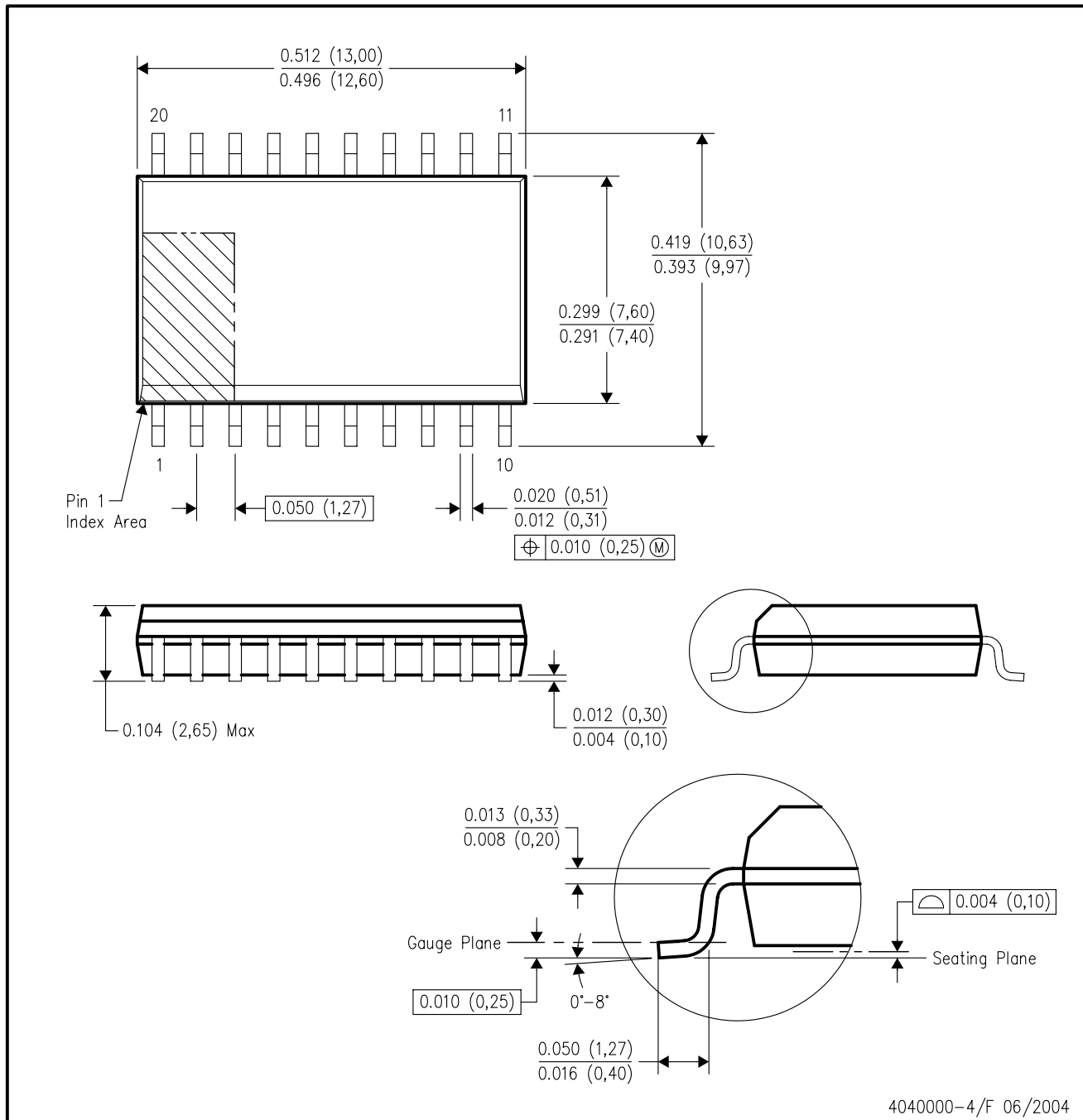
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

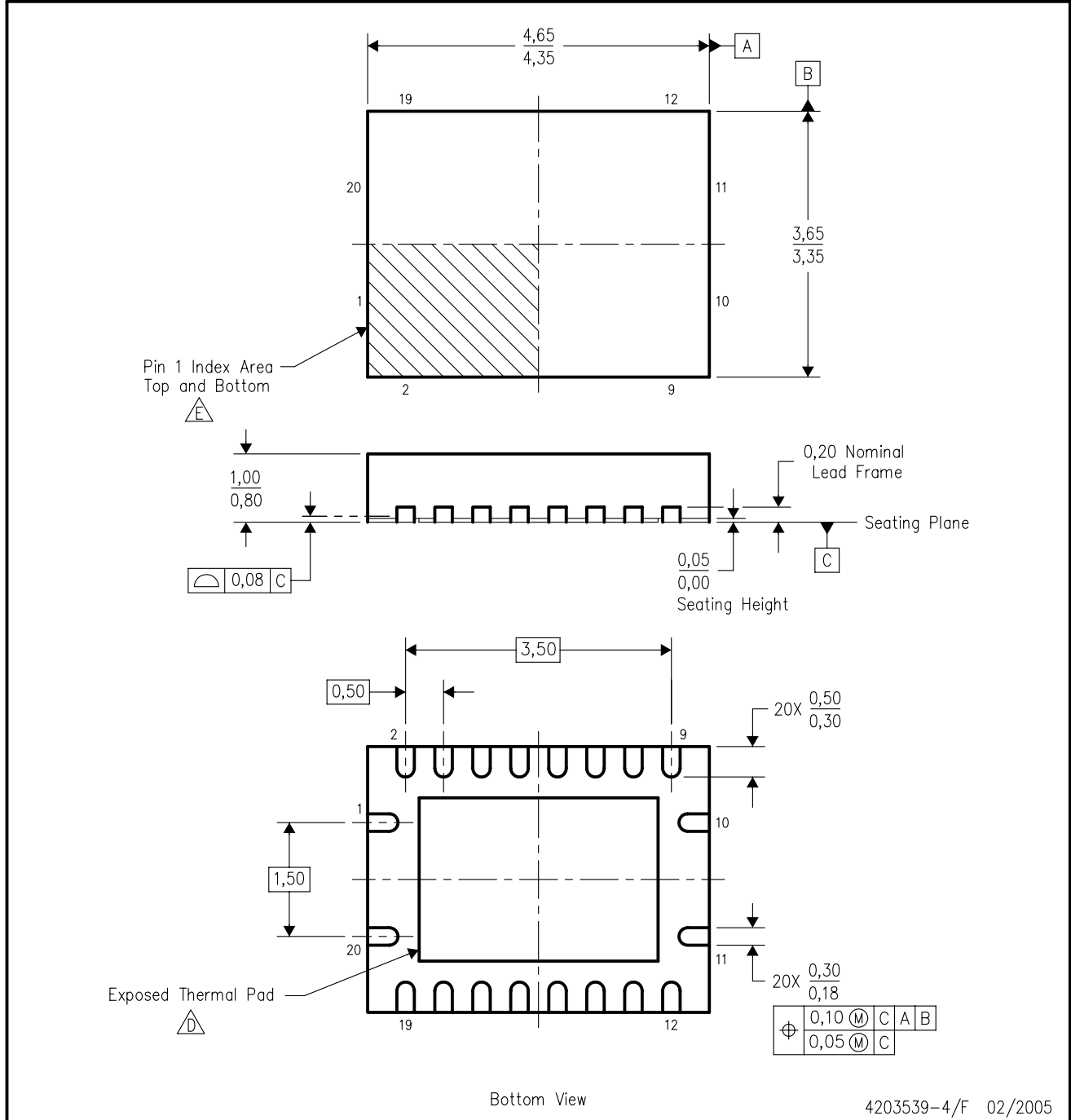
PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



4203539-4/F 02/2005

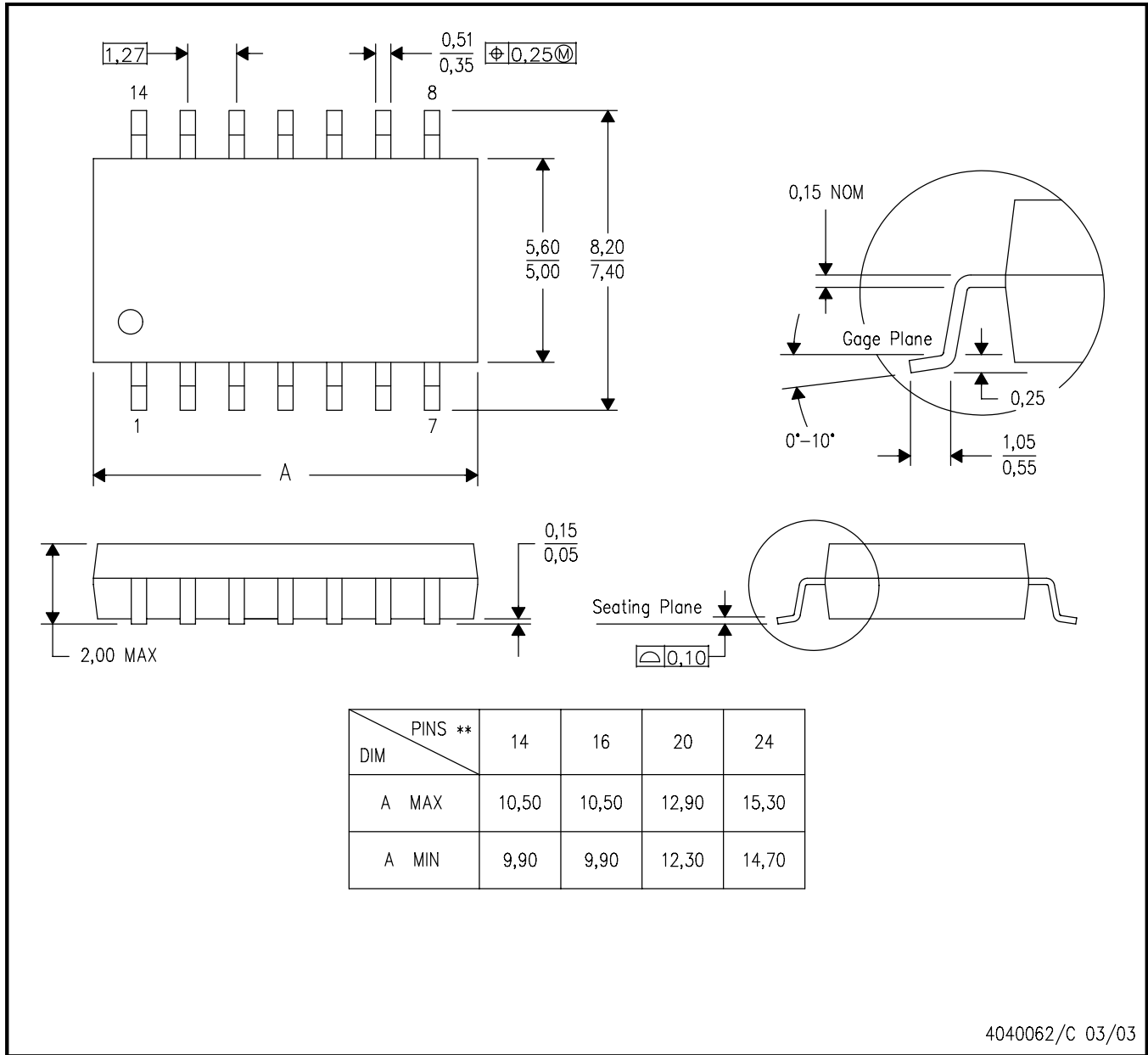
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - F. Package complies to JEDEC MO-241 variation BC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

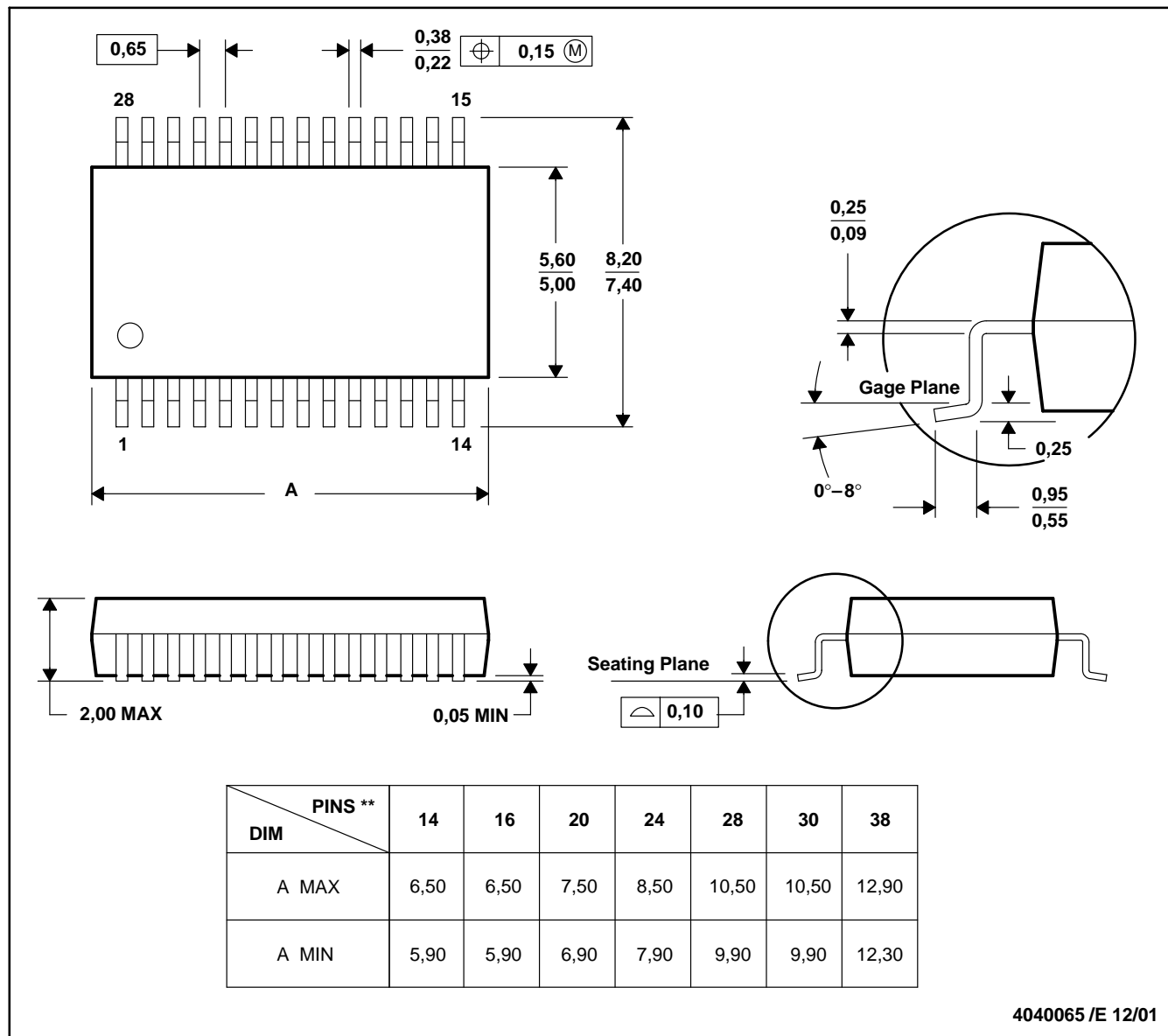


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

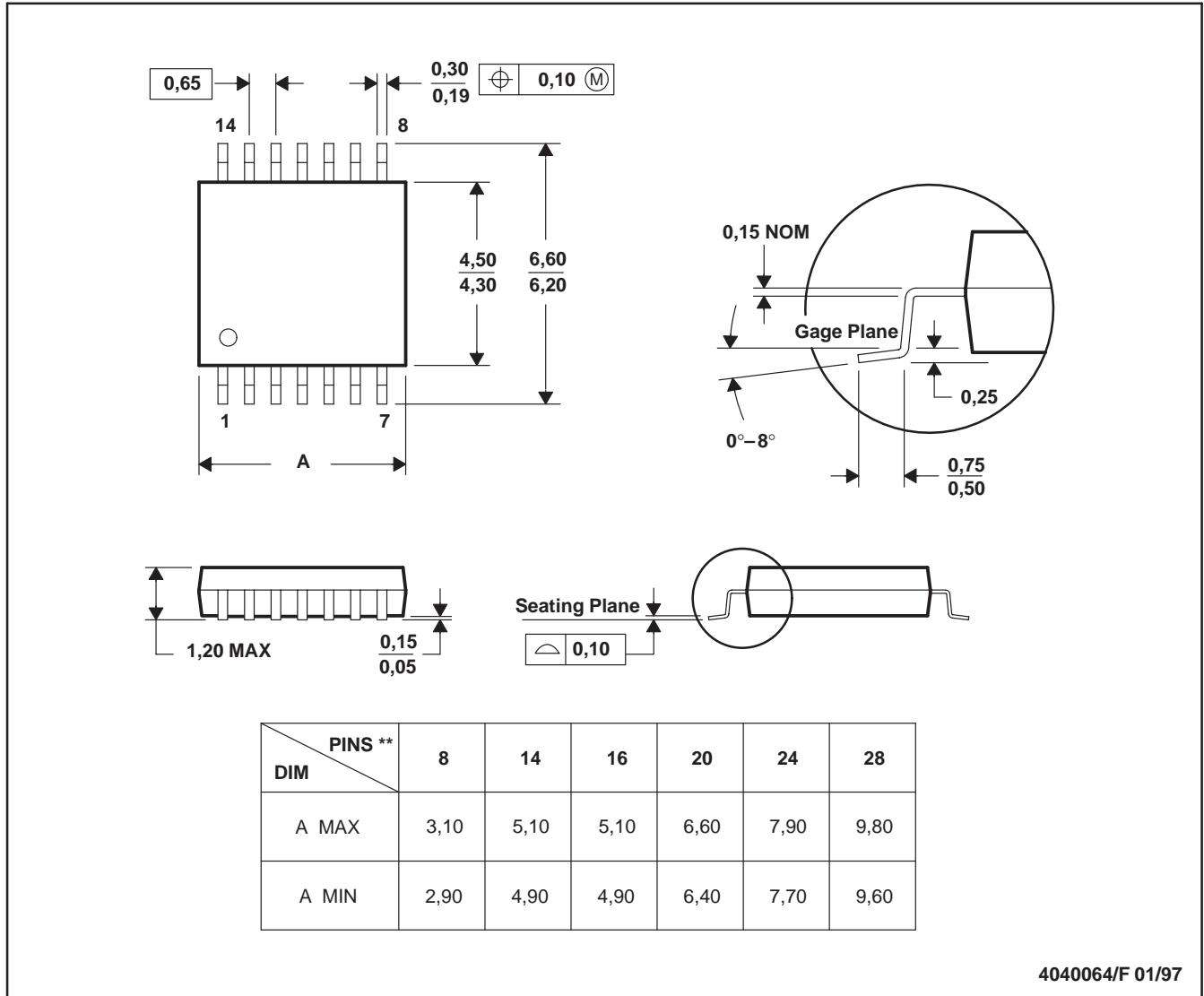


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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