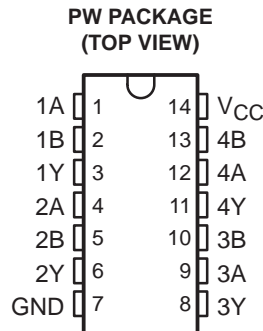


# SN74LV86A-Q1 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

SCLS534B – AUGUST 2003 – REVISED MAY 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 2-V to 5.5-V  $V_{CC}$  Operation
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2.3 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports



† Contact factory for details. Q100 qualification data available on request.

## description/ordering information

The SN74LV86A is a quadruple 2-input exclusive-OR gate designed for 2-V to 5.5-V  $V_{CC}$  operation.

This device contains four independent 2-input exclusive-OR gates. It performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

## ORDERING INFORMATION

$T_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	TSSOP – PW	Tape and reel	SN74LV86ATPWRQ1	LV86AT

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

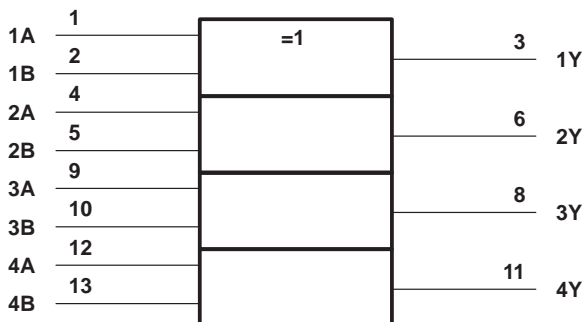
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# SN74LV86A-Q1 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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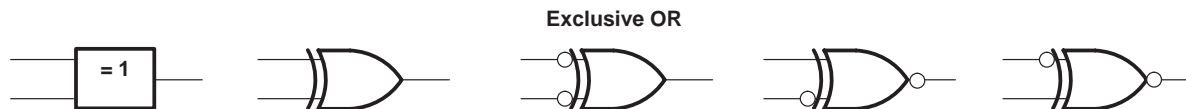
## logic symbol†



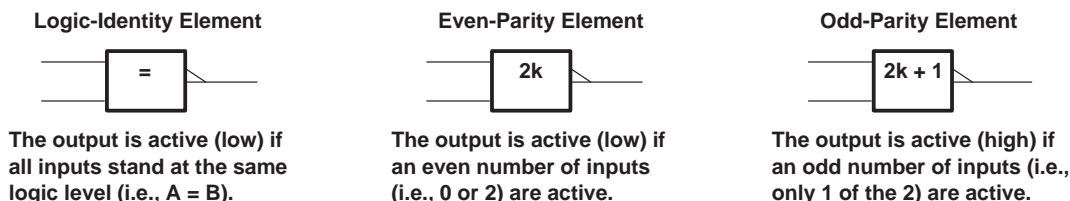
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'LV86A gate in positive logic; negation can be shown at any two ports.



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 5.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74LV86A-Q1 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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## recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2	5.5	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	$V_{CC} \times 0.3$		
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	$V_{CC} \times 0.3$		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$V_{CC} \times 0.3$		
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	-50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	-6		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-12		
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	$\mu\text{A}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	2	mA	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	6		
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	12		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	200	ns/V
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	0	100	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0	20	
$T_A$	Operating free-air temperature	-40	105	$^{\circ}\text{C}$	

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	2 V to 5.5 V	$V_{CC}-0.1$			V
	$I_{OH} = -2\ \text{mA}$	2.3 V	2			
	$I_{OH} = -6\ \text{mA}$	3 V	2.48			
	$I_{OH} = -12\ \text{mA}$	4.5 V	3.8			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	2 V to 5.5 V			0.1	V
	$I_{OL} = 2\ \text{mA}$	2.3 V			0.4	
	$I_{OL} = 6\ \text{mA}$	3 V			0.44	
	$I_{OL} = 12\ \text{mA}$	4.5 V			0.55	
$I_I$	$V_I = 5.5\text{ V or GND}$	0 to 5.5 V			$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}\text{ or GND, } I_O = 0$	5.5 V			20	$\mu\text{A}$
$I_{off}$	$V_I\text{ or }V_O = 0\text{ to }5.5\text{ V}$	0			5	$\mu\text{A}$
$C_i$	$V_I = V_{CC}\text{ or GND}$	3.3 V		1.4		pF



# SN74LV86A-Q1

## QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE

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switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A or B	Y	$C_L = 50\text{ pF}$	10.5	22.6		1	26.5	ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A or B	Y	$C_L = 50\text{ pF}$	7.4	14.5		1	16.5	ns

switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A or B	Y	$C_L = 50\text{ pF}$	5.3	8.8		1	10	ns

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

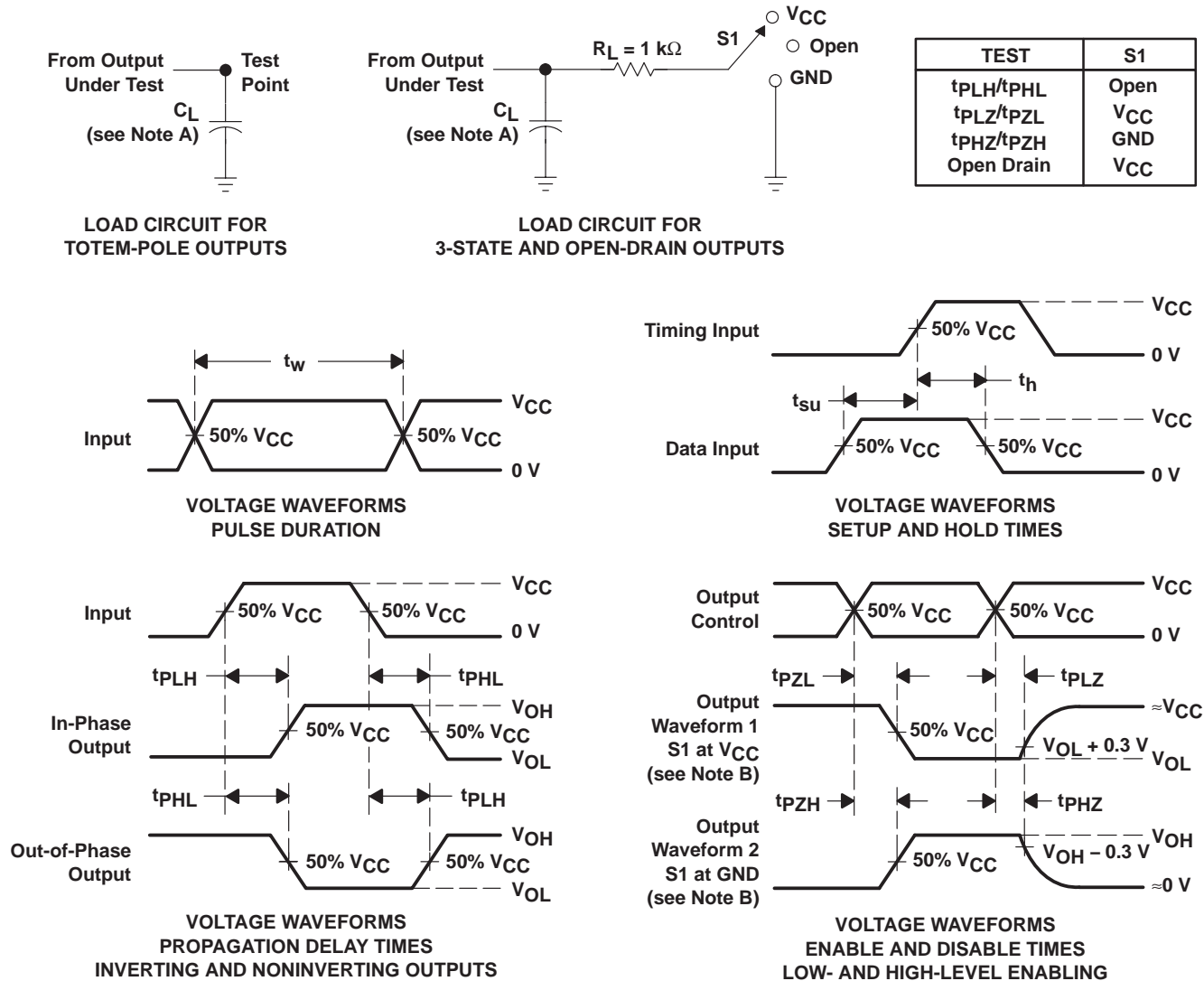
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$	-0.1		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.1		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	8.4	pF
			5 V	8.8	

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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