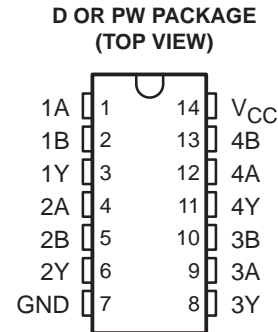


# SN74LVC00A-Q1 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCAS703A – SEPTEMBER 2003 – REVISED MAY 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operates From 2 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 4.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$



† Contact factory for details. Q100 qualification data available on request.

## description/ordering information

The SN74LVC00A-Q1 quadruple 2-input positive-NAND gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The device performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

## ORDERING INFORMATION

$T_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC00AQDRQ1	LVC00AQ
	TSSOP – PW	Reel of 2000	SN74LVC00AQPWRQ1	LVC00AQ

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## logic diagram, each gate (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN74LVC00A-Q1

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	-50 mA
Continuous output current, $I_O$	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	86°C/W
PW package	113°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V	
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V	-12	mA	
		$V_{CC} = 3$ V	-24		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V	12	mA	
		$V_{CC} = 3$ V	24		
$T_A$	Operating free-air temperature	-40	125	°C	

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74LVC00A-Q1 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	2.7 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			
		3 V	2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	2.7 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		3 V			0.55	
	I <sub>OL</sub> = 24 mA	3 V				
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		5		pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	5.1		1	4.3	ns

**operating characteristics, T<sub>A</sub> = 25°C**

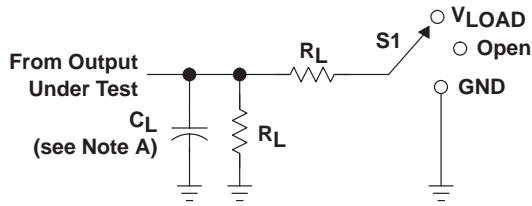
PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
		TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance per gate	f = 10 MHz	18	19	pF

# SN74LVC00A-Q1

## QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCAS703A – SEPTEMBER 2003 – REVISED MAY 2004

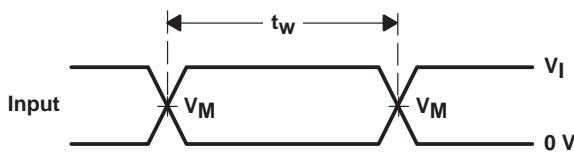
### PARAMETER MEASUREMENT INFORMATION



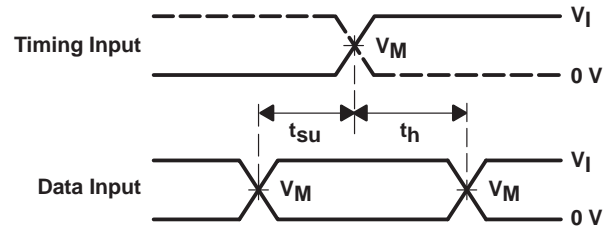
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	VLOAD
$t_{PHZ}/t_{PZH}$	GND

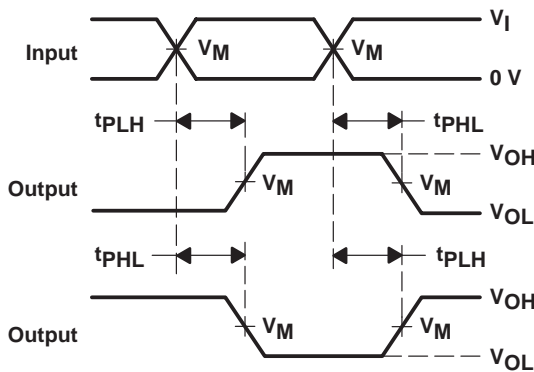
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



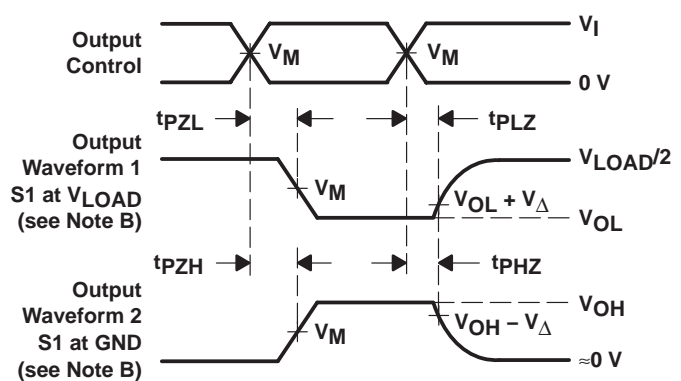
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



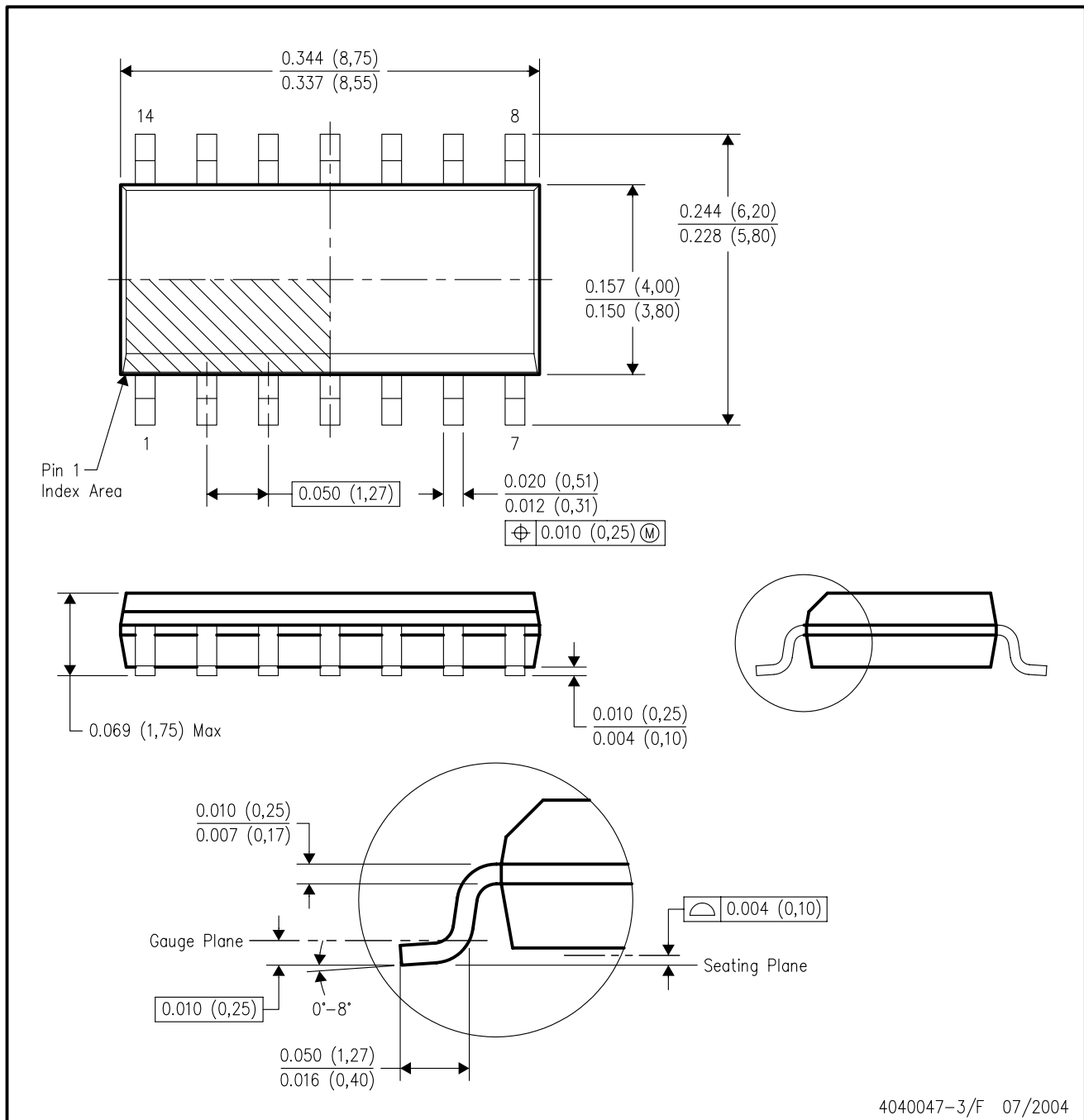
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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