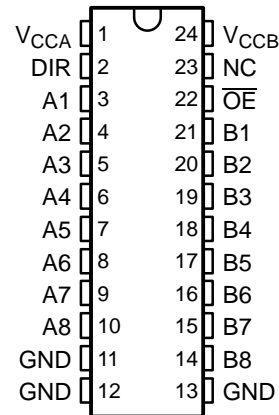


## FEATURES

- Bidirectional Voltage Translator
- 2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port
- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DB, DBQ, DW, NS, OR PW PACKAGE  
(TOP VIEW)



NC - No internal connection

## DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track  $V_{CCB}$ , which accepts voltages from 3 V to 5.5 V, and the A port is designed to track  $V_{CCA}$ , which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR,  $\overline{OE}$ ) is powered by  $V_{CCA}$ .

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube of 25	SN74LVCC3245ADW	LVCC3245A
		Reel of 2000	SN74LVCC3245ADWR	
	SOP – NS	Reel of 2000	SN74LVCC3245ANSR	LVCC3245A
	SSOP – DB	Reel of 2000	SN74LVCC3245ADBR	LH245A
	SSOP (QSOP) – DBQ	Reel of 2500	SN74LVCC3245ADBQR	LVCC3245A
	TSSOP – PW	Tube of 60	SN74LVCC3245APW	LH245A
		Reel of 2000	SN74LVCC3245APWR	
		Reel of 250	SN74LVCC3245APWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (EACH TRANSCEIVER)

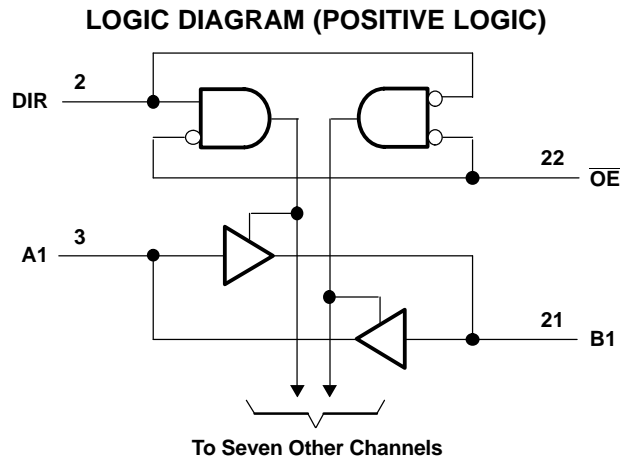
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS**

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**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CCA}$ $V_{CCB}$	Supply voltage range	-0.5	6	V	
$V_I$	Input voltage range	All A ports <sup>(2)</sup>	-0.5	$V_{CCA} + 0.5$	V
		All B ports <sup>(3)</sup>	-0.5	$V_{CCB} + 0.5$	
		Except I/O ports <sup>(2)</sup>	-0.5	$V_{CCA} + 0.5$	
$V_O$	Output voltage range <sup>(3)</sup>	All A ports	-0.5	$V_{CCA} + 0.5$	V
		All B ports	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current		$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current		$V_O < 0$	-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND			±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DB package		63	°C/W
		DBQ package		61	
		DW package		46	
		NS package		65	
		PW package		88	
$T_{stg}$	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This value is limited to 4.6 V maximum.
- (3) This value is limited to 6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

		$V_{CCA}$	$V_{CCB}$	MIN	NOM	MAX	UNIT
$V_{CCA}$	Supply voltage			2.3	3.3	3.6	V
$V_{CCB}$	Supply voltage			3	5	5.5	V
$V_{IHA}$	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
$V_{IHB}$	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			
$V_{ILA}$	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
$V_{ILB}$	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
$V_{IH}$	High-level input voltage (control pins) (referenced to $V_{CCA}$ )	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
$V_{IL}$	Low-level input voltage (control pins) (referenced to $V_{CCA}$ )	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
$V_{IA}$	Input voltage			0		$V_{CCA}$	V
$V_{IB}$	Input voltage			0		$V_{CCB}$	V
$V_{OA}$	Output voltage			0		$V_{CCA}$	V
$V_{OB}$	Output voltage			0		$V_{CCB}$	V
$I_{OHA}$	High-level output current	2.3 V	3 V			-8	mA
		2.7 V	3 V			-12	
		3 V	3 V			-24	
		2.7 V	4.5 V			-24	
$I_{OHB}$	High-level output current	2.3 V	3 V			-12	mA
		2.7 V	3 V			-12	
		3 V	3 V			-24	
		2.7 V	4.5 V			-24	
$I_{OLA}$	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	

(1) All unused inputs of the device must be held at the associated  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**Recommended Operating Conditions (continued)**

		$V_{CCA}$	$V_{CCB}$	MIN	NOM	MAX	UNIT
$I_{OLB}$	Low-level output current	2.3 V	3 V			12	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate					10	ns/V
$T_A$	Operating free-air temperature			-40		85	°C

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP	MAX	UNIT
V <sub>OHA</sub>		I <sub>OH</sub> = –100 μA	3 V	3 V	2.9	3		V
		I <sub>OH</sub> = –8 mA	2.3 V	3 V	2			
		I <sub>OH</sub> = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I <sub>OH</sub> = –24 mA	3 V	3 V	2.2	2.6		
	2.7 V		4.5 V	2	2.3			
V <sub>OHB</sub>		I <sub>OH</sub> = –100 μA	3 V	3 V	2.9	3		V
		I <sub>OH</sub> = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I <sub>OH</sub> = –24 mA	3 V	3 V	2.2	2.6		
	2.7 V		4.5 V	3.2	4.2			
V <sub>OLA</sub>		I <sub>OL</sub> = 100 μA	3 V	3 V			0.1	V
		I <sub>OL</sub> = 8 mA	2.3 V	3 V			0.6	
		I <sub>OL</sub> = 12 mA	2.7 V	3 V		0.1	0.5	
			3 V	3 V		0.2	0.5	
	I <sub>OL</sub> = 24 mA	2.7 V	4.5 V		0.2	0.5		
V <sub>OLB</sub>		I <sub>OL</sub> = 100 μA	3 V	3 V			0.1	V
		I <sub>OL</sub> = 12 mA	2.3 V	3 V			0.4	
			3 V	3 V		0.2	0.5	
		I <sub>OL</sub> = 24 mA	2.7 V	4.5 V		0.2	0.5	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.6 V	3.6 V		±0.1	±1	μA
				5.5 V		±0.1	±1	
I <sub>OZ</sub> <sup>(1)</sup>	A or B ports	V <sub>O</sub> = V <sub>CCA/B</sub> or GND, V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.6 V	3.6 V		±0.5	±5	μA
I <sub>CCA</sub>	B to A	A port = V <sub>CCA</sub> or GND, I <sub>O</sub> = 0	3.6 V	Open		5	50	μA
		B port = V <sub>CCB</sub> or GND, I <sub>O</sub> = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I <sub>CCB</sub>	A to B	A port = V <sub>CCA</sub> or GND, I <sub>O</sub> = 0	3.6 V	3.6 V		5	50	μA
				5.5 V		8	80	
ΔI <sub>CCA</sub> <sup>(2)</sup>	A port	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, $\overline{OE}$ at GND and DIR at V <sub>CCA</sub>	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, DIR at V <sub>CCA</sub>	3.6 V	3.6 V		0.35	0.5	
	DIR	V <sub>I</sub> = V <sub>CCA</sub> – 0.6 V, Other inputs at V <sub>CCA</sub> or GND, $\overline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI <sub>CCB</sub> <sup>(2)</sup>	B port	V <sub>I</sub> = V <sub>CCB</sub> – 2.1 V, Other inputs at V <sub>CCB</sub> or GND, $\overline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CCA</sub> or GND	Open	Open		4		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	3.3 V	5 V		18.5		pF

 (1) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

 (2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V<sub>CC</sub>.

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**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ , $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$ , $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CCA} = 2.7\text{ V TO } 3.6\text{ V}$ , $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PHL}$	A	B	1	9.4	1	6	1	7.1	ns
$t_{PLH}$			1	9.1	1	5.3	1	7.2	
$t_{PHL}$	B	A	1	11.2	1	5.8	1	6.4	ns
$t_{PLH}$			1	9.9	1	7	1	7.6	
$t_{PZL}$	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
$t_{PZH}$			1	12.9	1	9.5	1	9.5	
$t_{PZL}$	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
$t_{PZH}$			1	12.8	1	8.4	1	9.9	
$t_{PLZ}$	$\overline{OE}$	A	1	7.1	1	7	1	6.6	ns
$t_{PHZ}$			1	6.9	1	7.8	1	6.9	
$t_{PLZ}$	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
$t_{PHZ}$			1	8.9	1	7	1	7.9	

**Operating Characteristics**

$V_{CCA} = 3.3\text{ V}$ ,  $V_{CCB} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance per transceiver	$C_L = 50$ , $f = 10\text{ MHz}$	38	pF
			Outputs enabled	
			4.5	
			Outputs disabled	

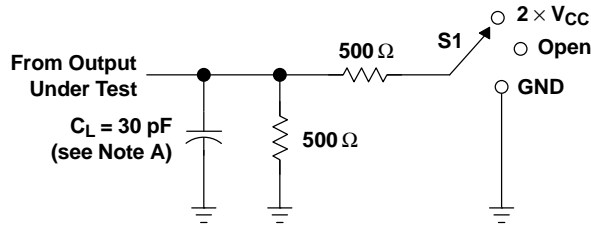
**Power-Up Considerations<sup>(1)</sup>**

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ( $V_{CCA}$  for all four of these devices).
3. Tie  $\overline{OE}$  to  $V_{CCA}$  with a pullup resistor so that it ramps with  $V_{CCA}$ .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with  $V_{CCA}$ . Otherwise, keep DIR low.

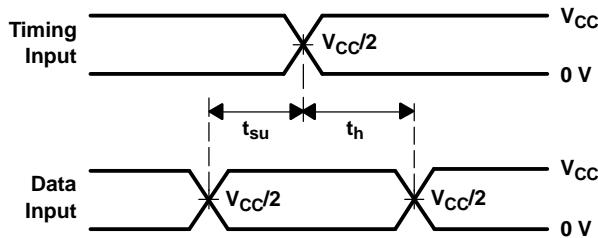
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION FOR A PORT  
 $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  AND  $V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$

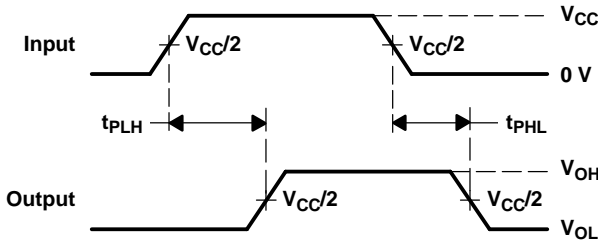


LOAD CIRCUIT

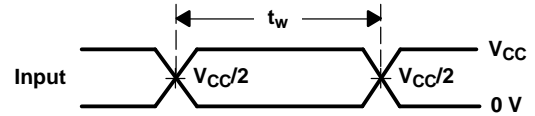
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



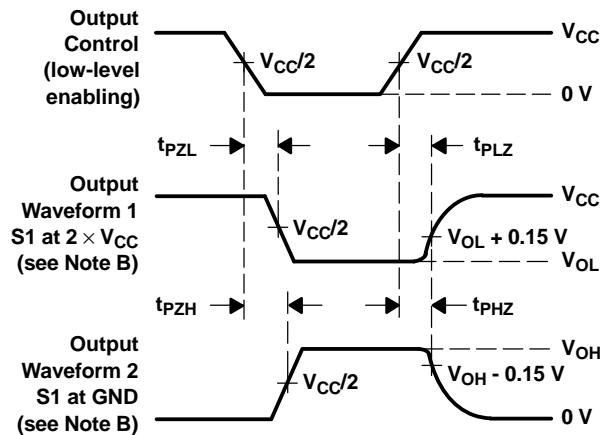
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

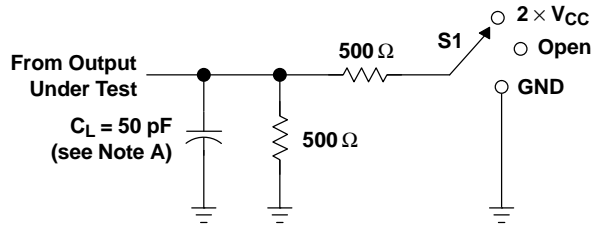
Figure 1. Load Circuit and Voltage Waveforms

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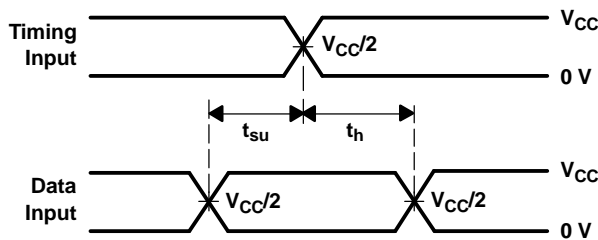
**PARAMETER MEASUREMENT INFORMATION FOR B PORT**

$V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  AND  $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$

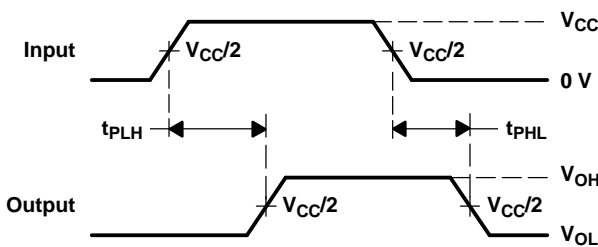


**LOAD CIRCUIT**

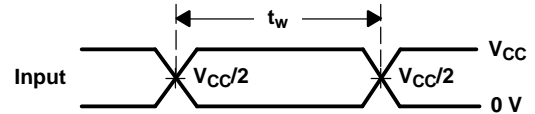
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



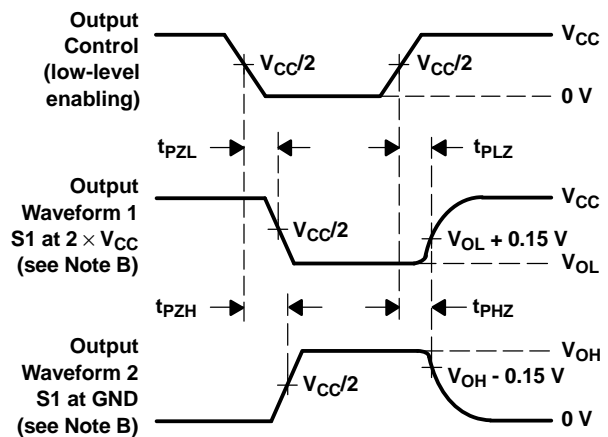
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



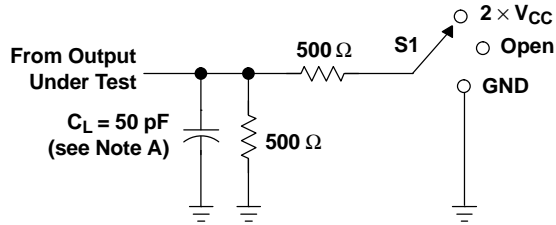
**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

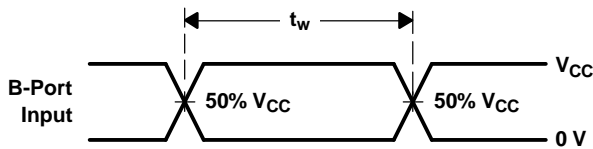
PARAMETER MEASUREMENT INFORMATION FOR B PORT

$V_{CCA} = 3.6\text{ V}$  and  $v_{CCB} = 5.5\text{ V}$

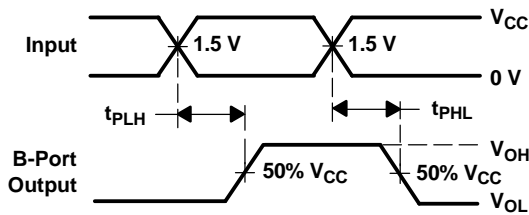


LOAD CIRCUIT

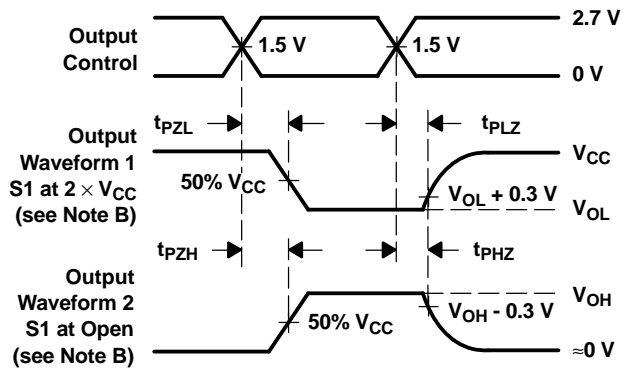
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
NONINVERTING OUTPUTS

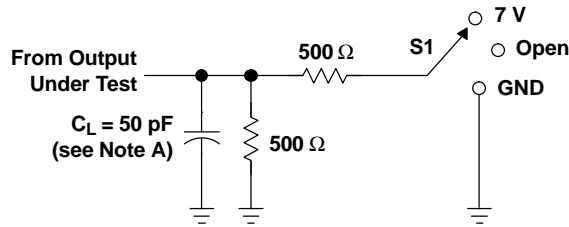


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

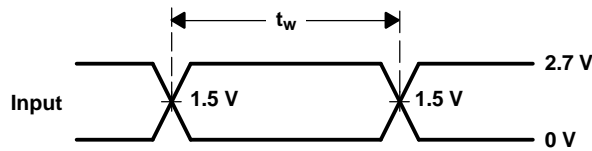
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT  
 $V_{CCA}$  AND  $V_{CCB} = 3.6\text{ V}$

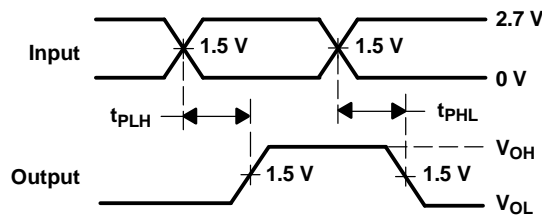


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

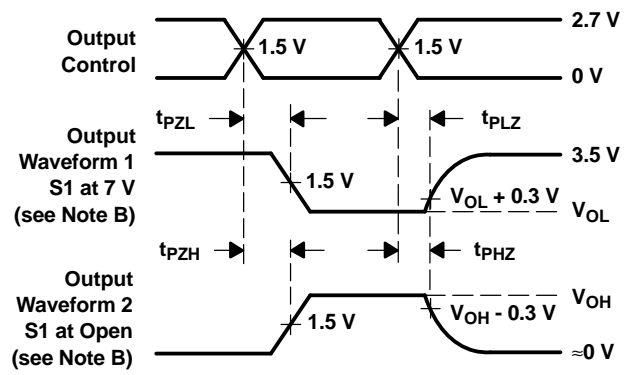
LOAD CIRCUIT



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVCC3245ADBLE	OBSOLETE	SSOP	DB	24		None	Call TI	Call TI
SN74LVCC3245ADBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVCC3245APWLE	OBSOLETE	TSSOP	PW	24		None	Call TI	Call TI
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265