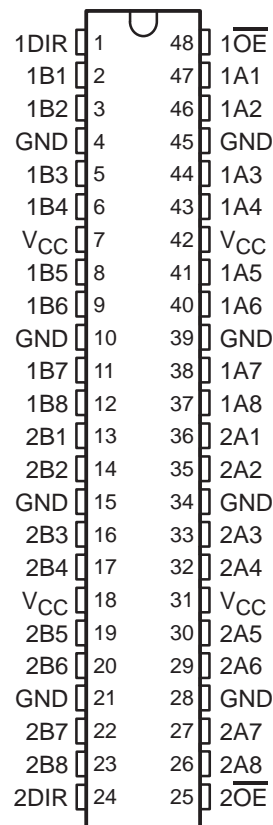


SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS714B – FEBRUARY 2000 – REVISED SEPTEMBER 2003

- Members of the Texas Instruments Widebus™ Family
- A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54LVT162245A . . . WD PACKAGE
SN74LVT162245A . . . DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'LVT162245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVT162245ADL	LVT162245A
		Tape and reel	SN74LVT162245ADLR	
	TSSOP – DGG	Tape and reel	SN74LVT162245ADGGR	LVT162245A
	VFBGA – GQL	Tape and reel	SN74LVT162245AGQLR	LZ245A
VFBGA – ZQL (Pb-free)			SN74LVT162245AZQLR	
–55°C to 125°C	CFP – WD	Tube	SNJ54LVT162245AWD	SNJ54LVT162245AWD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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 **TEXAS
INSTRUMENTS**

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SN54LVT162245A, SN74LVT162245A

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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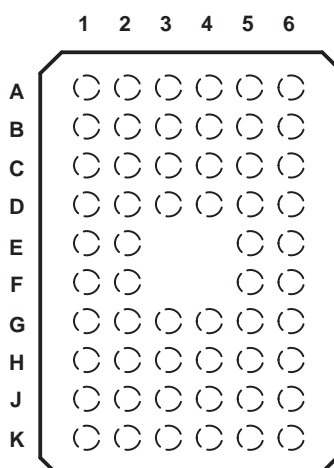
description/ordering information (continued)

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$\overline{1OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CC}	V_{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CC}	V_{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$\overline{2OE}$

NC – No internal connection

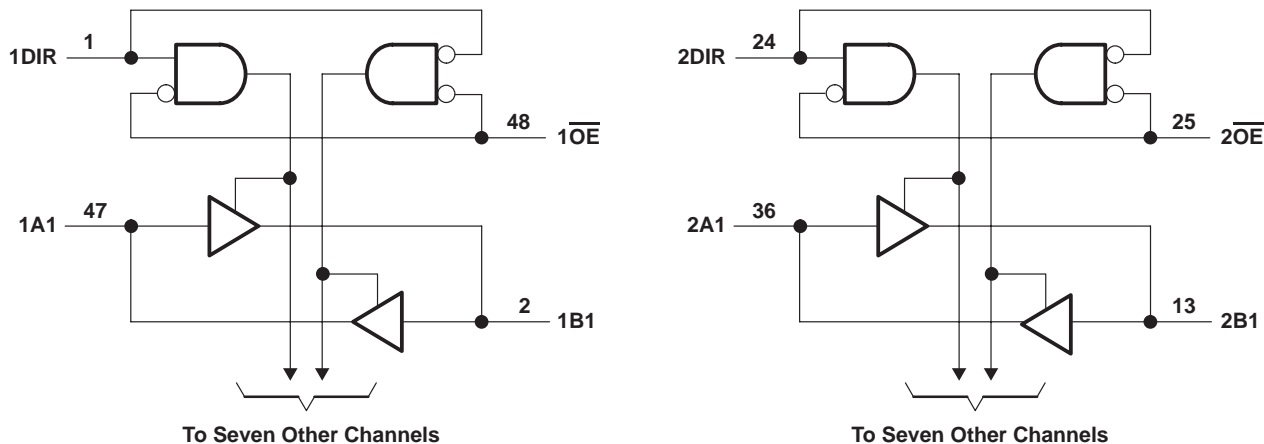
FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVT162245A (B port)	96 mA
SN74LVT162245A (B port)	128 mA
A port	30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT162245A (B port)	48 mA
SN74LVT162245A (B port)	64 mA
A port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	70°C/W
DL package	63°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54LVT162245A, SN74LVT162245A

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LVT162245A		SN74LVT162245A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current	A port		-12		mA
		B port		-24		
I_{OL}	Low-level output current	A port		12		mA
		B port		48		
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVT162245A			SN74LVT162245A			UNIT		
			MIN	TYP†	MAX	MIN	TYP†	MAX			
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$	-1.2			-1.2			V		
V_{OH}	A port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V		
		$V_{CC} = 3\text{ V}$, $I_{OH} = -12\text{ mA}$	2			2					
	B port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$					
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4					
		$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2							
			$I_{OH} = -32\text{ mA}$				2				
V_{OL}	A port	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$				0.2			V		
		$V_{CC} = 3\text{ V}$, $I_{OL} = 12\text{ mA}$				0.8					
	B port	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$				0.2				
			$I_{OL} = 24\text{ mA}$				0.5				
		$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$				0.4				
			$I_{OL} = 32\text{ mA}$				0.5				
			$I_{OL} = 48\text{ mA}$				0.55				
			$I_{OL} = 64\text{ mA}$				0.55				
	I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$				± 1			μA	
			$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$				10				
A or B ports‡		$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$				20				
			$V_I = V_{CC}$				5				
			$V_I = 0$				-10				
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$							± 100			
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$				$\pm 100^*$			± 100			
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$				$\pm 100^*$			± 100			
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high				0.19			mA		
		Outputs low				5					
		Outputs disabled				0.19					
ΔI_{CC}^{\S}	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.3			0.2			
C_i	$V_I = 3\text{ V or }0$				4			pF			
C_{io}	$V_O = 3\text{ V or }0$				10			pF			

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at V_{CC} or GND.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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SN54LVT162245A, SN74LVT162245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

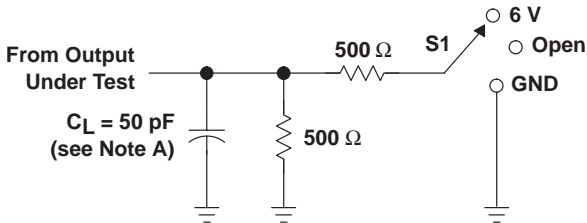
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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT162245A				SN74LVT162245A				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A	B	1	3.5	4		1	2.3	3.3	3.7		ns
t_{PHL}			1	3.5	3.9		1	2.2	3.3	3.5		
t_{PLH}	B	A	1	4.3	5.3		1	2.8	4	4.6		ns
t_{PHL}			1	4.2	4.5		1	2.5	3.4	3.6		
t_{PZH}	\overline{OE}	B	1	4.8	5.9		1	2.8	4.6	5.4		ns
t_{PZL}			1	4.8	5.5		1	3	4.6	5.2		
t_{PZH}	\overline{OE}	A	1	5.5	7.2		1	3.3	5.3	6.3		ns
t_{PZL}			1	5.4	6.4		1	3.3	5.1	5.8		
t_{PHZ}	\overline{OE}	B	1.5	5.5	5.8		1.5	3.8	5.2	5.5		ns
t_{PLZ}			1.5	5.5	5.8		1.5	3.5	5.1	5.4		
t_{PHZ}	\overline{OE}	A	1.5	5.8	6.5		1.5	4	5.6	5.9		ns
t_{PLZ}			1.2	6.3	6.3		1.5	3.8	5.5	5.5		
$t_{sk(o)}$								0.5			ns	

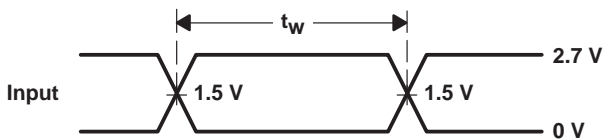
† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

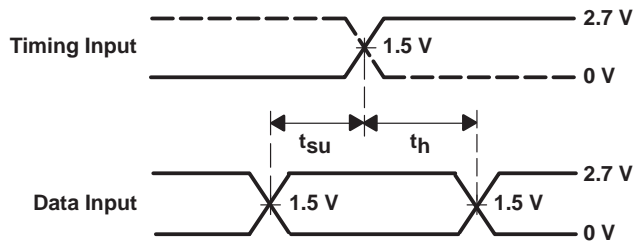


LOAD CIRCUIT

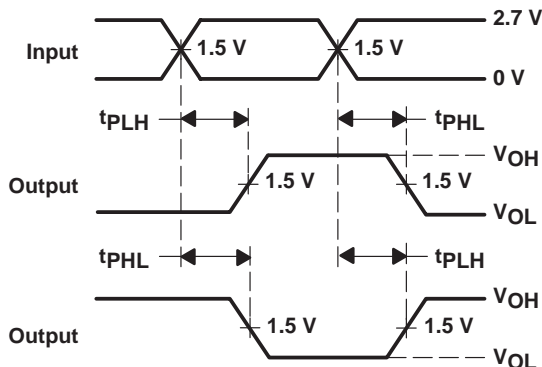
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



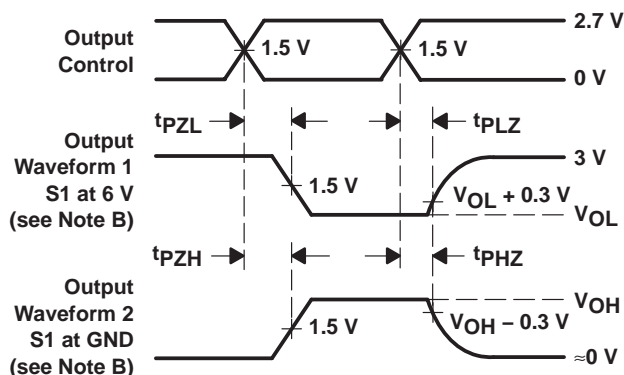
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVT162245ADGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVT162245ADL	ACTIVE	SSOP	DL	48	25	None	CU NIPDAU	Level-1-235C-UNLIM
SN74LVT162245ADLR	ACTIVE	SSOP	DL	48	1000	None	CU NIPDAU	Level-1-235C-UNLIM
SN74LVT162245AGQLR	ACTIVE	VFBGA	GQL	56	1000	None	SNPB	Level-1-240C-UNLIM
SN74LVT162245AZQLR	ACTIVE	VFBGA	ZQL	56	1000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

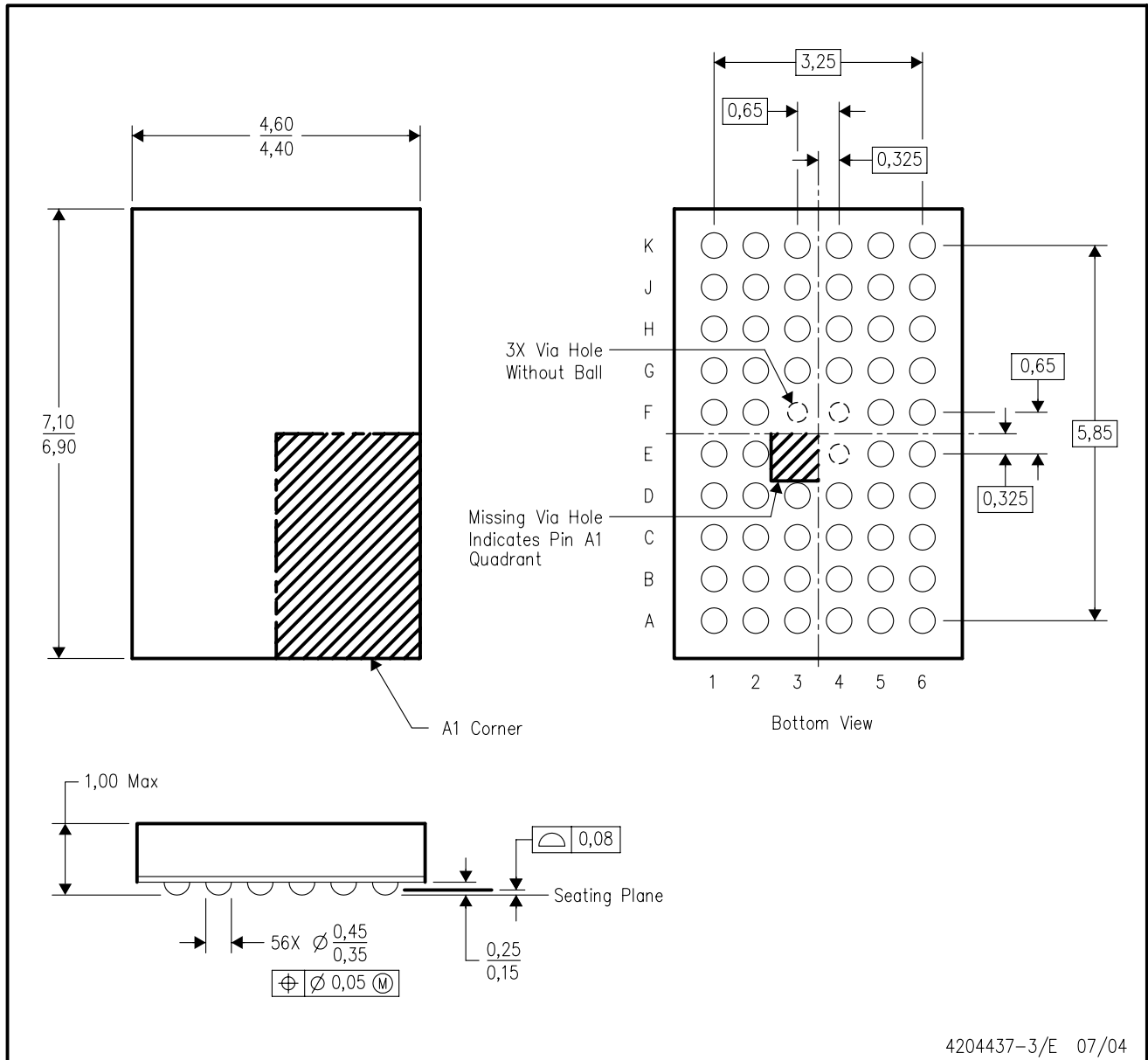
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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ZQL (R-PBGA-N56)

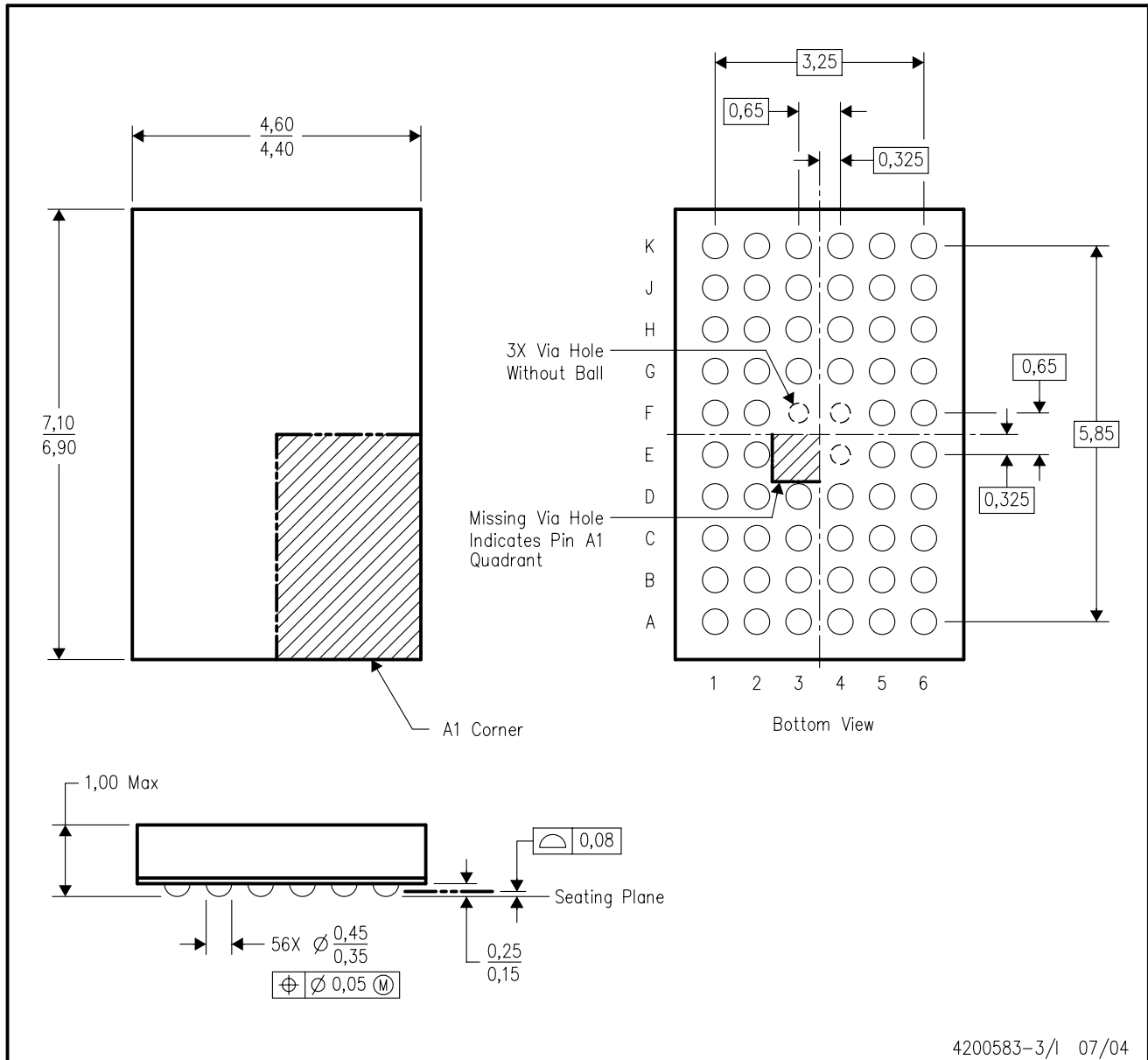
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265