

## FEATURES

- **Controlled Baseline**
    - One Assembly/Test Site, One Fabrication Site
  - **Extended Temperature Performance of –40°C to 85°C**
  - **Enhanced Diminishing Manufacturing Sources (DMS) Support**
  - **Enhanced Product-Change Notification**
  - **Qualification Pedigree <sup>(1)</sup>**
  - **Member of the Texas Instruments Widebus™ Family**
  - **1-to-2 Outputs Support Stacked DDR DIMMs**
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.
- **Supports SSTL\_2 Data Inputs**
  - **Outputs Meet SSTL\_2 Class II Specifications**
  - **Differential Clock (CLK and  $\overline{\text{CLK}}$ ) Inputs**
  - **Supports LVCMOS Switching Levels on the  $\overline{\text{RESET}}$  Input**
  - **$\overline{\text{RESET}}$  Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low**
  - **Pinout Optimizes DIMM PCB Layout**
  - **One Device Per DIMM Required**
  - **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
  - **ESD Protection Exceeds JESD 22**
    - **2000-V Human-Body Model (A114-A)**
    - **1000-V Charged-Device Model (C101)**

## DESCRIPTION/ORDERING INFORMATION

This 24-bit to 48-bit registered buffer is designed for 2.3-V to 2.7-V  $V_{CC}$  operation.

All inputs are SSTL\_2, except the LVCMOS reset ( $\overline{\text{RESET}}$ ) input. All outputs are SSTL\_2, Class II compatible.

The SN74SSTV32852 operates from a differential clock (CLK and  $\overline{\text{CLK}}$ ). Data are registered at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low.

The device supports low-power standby operation. When  $\overline{\text{RESET}}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ( $V_{REF}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are forced low. The LVCMOS  $\overline{\text{RESET}}$  input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LFBGA – GKF	Tape and reel	CSSTV32852GKFREP	SV852IEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

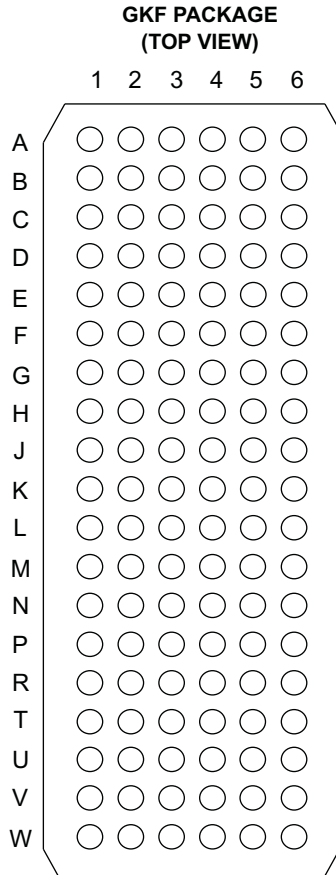
Widebus is a trademark of Texas Instruments.

# SN74SSTV32852-EP

## 24-BIT TO 48-BIT REGISTERED BUFFER

### WITH SSTL\_2 INPUTS AND OUTPUTS

SCES700–OCTOBER 2007



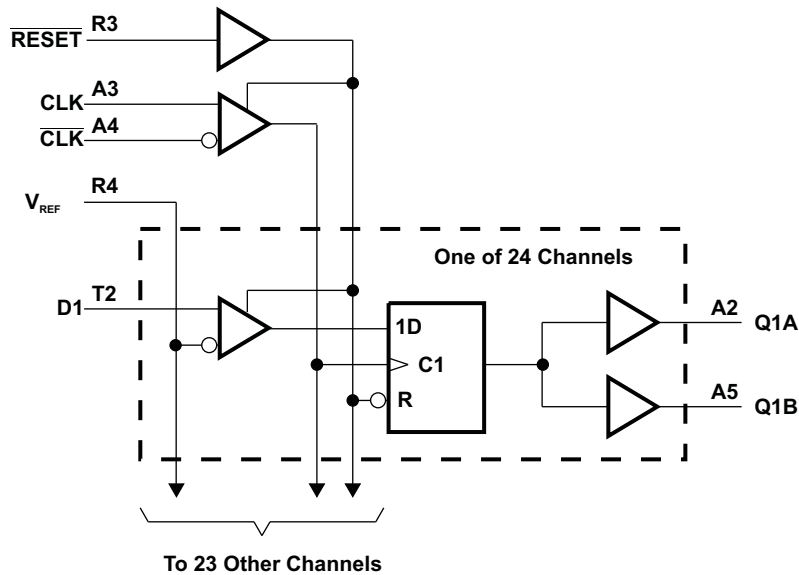
### Terminal Assignments

	1	2	3	4	5	6
<b>A</b>	Q2A	Q1A	CLK	$\overline{\text{CLK}}$	Q1B	Q2B
<b>B</b>	Q3A	V <sub>DDQ</sub>	GND	GND	V <sub>DDQ</sub>	Q3B
<b>C</b>	Q5A	Q4A	V <sub>DDQ</sub>	V <sub>DDQ</sub>	Q4B	Q5B
<b>D</b>	Q7A	Q6A	GND	GND	Q6B	Q7B
<b>E</b>	Q8A	GND	V <sub>DDQ</sub>	V <sub>DDQ</sub>	GND	Q8B
<b>F</b>	Q10A	Q9A	V <sub>DDQ</sub>	V <sub>DDQ</sub>	Q9B	Q10B
<b>G</b>	Q12A	Q11A	GND	GND	Q11B	Q12B
<b>H</b>	Q13A	V <sub>CC</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>CC</sub>	Q13B
<b>J</b>	Q14A	Q15A	GND	GND	Q15B	Q14B
<b>K</b>	Q17A	Q16A	V <sub>DDQ</sub>	V <sub>DDQ</sub>	Q16B	Q17B
<b>L</b>	Q18A	Q19A	GND	GND	Q19B	Q18B
<b>M</b>	Q20A	V <sub>DDQ</sub>	GND	GND	V <sub>DDQ</sub>	Q20B
<b>N</b>	Q22A	Q21A	V <sub>DDQ</sub>	V <sub>DDQ</sub>	Q21B	Q22B
<b>P</b>	Q23A	V <sub>DDQ</sub>	GND	GND	V <sub>DDQ</sub>	Q23B
<b>R</b>	Q24A	V <sub>CC</sub>	RESET	V <sub>REF</sub>	V <sub>CC</sub>	Q24B
<b>T</b>	D2	D1	D6	D18	D13	D14
<b>U</b>	D4	D3	D10	D22	D15	D16
<b>V</b>	D5	D7	D11	D23	D19	D17
<b>W</b>	D8	D9	D12	D24	D21	D20

### FUNCTION TABLE

RESET	INPUTS			OUTPUT Q
	CLK	$\overline{\text{CLK}}$	D	
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q <sub>0</sub>
L	X or floating	X or floating	X or floating	L

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT	
$V_{CC}$ or $V_{DDQ}$	Supply voltage range	-0.5 to 3.6	V	
$V_I$	Input voltage range <sup>(2)(3)</sup>	-0.5 to $V_{CC} + 0.5$	V	
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5 to $V_{DDQ} + 0.5$	V	
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{DDQ}$	±50	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{DDQ}$	±50	mA
	Continuous current through each $V_{CC}$ , $V_{DDQ}$ , or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	36	°C/W	
$T_{stg}$	Storage temperature range	-65 to 150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 3.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

# SN74SSTV32852-EP

## 24-BIT TO 48-BIT REGISTERED BUFFER WITH SSTL\_2 INPUTS AND OUTPUTS

SCES700–OCTOBER 2007

### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	NOM	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	V <sub>DDQ</sub>		2.7	V	
V <sub>DDQ</sub>	Output supply voltage	2.3		2.7	V	
V <sub>REF</sub>	Reference voltage (V <sub>REF</sub> = V <sub>DDQ</sub> /2)	1.15	1.25	1.35	V	
V <sub>TT</sub>	Termination voltage	V <sub>REF</sub> – 40 mV	V <sub>REF</sub>	V <sub>REF</sub> + 40 mV	V	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	V	
V <sub>IH</sub>	AC high-level input voltage	Data inputs		V <sub>REF</sub> + 310 mV	V	
V <sub>IL</sub>	AC low-level input voltage	Data inputs		V <sub>REF</sub> – 310 mV	V	
V <sub>IH</sub>	DC high-level input voltage	Data inputs		V <sub>REF</sub> + 150 mV	V	
V <sub>IL</sub>	DC low-level input voltage	Data inputs		V <sub>REF</sub> – 150 mV	V	
V <sub>IH</sub>	High-level input voltage	RESET		1.7	V	
V <sub>IL</sub>	Low-level input voltage	RESET		0.7	V	
V <sub>ICR</sub>	Common-mode input voltage range	CLK, CLK		0.97	1.53	V
V <sub>I(PP)</sub>	Peak-to-peak input voltage	CLK, CLK		360	mV	
I <sub>OH</sub>	High-level output current			-20	mA	
I <sub>OL</sub>	Low-level output current			20		
T <sub>A</sub>	Operating free-air temperature			-40	85	°C

- (1) The RESET input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless RESET is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>IK</sub>		I <sub>I</sub> = –18 mA	2.3 V			–1.2	V	
V <sub>OH</sub>		I <sub>OH</sub> = –100 μA	2.3 V to 2.7 V	V <sub>DDQ</sub> – 0.2			V	
		I <sub>OH</sub> = –16 mA	2.3 V	1.95				
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	2.3 V to 2.7 V			0.2	V	
		I <sub>OL</sub> = 16 mA	2.3 V			0.35		
I <sub>I</sub>	All inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	2.7 V			±5	μA	
I <sub>CC</sub>	Static standby	RESET = GND	2.7 V			10	μA	
	Static operating	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub>				35	mA	
I <sub>CCD</sub>	Dynamic operating – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching 50% duty cycle	2.7 V			46	μA/MHz	
	Dynamic operating – per each data input	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle				12	μA/clock MHz/D input	
r <sub>OH</sub>	Output high	I <sub>OH</sub> = –20 mA	2.3 V to 2.7 V	7			20	Ω
r <sub>OL</sub>	Output low	I <sub>OL</sub> = 20 mA	2.3 V to 2.7 V	7			20	Ω
C <sub>I</sub>	Data inputs	V <sub>I</sub> = V <sub>REF</sub> ± 310 mV	2.5 V	3	3.75	4.25	pF	
	CLK, CLK	V <sub>ICR</sub> = 1.25 V, V <sub>I(PP)</sub> = 360 mV		3	3.5	4		
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND		3.5	4.35	5		

- (1) All typical values are at V<sub>CC</sub> = 2.5 V, T<sub>A</sub> = 25°C.

## TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

			$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		UNIT
			MIN	MAX	
$f_{\text{clock}}$	Clock frequency		200		MHz
$t_w$	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low		2.5		ns
$t_{\text{act}}$	Differential inputs active time <sup>(1)</sup>		22		ns
$t_{\text{inact}}$	Differential inputs inactive time <sup>(2)</sup>		22		ns
$t_{\text{su}}$	Setup time	Fast slew rate <sup>(3)(4)</sup>	Data before CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$	0.75	ns
		Slow slew rate <sup>(5)(4)</sup>		0.9	
$t_h$	Hold time	Fast slew rate <sup>(3)(4)</sup>	Data after CLK $\uparrow$ , $\overline{\text{CLK}}\downarrow$	0.75	ns
		Slow slew rate <sup>(5)(4)</sup>		0.9	

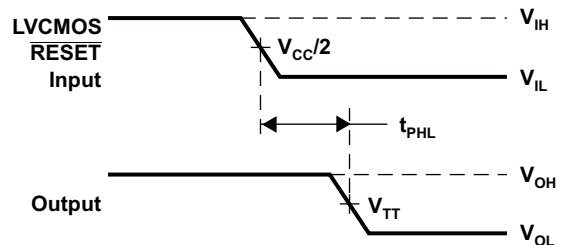
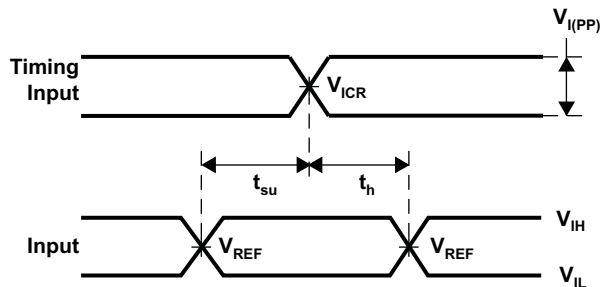
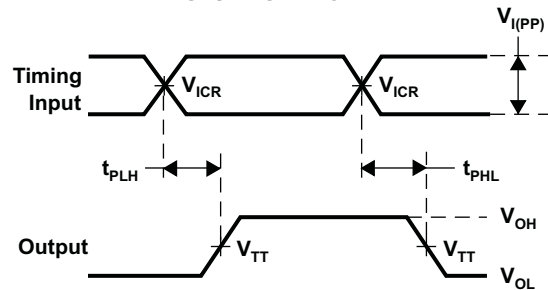
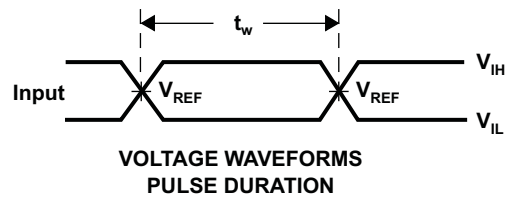
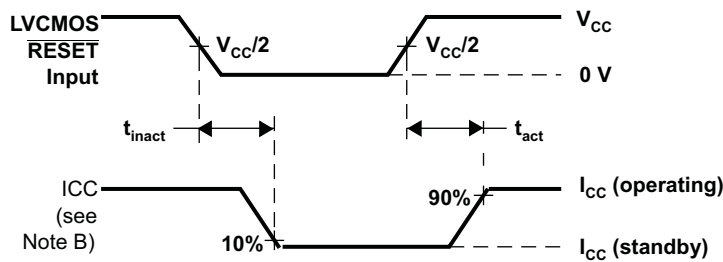
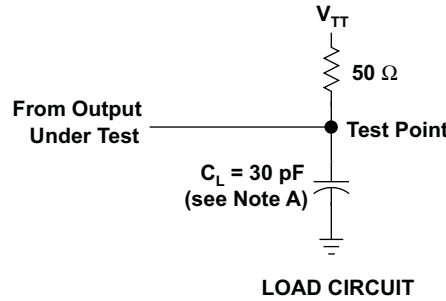
- (1)  $V_{\text{REF}}$  must be held at a valid input level, and data inputs must be held low for a minimum time of  $t_{\text{act}}$  max, after  $\overline{\text{RESET}}$  is taken high.  
 (2)  $V_{\text{REF}}$ , data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of  $t_{\text{inact}}$  max, after  $\overline{\text{RESET}}$  is taken low.  
 (3) Data signal input slew rate  $\geq 1\text{ V/ns}$   
 (4) CLK,  $\overline{\text{CLK}}$  input slew rates are  $\geq 1\text{ V/ns}$ .  
 (5) Data signal input slew rate  $\geq 0.5\text{ V/ns}$  and  $< 1\text{ V/ns}$

## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		UNIT
			MIN	MAX	
$f_{\text{max}}$			200		MHz
$t_{\text{pd}}$	CLK and $\overline{\text{CLK}}$	Q	1.1	3.1	ns
$t_{\text{PHL}}$	$\overline{\text{RESET}}$	Q	5		ns

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B.  $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0$  mA.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10$  MHz,  $Z_O = 50 \Omega$ , Input slew rate = 1 V/ns  $\pm 20\%$  (unless otherwise noted).  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $V_{TT} = V_{REF} = V_{DDQ}/2$   
F.  $V_{IH} = V_{REF} + 310$  mV (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVC MOS input.  
G.  $V_{IL} = V_{REF} - 310$  mV (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.  
H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSSTV32852GKFREP	BGA MICROSTAR	GKF	114	1000	330.0	24.4	5.8	16.3	1.8	8.0	24.0	Q1

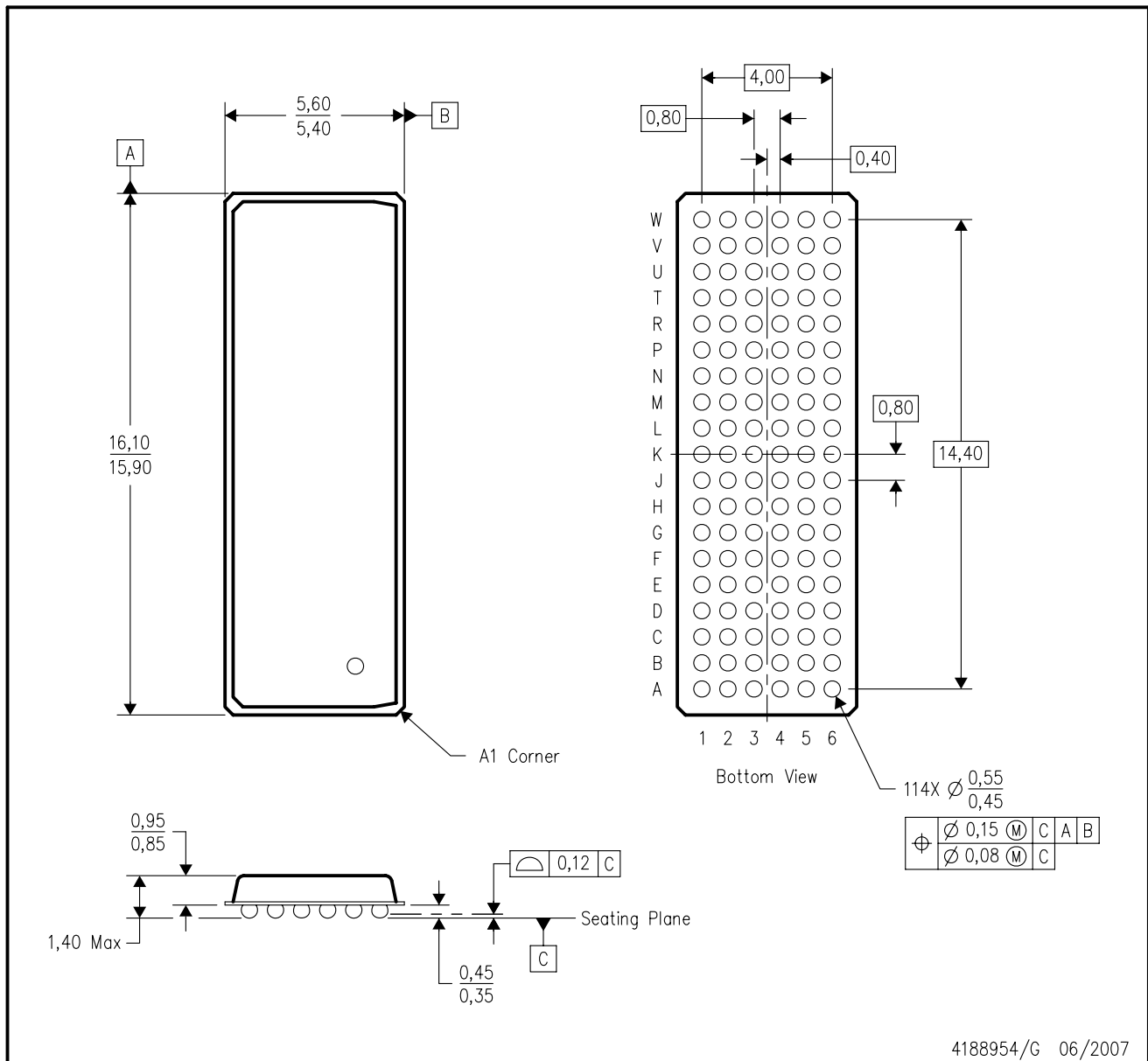
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSSTV32852GKFREP	BGA MICROSTAR	GKF	114	1000	346.0	346.0	41.0

GKF (R-PBGA-N114)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation DC.
  - D. This package is tin-lead (SnPb). Refer to the 114 ZKF package (drawing 4204494) for lead-free.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2009, Texas Instruments Incorporated