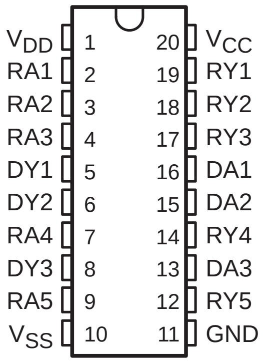
SN75185
MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS181C − DECEMBER 1994 − REVISED OCTOBER 2003

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT™ and Compatibles**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Supports Data Rates Up To 120 kbit/s**
- **ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 3.5 kV on All Other Pins (Human-Body Model)**
- **Pin-to-Pin Compatible With the SN75C185**

DB, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The SN75185 combines three drivers and five receivers from the TI SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The SN75185 complies with the requirements of the TIA/EIA-232-F and ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU v.10) and TIA/EIA-422-B (ITU v.11) standards is recommended.

The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 20	SN75185N	SN75185N
	SOIC (DW)	Tube of 25	SN75185DW	SN75185
		Reel of 2000	SN75185DWR	
	SSOP (DB)	Tube of 70	SN75185DB	A185
		Reel of 2000	SN75185DBR	

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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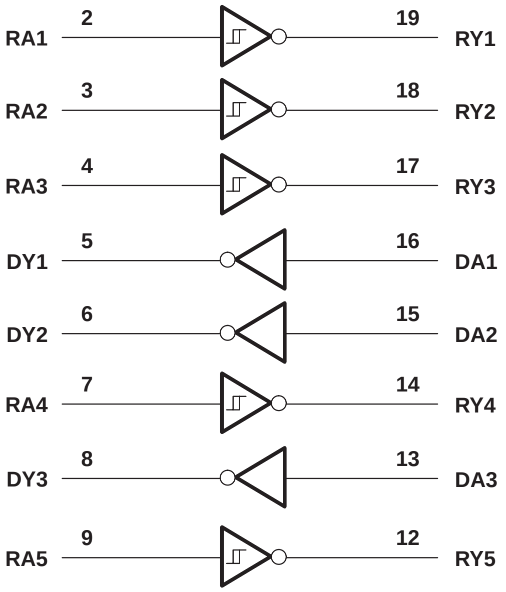
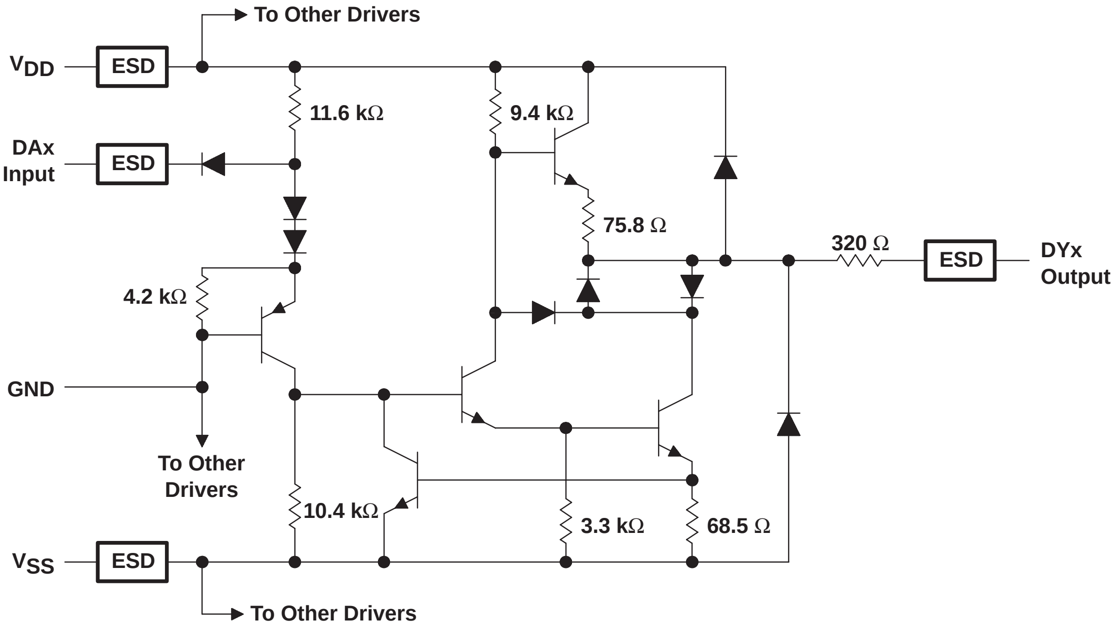
logic diagram (positive logic)

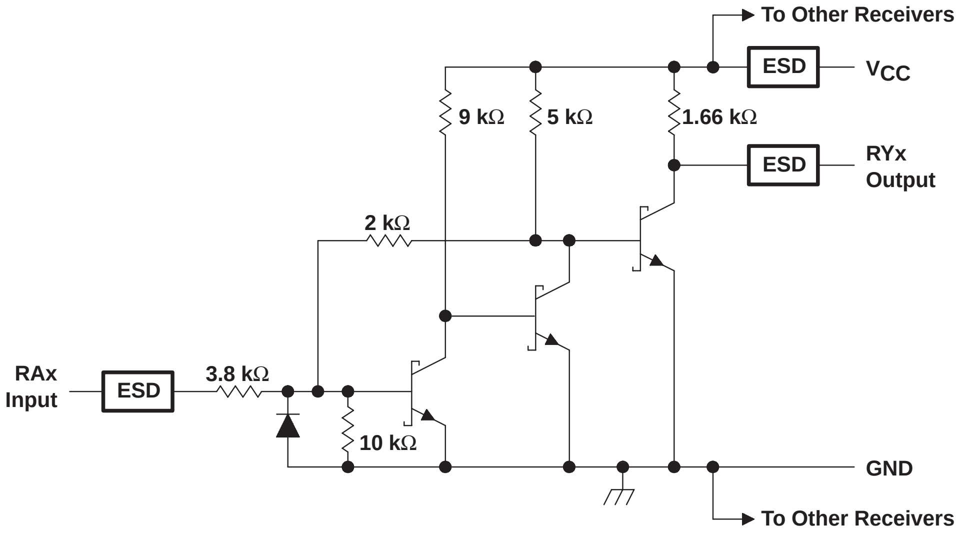


schematic of drivers



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1):	V_{CC}	10 V
	V_{DD}	15 V
	V_{SS}	−15 V
Input voltage range:	Driver	−15 V to 7 V
	Receiver	−30 V to 30 V
Driver output voltage range		−15 V to 15 V
Receiver low-level output current		20 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3):	DB package	70°C/W
	DW package	58°C/W
	N package	69°C/W
Operating virtual junction temperature, T_J		150°C
Electrostatic discharge: Human-Body Model:	RS-232 pins, class 3, A (see Note 4)	10 kV
	All pins, class 3, A (see Note 5)	3.5 kV
Machine Model:	RS-232 pins, class 3, B (see Note 6)	600 V
	All pins, class 3, B (see Note 4)	250 V
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. RS-232 pins are tested with respect to ground and to each other.
5. Per MIL-PRF-38535
6. RS-232 pins are tested with respect to ground.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{DD}	Supply voltage		7.5	9	15	V
V_{SS}	Supply voltage		−7.5	−9	−15	V
V_{IH}	High-level input voltage (drivers only)		1.9			V
V_{IL}	Low-level input voltage (drivers only)				0.8	V
I_{OH}	High-level output current	Drivers			−6	mA
		Receivers			−0.5	
I_{OL}	Low-level output current	Drivers			6	mA
		Receivers			16	
T_A	Operating free-air temperature		0		70	°C

supply currents

PARAMETER		TEST CONDITIONS				MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	All inputs at 5 V,	No load,	V_{CC} = 5 V			30	mA
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		15	mA
				V_{DD} = 12 V,	V_{SS} = −12 V		19	
				V_{DD} = 15 V,	V_{SS} = −15 V		25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		4.5	
				V_{DD} = 12 V,	V_{SS} = −12 V		5.5	
				V_{DD} = 15 V,	V_{SS} = −15 V		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		−15	mA
				V_{DD} = 12 V,	V_{SS} = −12 V		−19	
				V_{DD} = 15 V,	V_{SS} = −15 V		−25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		−3.2	
				V_{DD} = 12 V,	V_{SS} = −12 V		−3.2	
				V_{DD} = 15 V,	V_{SS} = −15 V		−3.2	

DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 9 V, V_{SS} = −9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 7)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		−7.5	−6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	µA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 8)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	−4.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	12	19.5	mA
r_o	Output resistance (see Note 9)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = −2 V to 2 V	300			Ω

NOTES: 7. The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if −10 V is maximum, the typical value is a more negative voltage).
8. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
9. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF		75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF		60	100	ns
			C_L = 2500 pF, See Note 10		1.7	2.5	µs
t_{THL}	Transition time, high- to low-level output	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF		40	75	ns
			C_L = 2500 pF, See Note 11		1.5	2.5	µs

NOTES: 10. Measured between −3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.
11. Measured between 3-V and −3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70 °C	1.55		2.3	
V_{T-}	Negative-going threshold voltage			0.75	0.97	1.25	
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5			
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level input voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level output current	V_I = −25 V,	See Figure 5	−3.6		−8.3	mA
		V_I = −3 V,	See Figure 5	−0.43			
I_{OS}	Short-circuit output current	See Figure 4			−3.4	−12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = −9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ		107	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ		42	150	ns
t_{TLH}	Transition time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ		175	525	ns
t_{THL}	Transition time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ		16	60	ns

PARAMETER MEASUREMENT INFORMATION

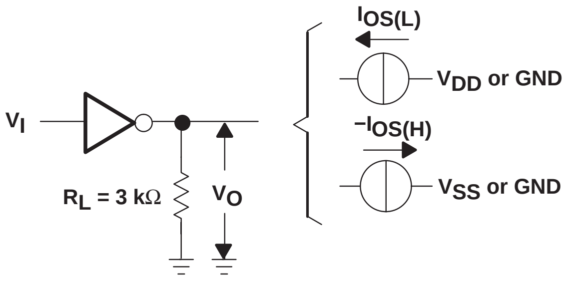


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

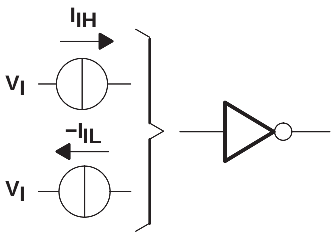
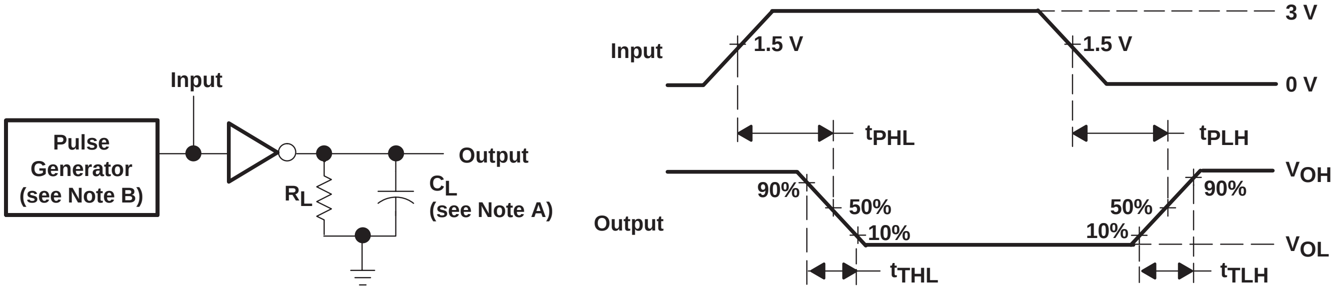


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

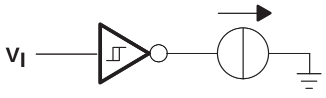


Figure 4. Receiver Test Circuit for I_{OS}

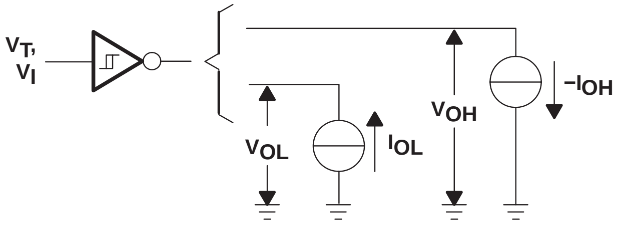
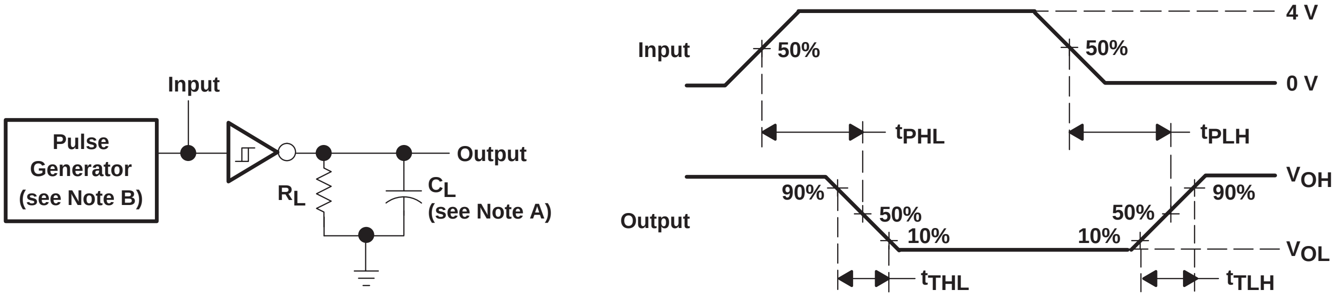


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

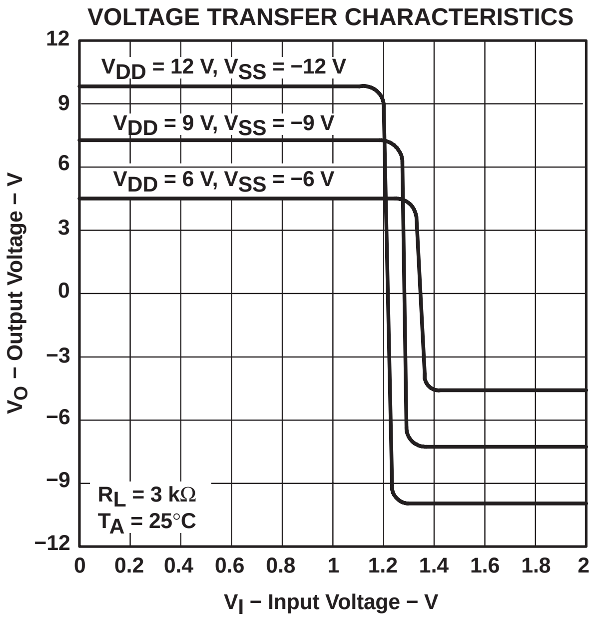

VOLTAGE TRANSFER CHARACTERISTICS

Figure 7

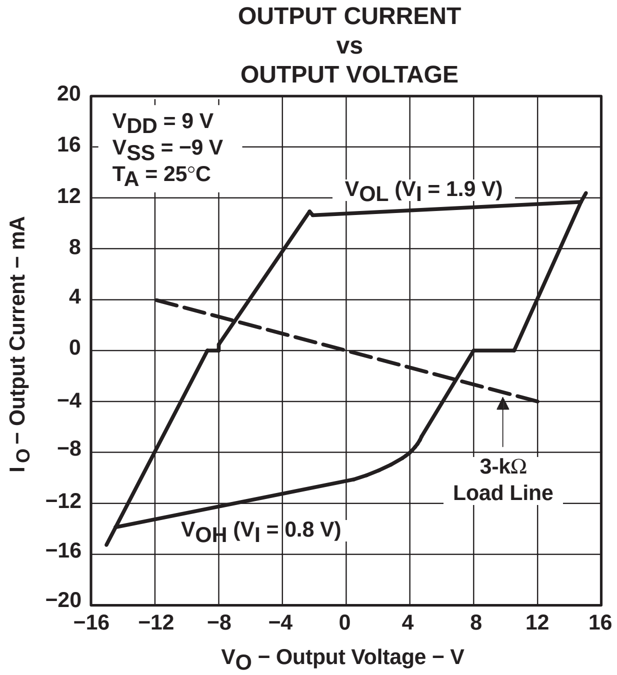

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

Figure 8

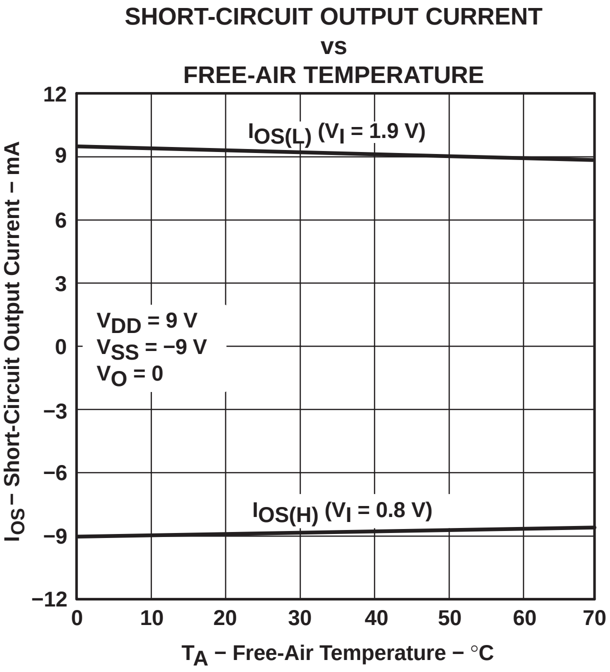

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 9

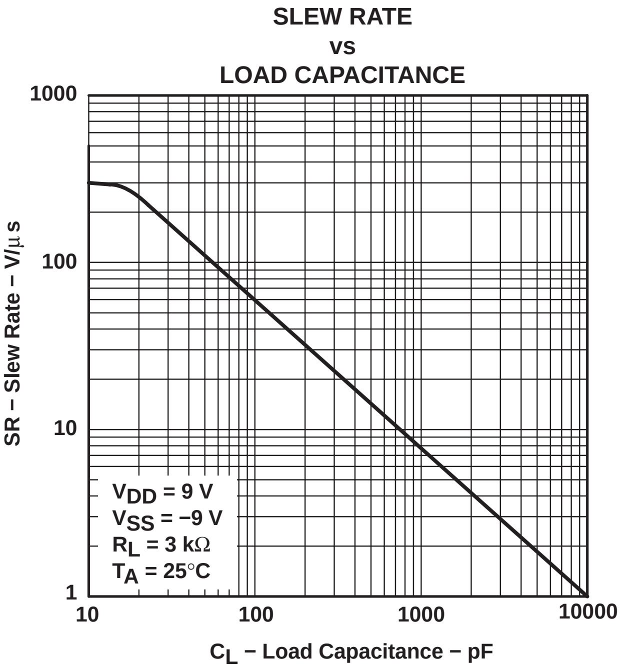
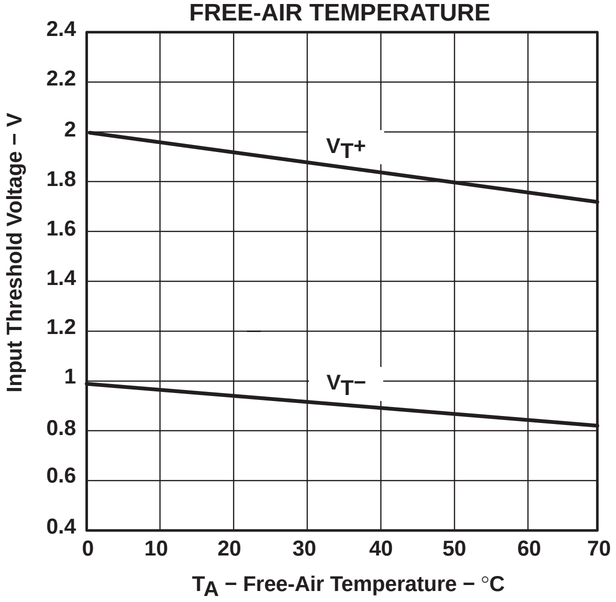

SLEW RATE
vs
LOAD CAPACITANCE

Figure 10

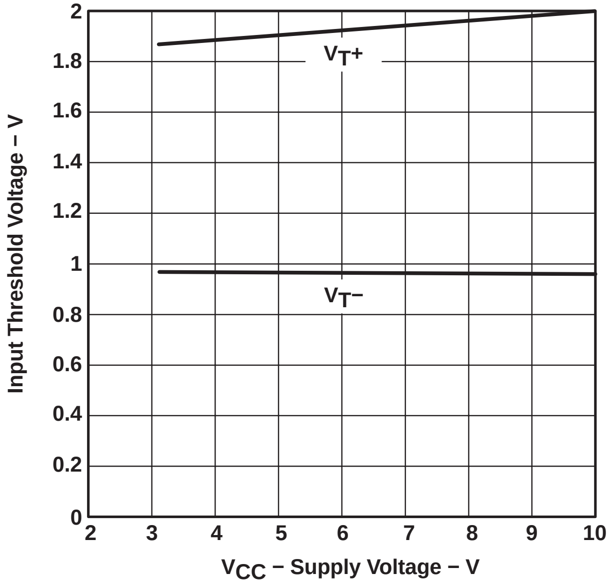
TYPICAL CHARACTERISTICS

RECEIVER SECTION



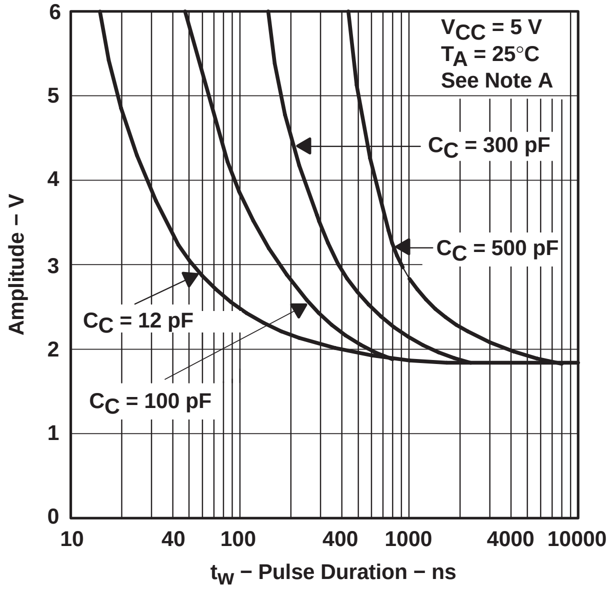
INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 11



INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

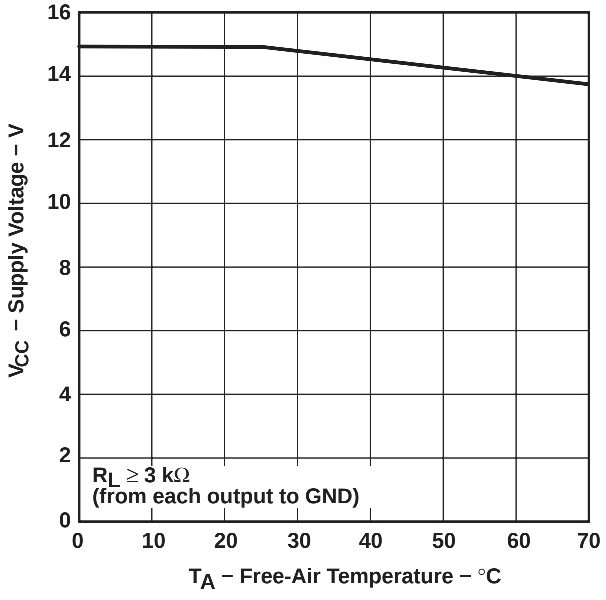
Figure 12



NOISE REJECTION

NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13



MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75185 in the fault condition. In the fault condition, the device outputs are shorted to ±15 V, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

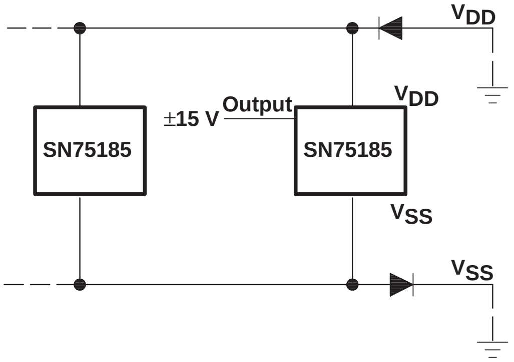
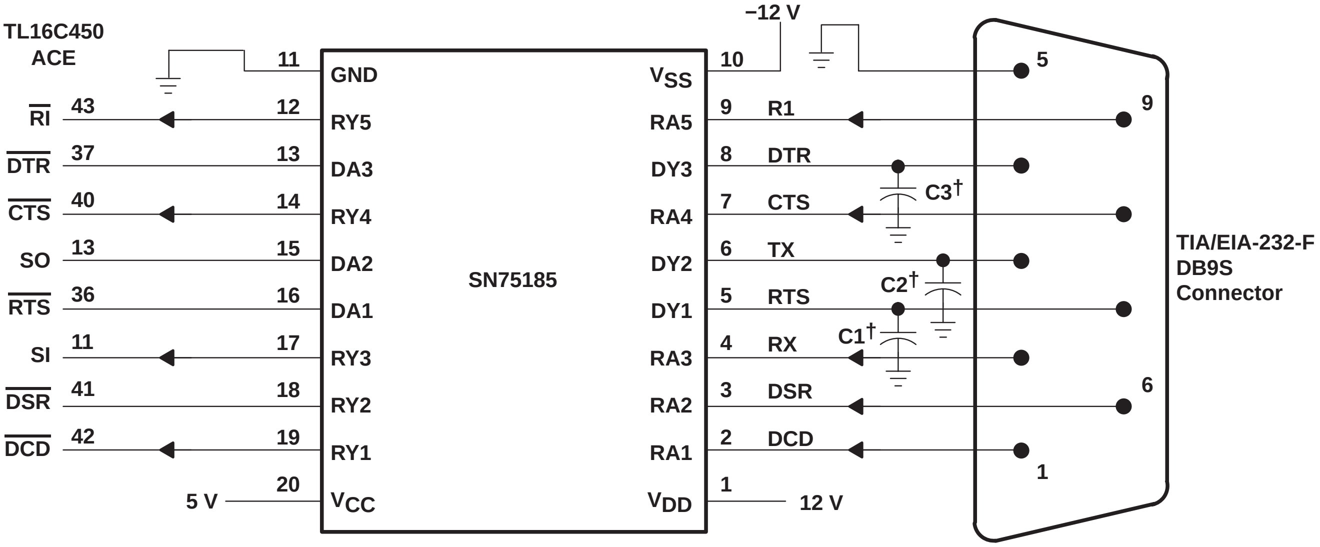


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which are required to meet the RS-232 maximum slew-rate requirement of 30 V/μs. The value of the loading capacitors required depends on the line length and desired slew rate, but typically is 330 pF.

Figure 16. Typical Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75185DB	ACTIVE	SSOP	DB	20	70	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75185DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN75185DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN75185DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN75185N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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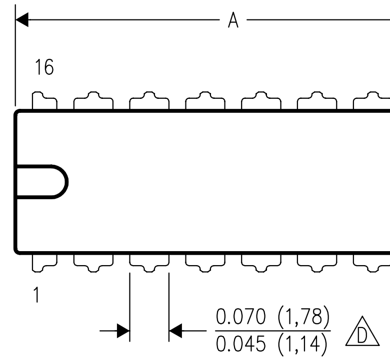
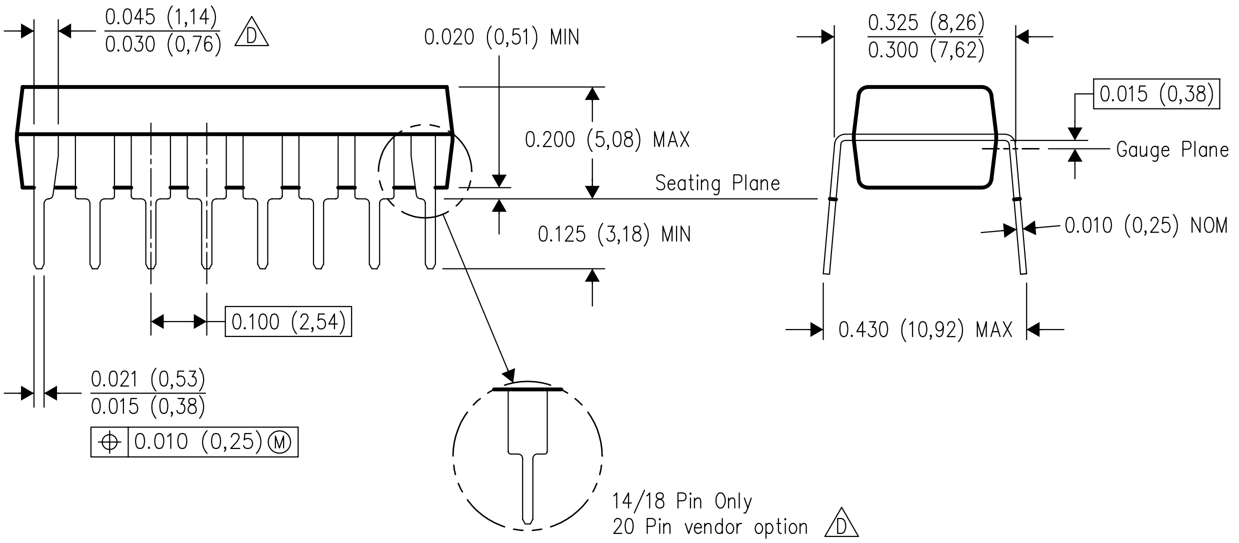
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



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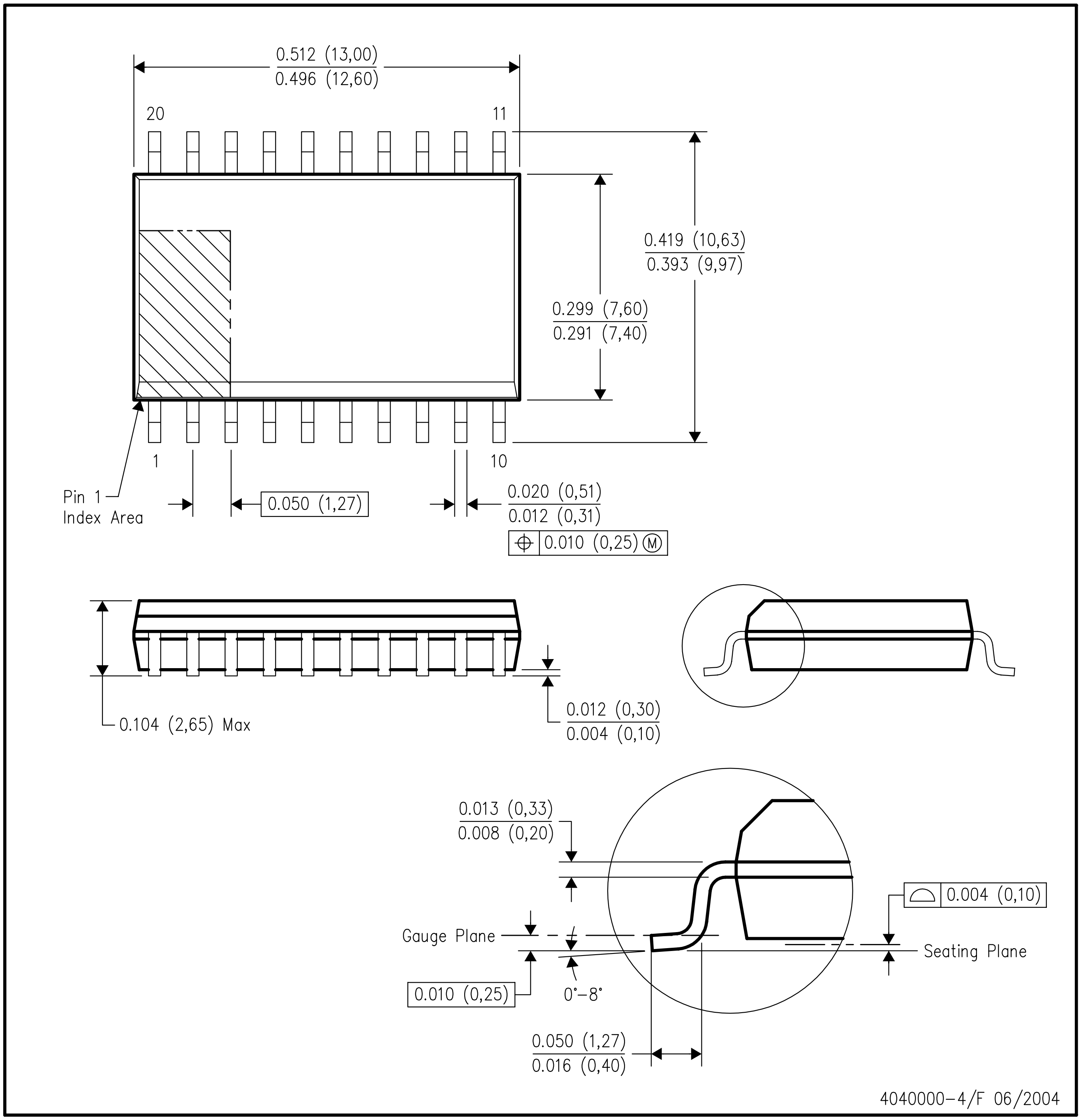
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

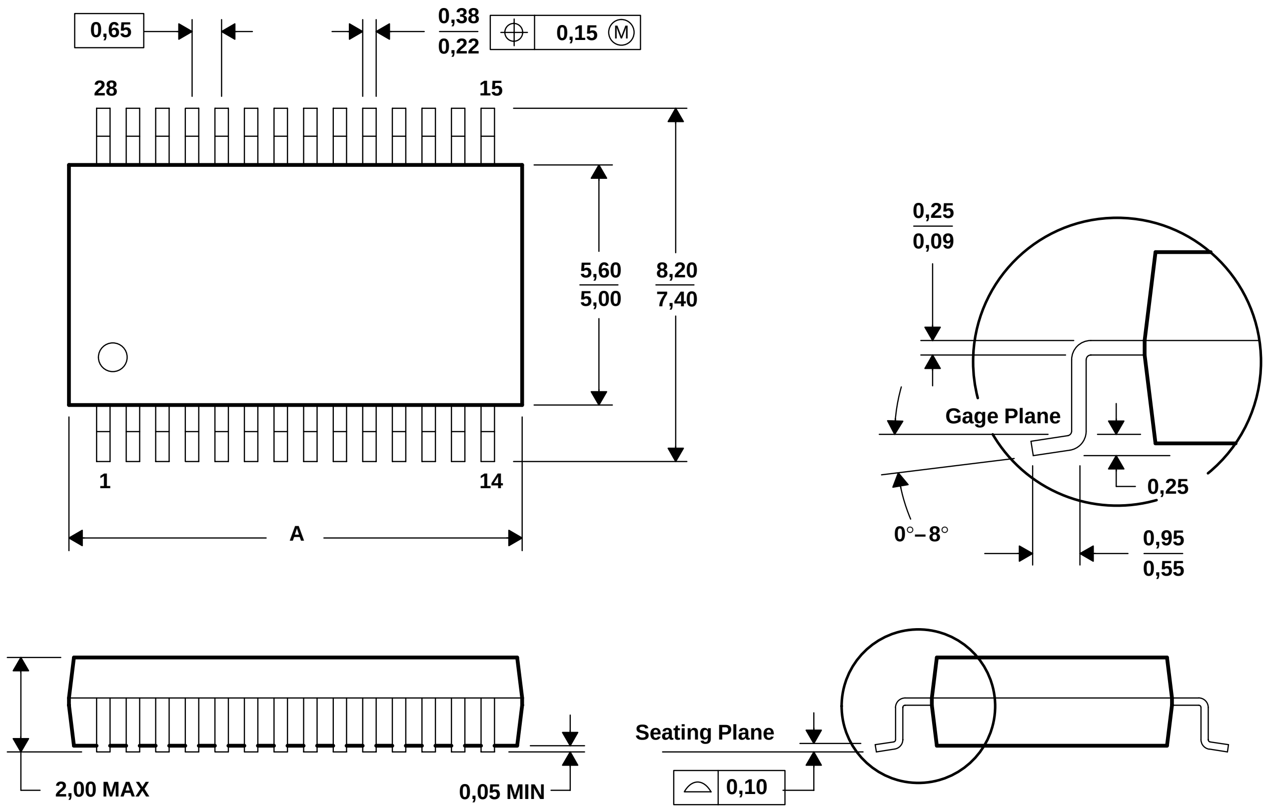
DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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