

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL082Y, TL084, TL084A, TL084B, TL084Y JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

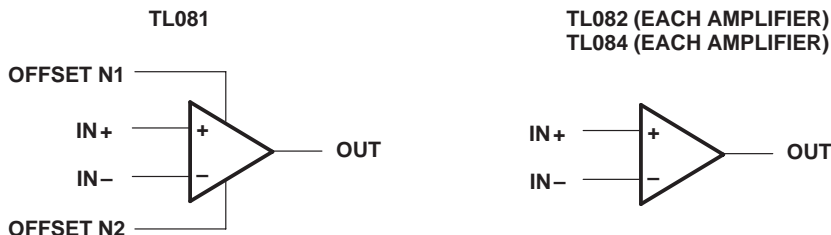
- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET-Input Stage
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ μ s Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

symbols



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

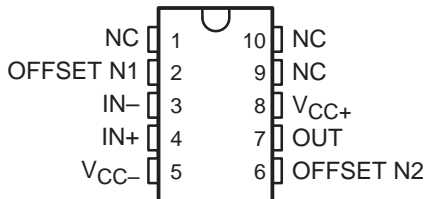
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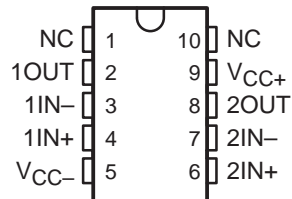
TL081, TL081A, TL081B, TL082, TL082A, TL082B TL082Y, TL084, TL084A, TL084B, TL084Y JFET-INPUT OPERATIONAL AMPLIFIERS

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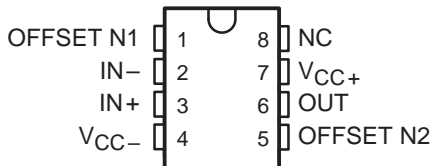
**TL081M
U PACKAGE
(TOP VIEW)**



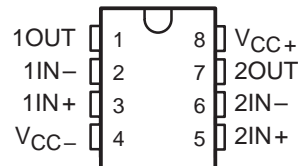
**TL082M
U PACKAGE
(TOP VIEW)**



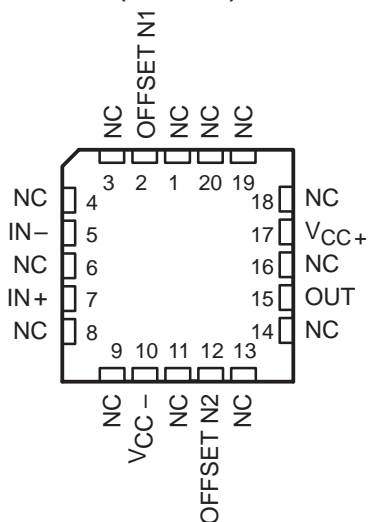
**TL081, TL081A, TL081B
D, JG, P, OR PW PACKAGE
(TOP VIEW)**



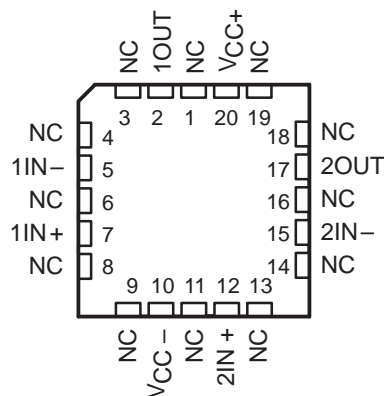
**TL082, TL082A, TL082B
D, JG, P, OR PW PACKAGE
(TOP VIEW)**



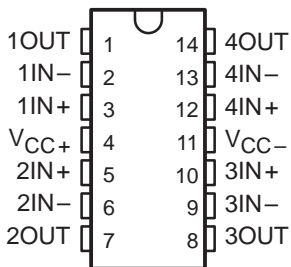
**TL081M . . . FK PACKAGE
(TOP VIEW)**



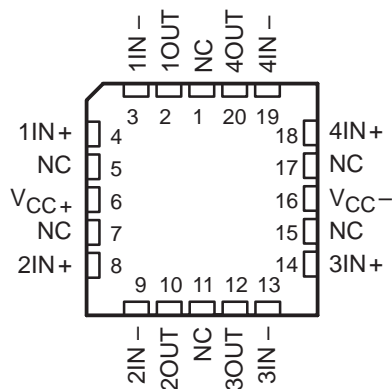
**TL082M . . . FK PACKAGE
(TOP VIEW)**



**TL084, TL084A, TL084B
D, J, N, PW, OR W PACKAGE
(TOP VIEW)**



**TL084M . . . FK PACKAGE
(TOP VIEW)**



NC – No internal connection

AVAILABLE OPTIONS

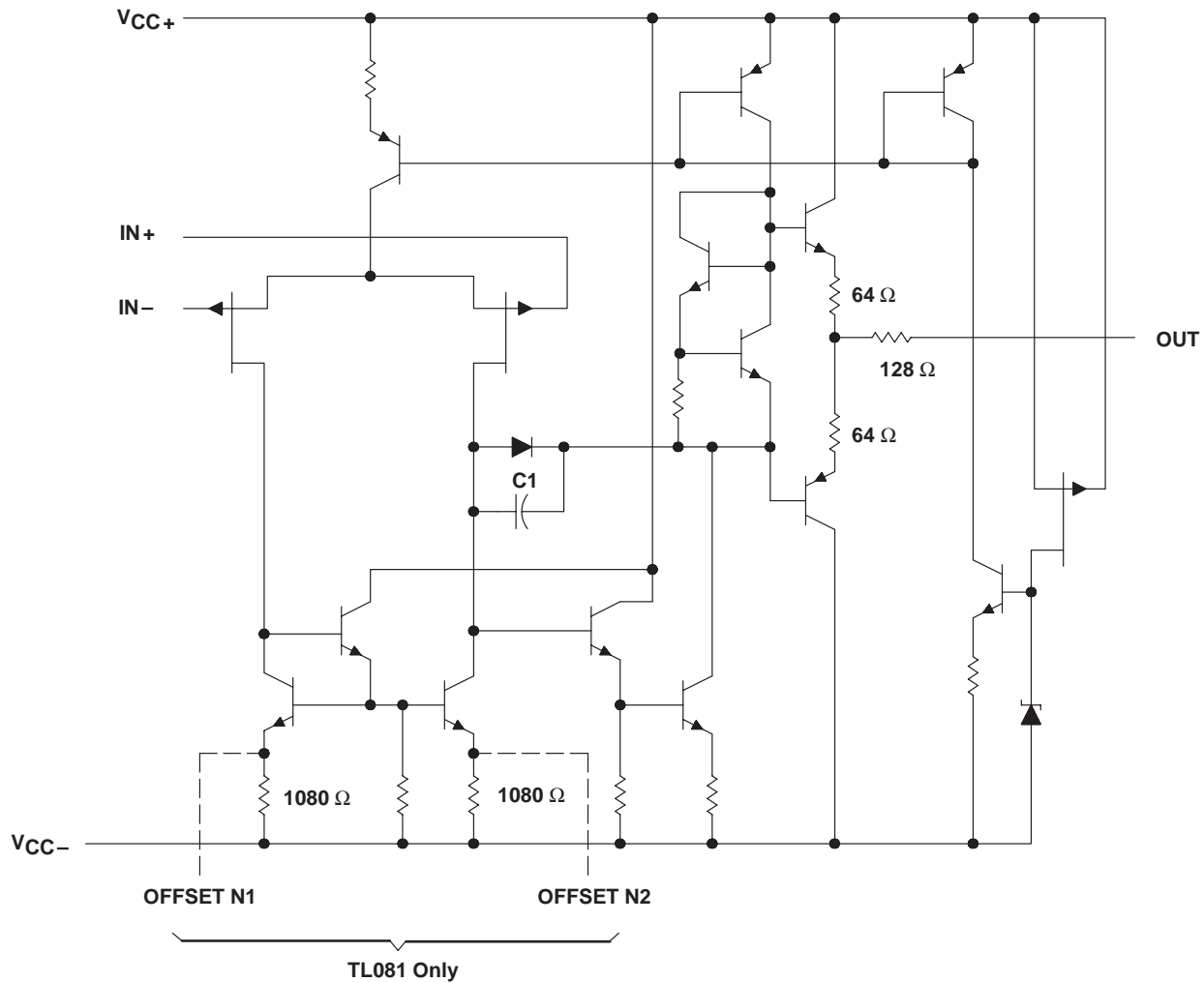
T _A	V _{IOMax} AT 25°C	PACKAGED DEVICES										CHIP FORM (Y)	
		SMALL OUTLINE (D008)	SMALL OUTLINE (D014)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	FLAT PACK (W)		
0°C to 70°C	15 mV 6 mV 3 mV	TL081CD TL081ACD TL081BCD	—	—	—	—	—	—	TL081CP TL081ACP TL081BCP	TL081CPW	—	—	—
	15 mV 6 mV 3 mV	TL082CD TL082ACD TL082BCD	—	—	—	—	—	—	TL082CP TL082ACP TL082BCP	TL082CPW	—	—	TL082Y
	15 mV 6 mV 3 mV	—	TL084CD TL084ACD TL084BCD	—	—	—	—	TL084CN TL084ACN TL084BCN	—	TL084CPW	—	—	TL084Y
-40°C to 85°C	6 mV 6 mV 6 mV	TL081ID TL082ID TL084ID	—	—	—	—	—	—	TL081IP TL082IP	—	—	—	—
-40°C to 125°C	9 mV	—	TL084QD	—	—	—	—	—	—	—	—	—	—
-55°C to 125°C	6 mV 6 mV 9 mV	—	—	TL081MFK TL082MFK TL084MFK	—	TL081MJG TL082MJG	—	—	—	—	TL081MU TL082MU	—	—
					TL084MJ							TL084MW	

The D package is available taped and reeled. Add R suffix to the device type (e.g., TL081CDR).

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
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TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
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schematic (each amplifier)



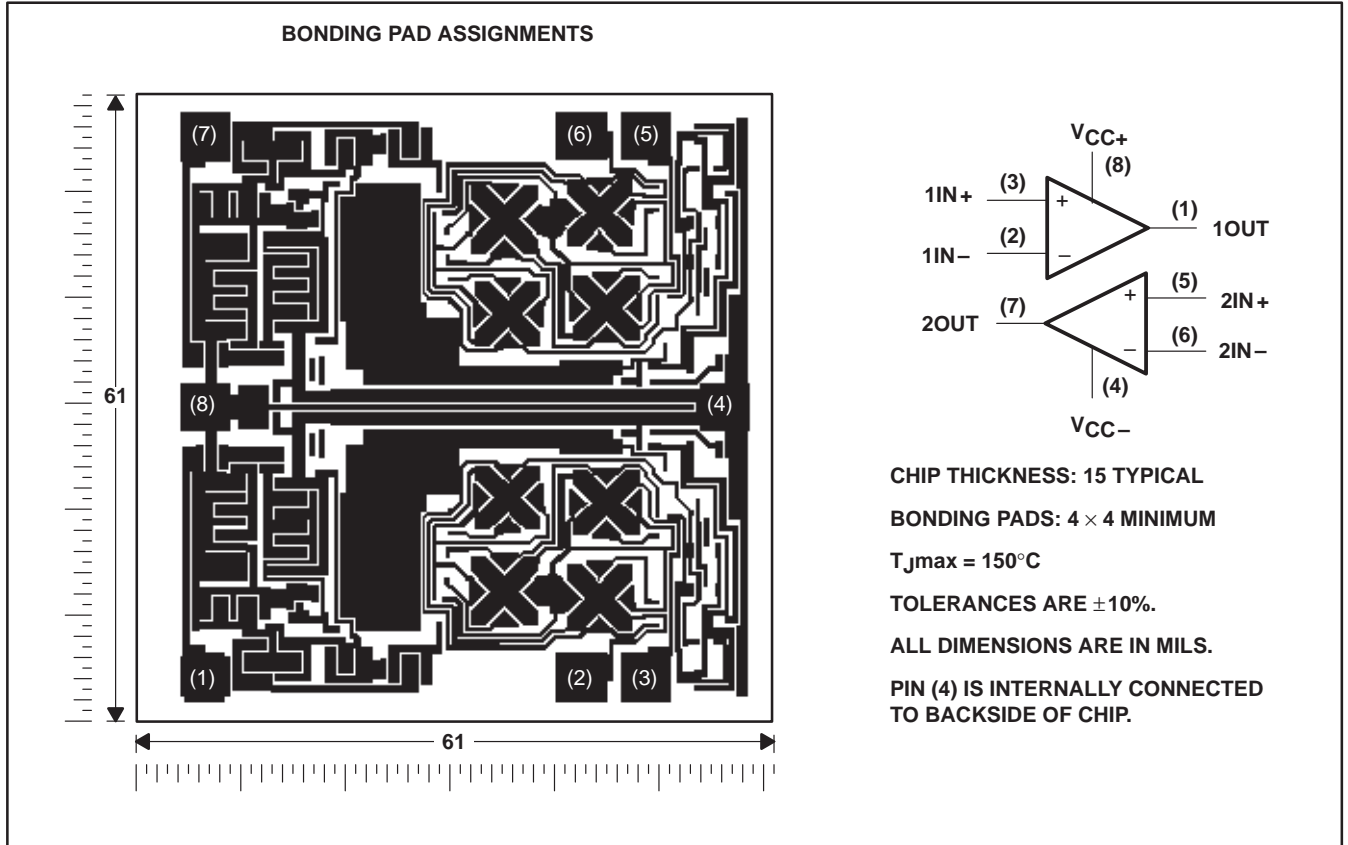
Component values shown are nominal.

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

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TL082Y chip information

These chips, when properly assembled, display characteristics similar to the TL082. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

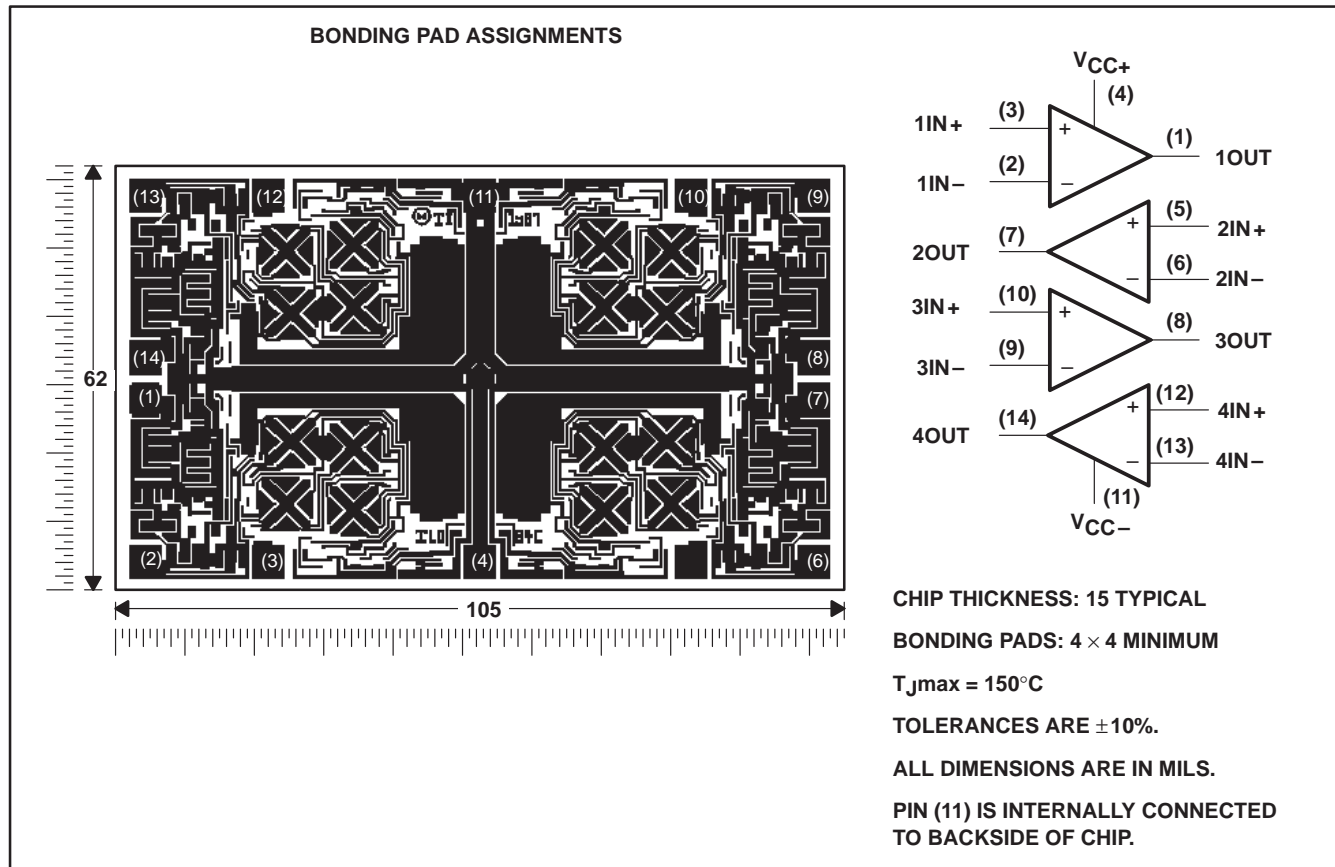


**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS**

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TL084Y chip information

These chips, when properly assembled, display characteristics similar to the TL084. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)	18	18	18	18	V
Supply voltage V_{CC-} (see Note 1)	-18	-18	-18	-18	V
Differential input voltage, V_{ID} (see Note 2)	± 30	± 30	± 30	± 30	V
Input voltage, V_I (see Notes 1 and 3)	± 15	± 15	± 15	± 15	V
Duration of output short circuit (see Note 4)	unlimited	unlimited	unlimited	unlimited	
Continuous total power dissipation	See Dissipation Rating Table				
Operating free-air temperature range, T_A	0 to 70	-40 to 85	-40 to 125	-55 to 125	°C
Storage temperature range, T_{stg}	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds, T_C	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, P, or PW package	260	260	260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8 pin)	680 mW	5.8 mW/°C	32°C	460 mW	373 mW	N/A
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	597 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
PW (8 pin)	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
PW (14 pin)	700 mW	5.6 mW/°C	25°C	448 mW	N/A	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW



electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	25°C	3	15		3	6		2	3		3	6	mV	
		Full range		20			7.5			5			9		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	Full range		18			18			18			18	$\mu\text{V}/^\circ\text{C}$	
I_{IO} Input offset current‡	$V_O = 0$	25°C	5	200		5	100		5	100		5	100	pA	
		Full range		2			2			2			10	nA	
I_{IB} Input bias current‡	$V_O = 0$	25°C	30	400		30	200		30	200		30	200	pA	
		Full range		10			7			7			20	nA	
V_{ICR} Common-mode input voltage range		25°C	± 11	-12 to 15		± 11	-12 to 15		± 11	-12 to 15		± 11	-12 to 15	V	
V_{OM} Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	± 12	± 13.5		± 12	± 13.5		± 12	± 13.5		± 12	± 13.5	V	
	$R_L \geq 10\ \text{k}\Omega$	Full range	± 12			± 12			± 12			± 12			
	$R_L \geq 2\ \text{k}\Omega$		± 10	± 12		± 10	± 12		± 10	± 12		± 10	± 12		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$, $R_L \geq 2\ \text{k}\Omega$	25°C	25	200		50	200		50	200		50	200	V/mV	
	$V_O = \pm 10\ \text{V}$, $R_L \geq 2\ \text{k}\Omega$	Full range	15			25			25			25			
B_1 Unity-gain bandwidth		25°C		3			3			3			3	MHz	
r_i Input resistance		25°C		10^{12}			10^{12}			10^{12}			10^{12}	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	86		75	86		75	86		75	86	dB	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC} = \pm 15\ \text{V}$ to $\pm 9\ \text{V}$, $V_O = 0$, $R_S = 50\ \Omega$	25°C	70	86		80	86		80	86		80	86	dB	
I_{CC} Supply current (per amplifier)	$V_O = 0$, No load	25°C		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120			120			120	dB	

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and -40°C to 85°C for TL08_I.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS**

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electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITION [†]	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C	3	6		3	9	mV	
		Full range			9		15		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range	18			18			$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current [‡]	$V_O = 0$	25°C	5	100		5	100	pA	
		125°C	20			20			nA
I_{IB} Input bias current [‡]	$V_O = 0$	25°C	30	200		30	200	pA	
		125°C	50			50			nA
V_{ICR} Common-mode input voltage range		25°C	± 11	± 12 to ± 15		± 11	± 12 to ± 15	V	
V_{OM} Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	± 12	± 13.5		± 12	± 13.5	V	
	$R_L \geq 10\ \text{k}\Omega$	Full range	± 12		± 12				
	$R_L \geq 2\ \text{k}\Omega$		± 10	± 12	± 10	± 12			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	25	200		25	200	V/mV	
	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	Full range	15		15				
B_1 Unity-gain bandwidth		25°C	3			3			MHz
r_i Input resistance		25°C	10^{12}			10^{12}			Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86	dB	
k_{SVR} Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15\ \text{V to } \pm 9\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86	dB	
I_{CC} Supply current (per amplifier)	$V_O = 0, \text{ No load}$	25°C	1.4	2.8		1.4	2.8	mA	
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$	25°C	120			120			dB

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

[‡] Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm} = \pm 15\ \text{V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SR Slew rate at unity gain	$V_I = 10\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, \text{ See Figure 1}$	8*	13		V/ μs	
	$V_I = 10\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, T_A = -55^\circ\text{C to } 125^\circ\text{C}, \text{ See Figure 1}$	5*				
t_r Rise time	$V_I = 20\ \text{mV}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, \text{ See Figure 1}$	0.05			μs	
Overshoot factor		20%				
V_n Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 1\ \text{kHz}$			18	nV/ $\sqrt{\text{Hz}}$
		$f = 10\ \text{Hz to } 10\ \text{kHz}$			4	μV
I_n Equivalent input noise current	$R_S = 20\ \Omega, f = 1\ \text{kHz}$	0.01			pA/ $\sqrt{\text{Hz}}$	
THD Total harmonic distortion	$V_{I\text{rms}} = 6\ \text{V}, f = 1\ \text{kHz}$	$A_{VD} = 1,$	$R_S \leq 1\ \text{k}\Omega,$	$R_L \geq 2\ \text{k}\Omega,$	0.003%	

*On products compliant to MIL-PRF-38535, this parameter is not production tested.



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TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS**

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electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	TL082Y, TL084Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$		3	15	mV
αV_{IO} Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$		18		$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current‡	$V_O = 0$,		5	200	pA
I_{IB} Input bias current‡	$V_O = 0$,		30	400	pA
V_{ICR} Common-mode input voltage range		± 11	-12 to 15		V
V_{OM} Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$,	± 12	± 13.5		V
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$, $R_L \geq 2\ \text{k}\Omega$	25	200		V/mV
B_1 Unity-gain bandwidth			3		MHz
r_i Input resistance			10^{12}		Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$, $V_O = 0$, $R_S = 50\ \Omega$	70 70	86 86		dB
kSVR Supply voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)	$V_{CC} = \pm 15\ \text{V}$ to $\pm 9\ \text{V}$, $V_O = 0$, $R_S = 50\ \Omega$	70 70	86 86		dB
I_{CC} Supply current (per amplifier)	$V_O = 0$, No load		1.4	2.8	mA
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$		120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15\ \text{V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10\ \text{V}$,	$R_L = 2\ \text{k}\Omega$,	$C_L = 100\ \text{pF}$, See Figure 1	8	13		$\text{V}/\mu\text{s}$
t_r Rise time	$V_I = 20\ \text{mV}$,	$R_L = 2\ \text{k}\Omega$,	$C_L = 100\ \text{pF}$, See Figure 1		0.05		μs
Overshoot factor					20%		
V_n Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 1 kHz			18		$\text{nV}/\sqrt{\text{Hz}}$
		f = 10 Hz to 10 kHz			4		μV
I_n Equivalent input noise current	$R_S = 20\ \Omega$,	f = 1 kHz			0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{I\text{rms}} = 6\ \text{V}$, f = 1 kHz	$A_{VD} = 1$,	$R_S \leq 1\ \text{k}\Omega$, $R_L \geq 2\ \text{k}\Omega$,		0.003%		



PARAMETER MEASUREMENT INFORMATION

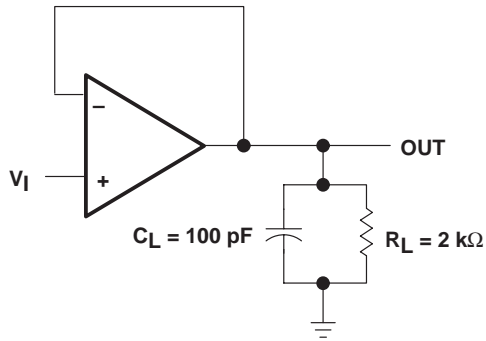


Figure 1

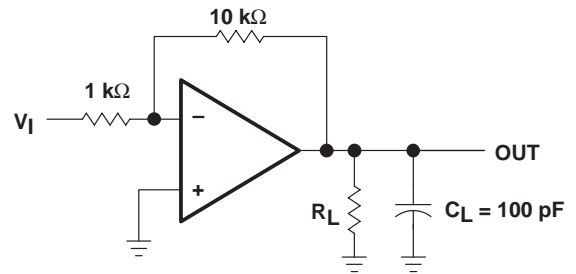


Figure 2

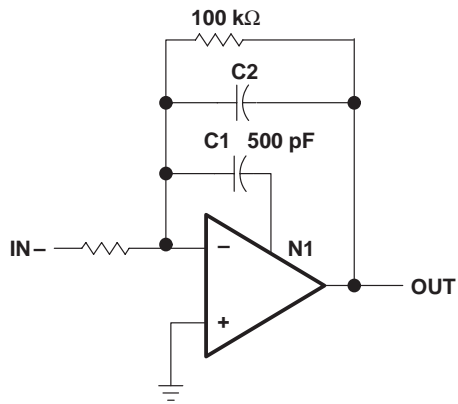


Figure 3

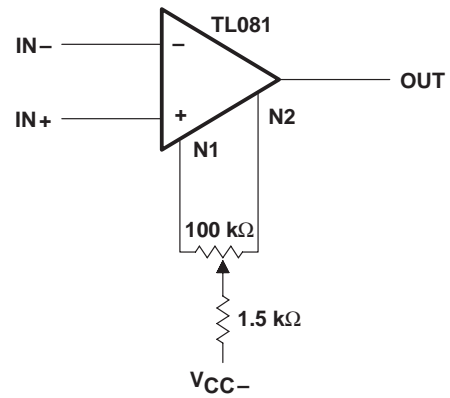


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V _{OM}	Maximum peak output voltage	vs Frequency
		vs Free-air temperature
		vs Load resistance
		vs Supply voltage
A _{VD}	Large-signal differential voltage amplification	5, 6, 7
	Differential voltage amplification	8, 9, 10
P _D	Total power dissipation	11, 12
I _{CC}	Supply current	13
I _{IB}	Input bias current	14
	Large-signal pulse response	15
V _O	Output voltage	16
CMRR	Common-mode rejection ratio	17
V _n	Equivalent input noise voltage	18
THD	Total harmonic distortion	19, 20, 21, 22

**MAXIMUM PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY**

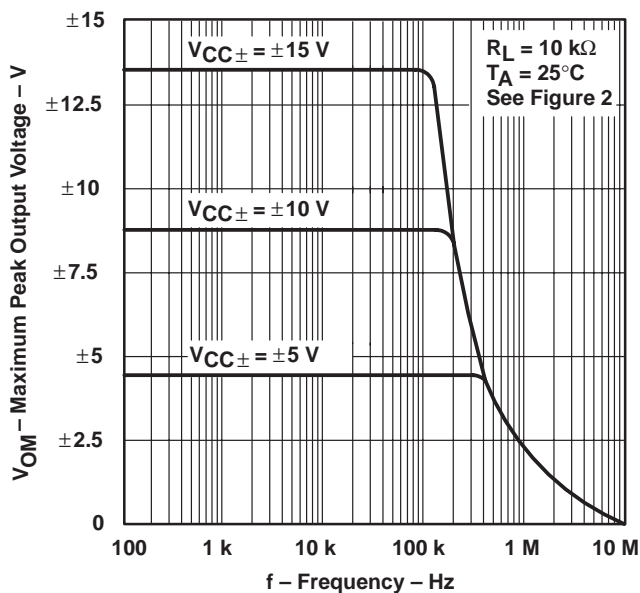


Figure 5

**MAXIMUM PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY**

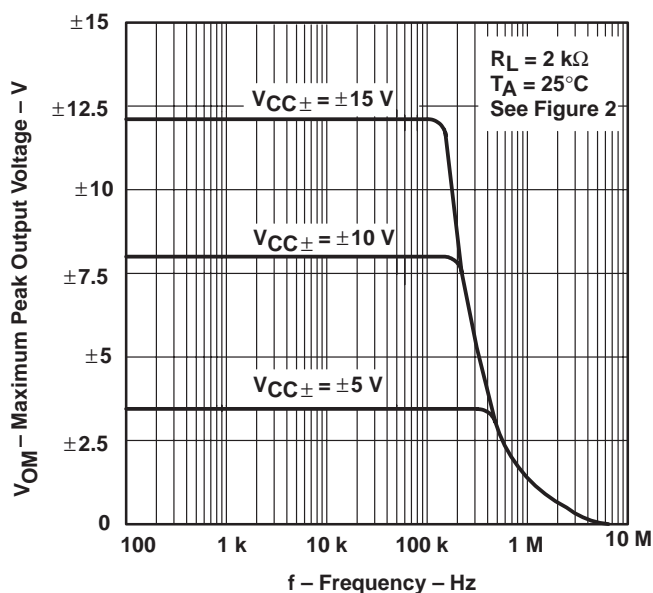


Figure 6

TYPICAL CHARACTERISTICS†

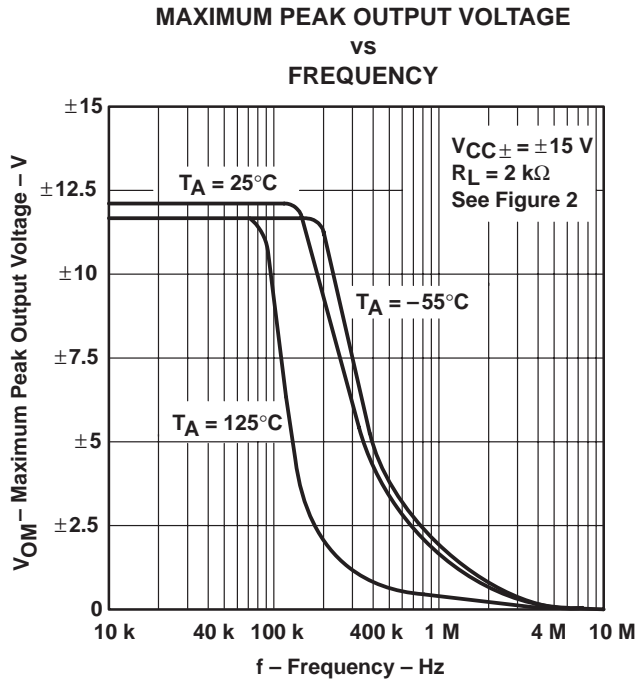


Figure 7

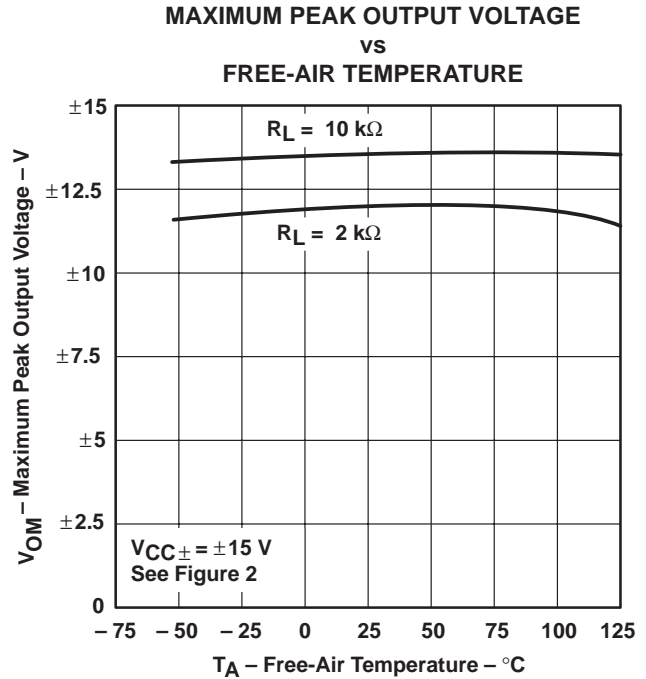


Figure 8

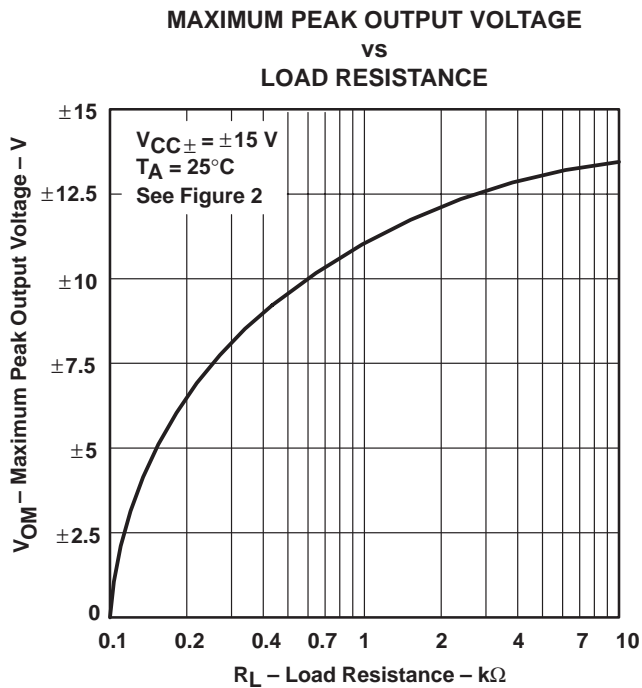


Figure 9

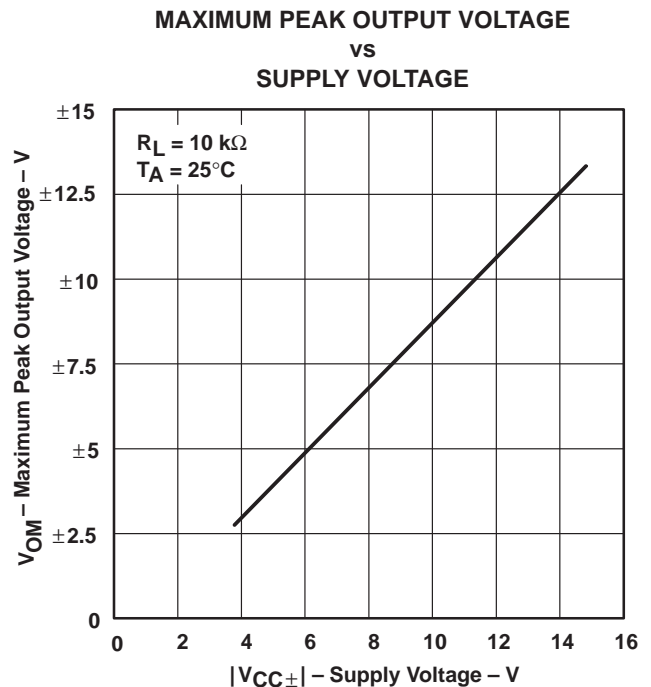


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

TYPICAL CHARACTERISTICS†

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE**

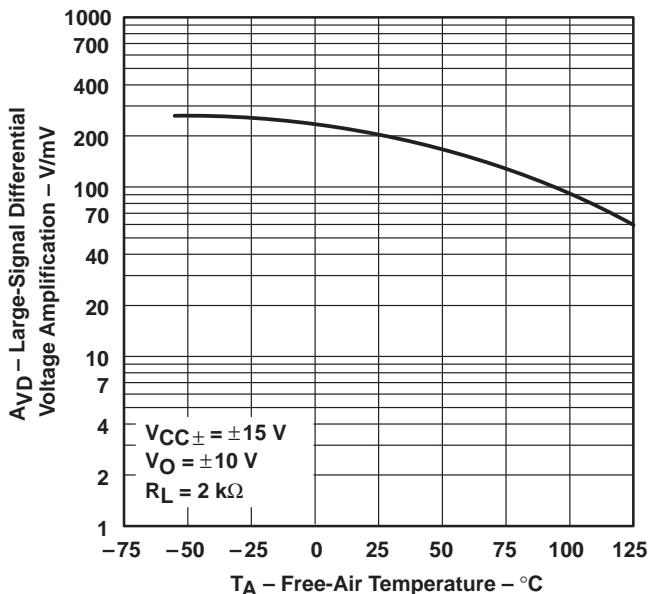


Figure 11

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREQUENCY**

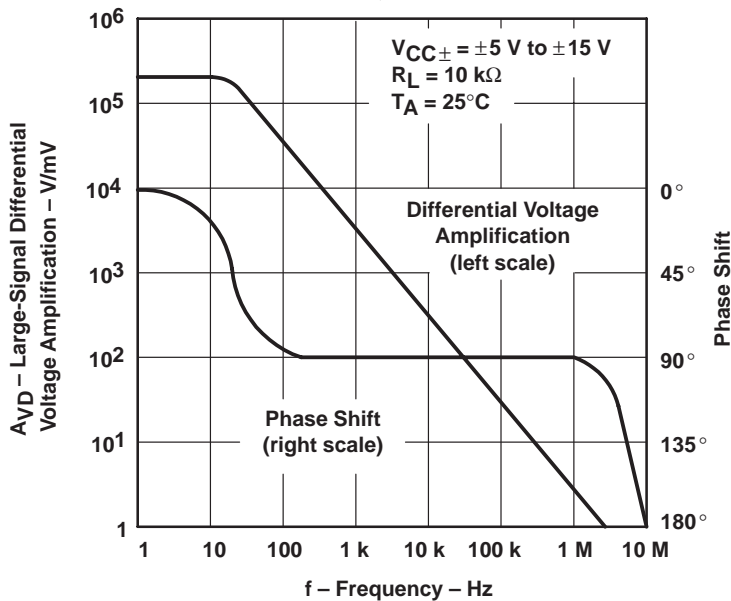


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREQUENCY WITH FEED-FORWARD COMPENSATION

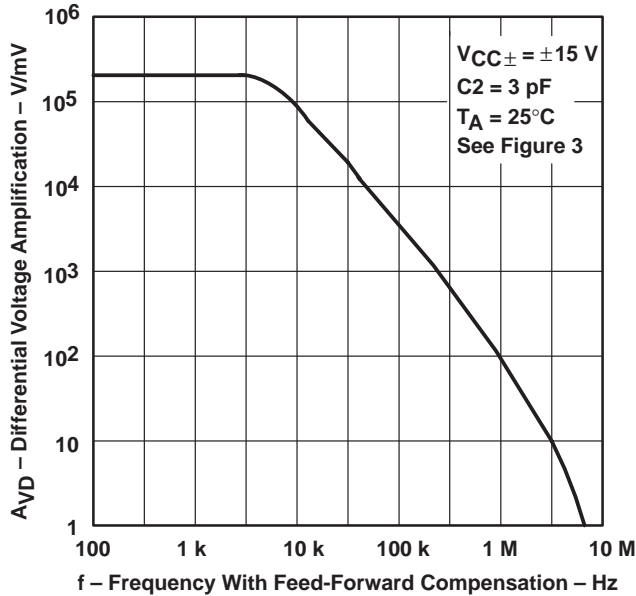


Figure 13

TOTAL POWER DISSIPATION
 vs
 FREE-AIR TEMPERATURE

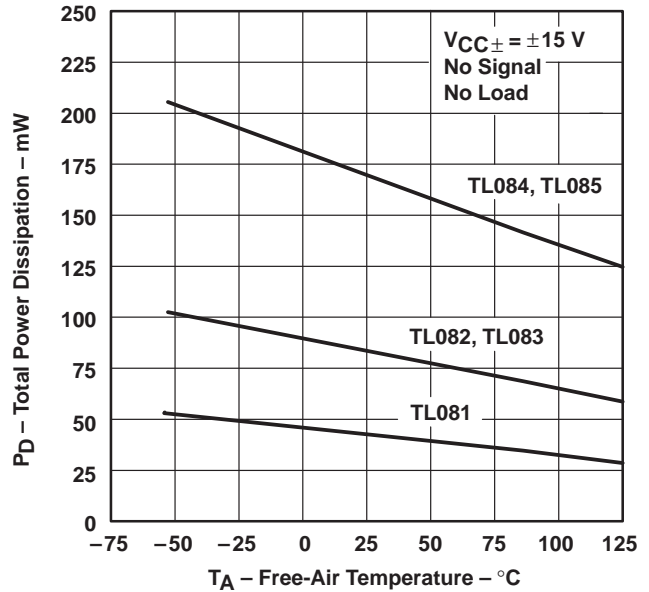


Figure 14

SUPPLY CURRENT PER AMPLIFIER
 vs
 FREE-AIR TEMPERATURE

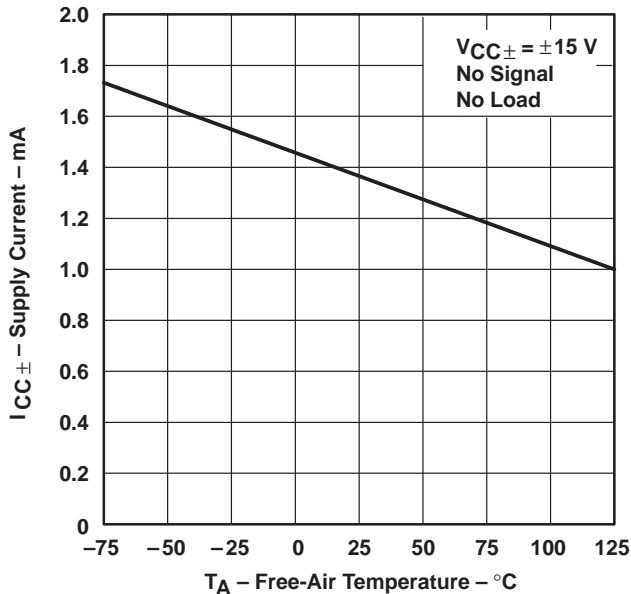


Figure 15

SUPPLY CURRENT
 vs
 SUPPLY VOLTAGE

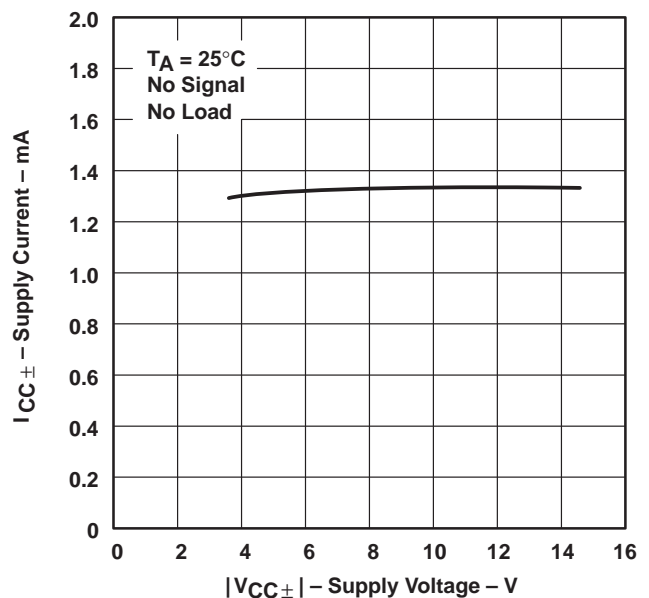


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

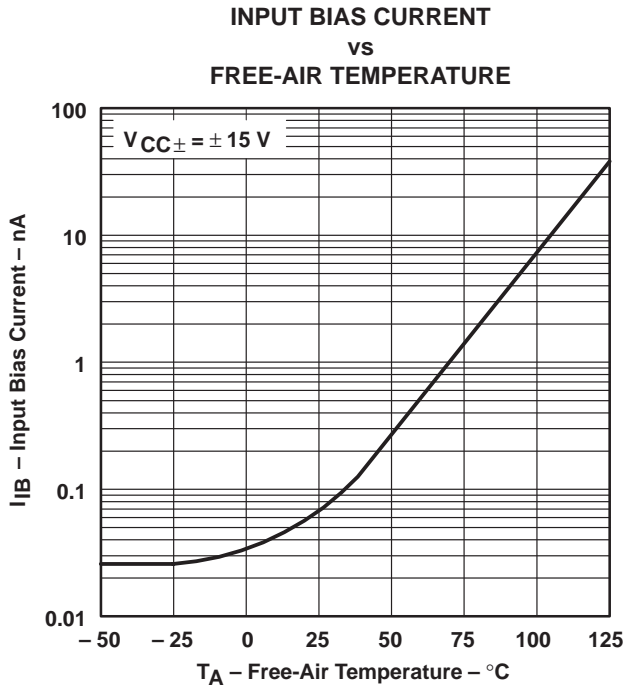


Figure 17

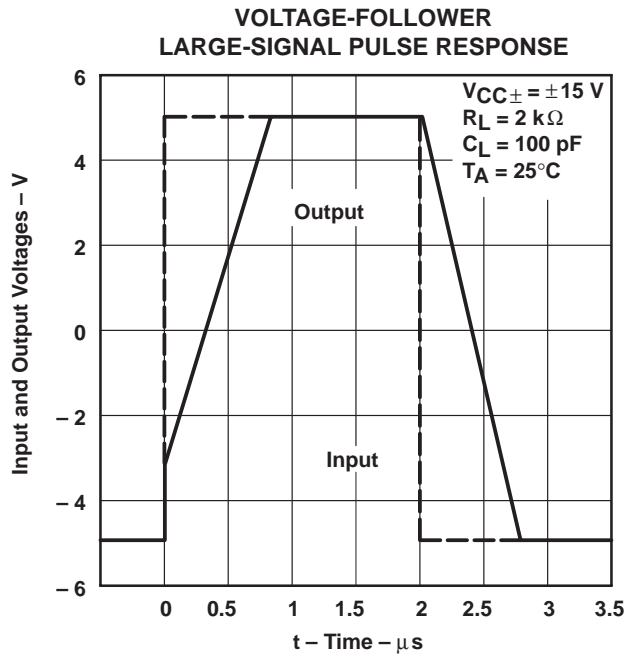


Figure 18

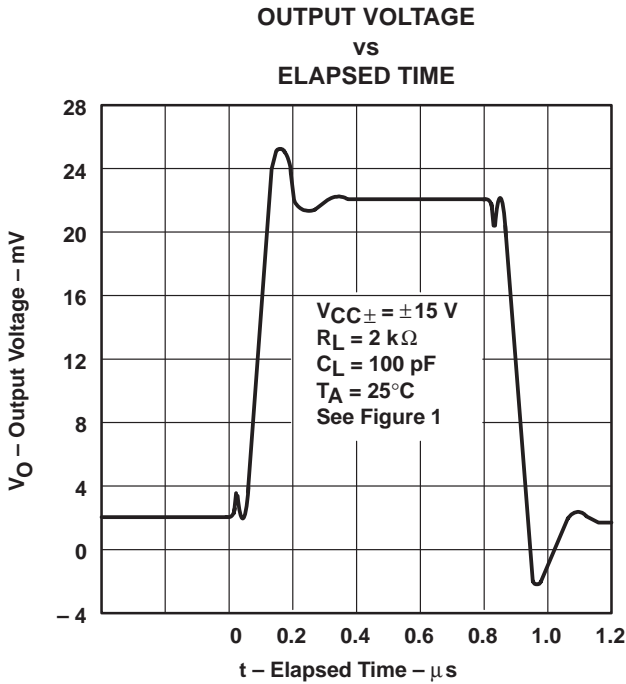


Figure 19

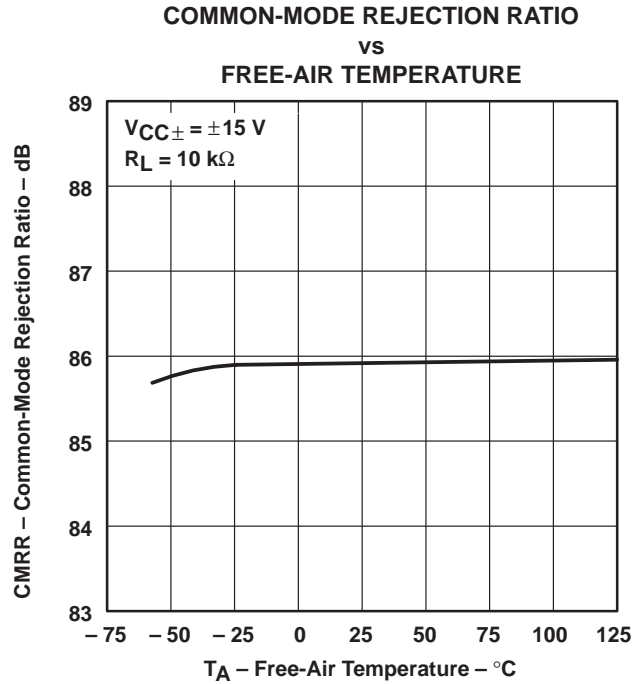
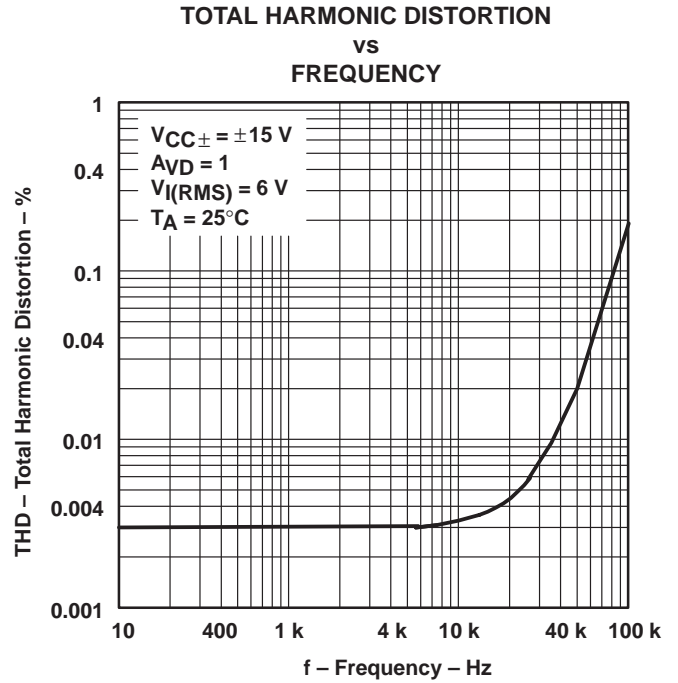
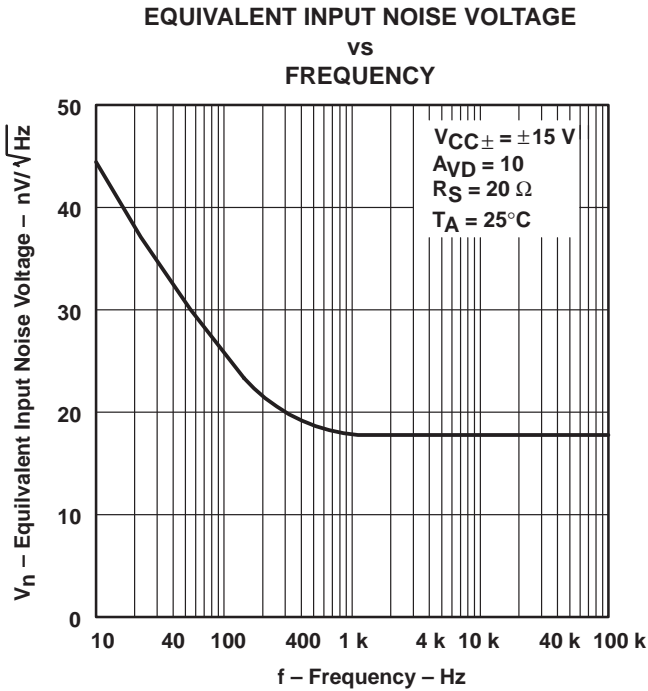


Figure 20

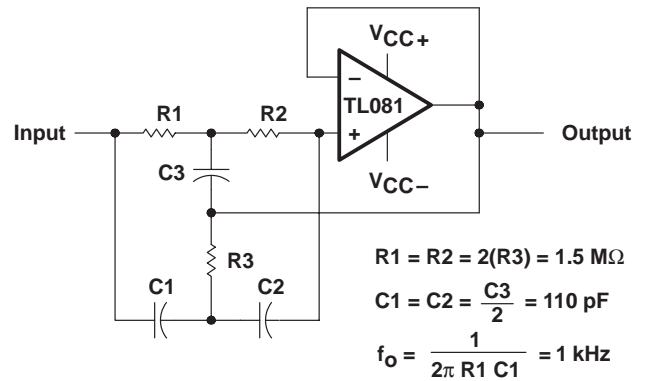
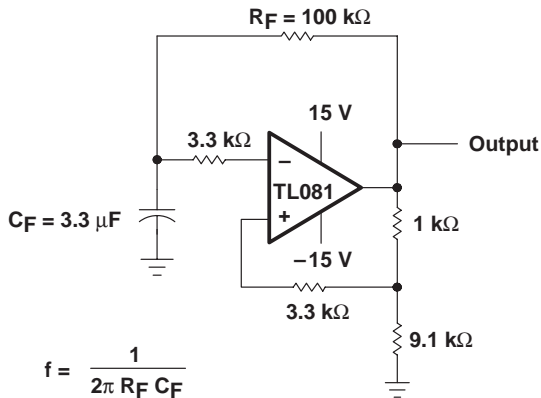
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION



APPLICATION INFORMATION

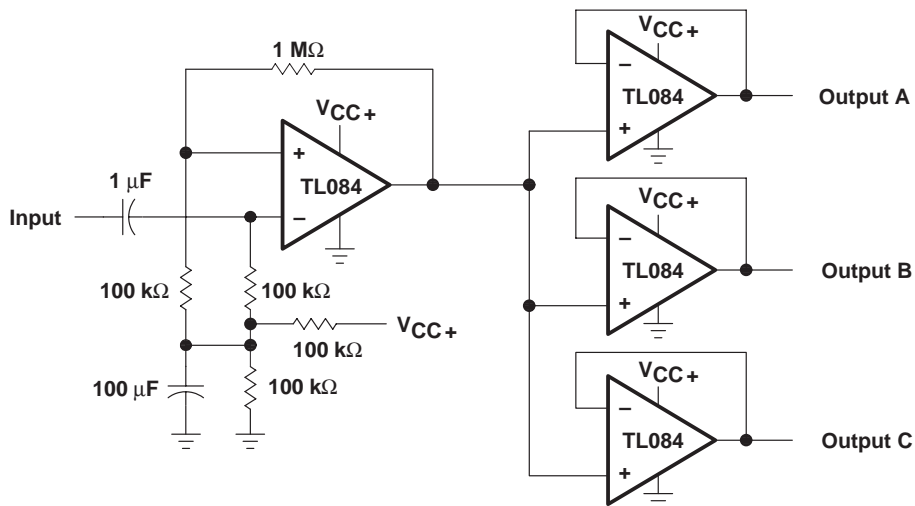
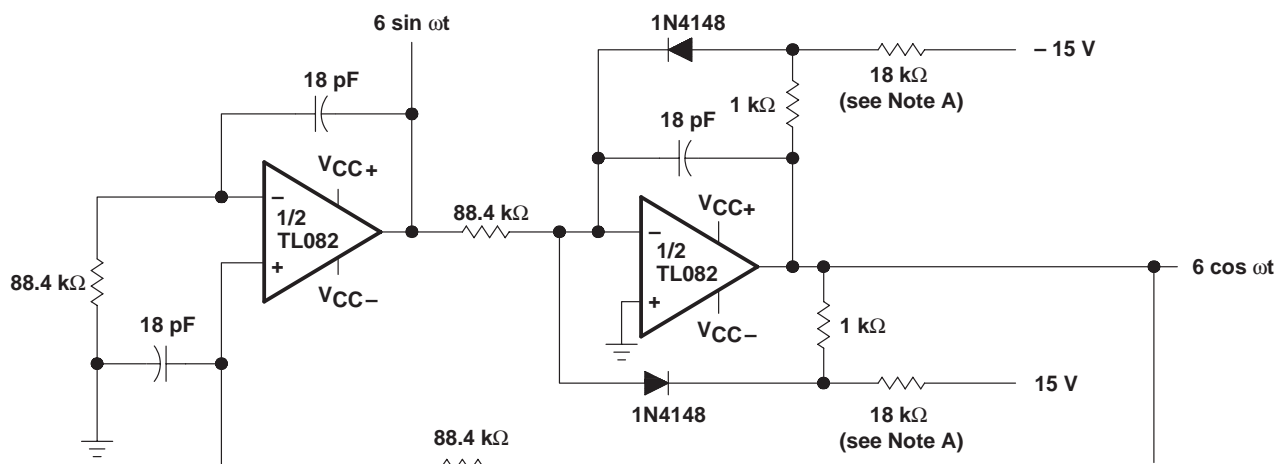


Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

APPLICATION INFORMATION

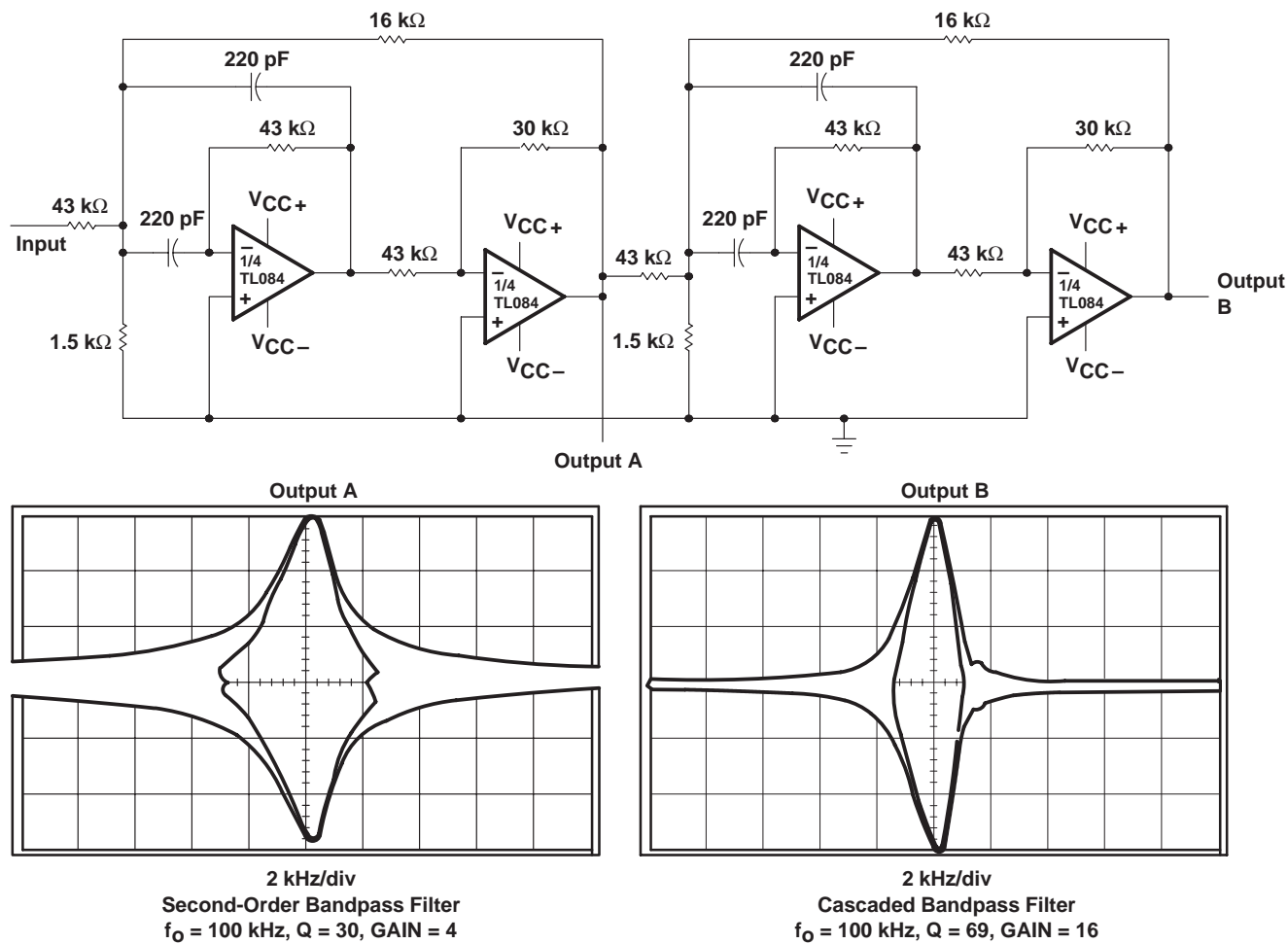


Figure 27. Positive-Feedback Bandpass Filter

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

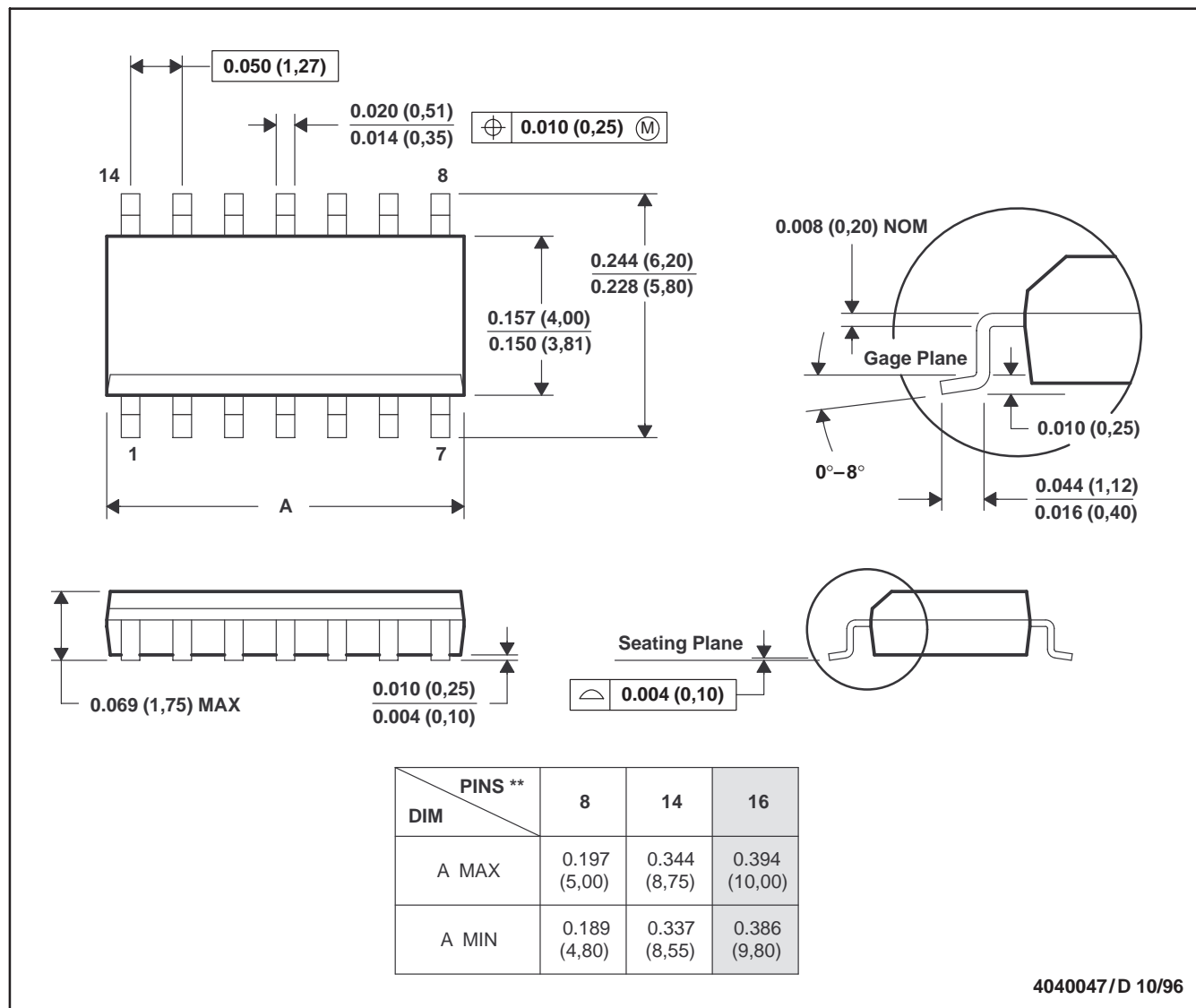
SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
 JFET-INPUT OPERATIONAL AMPLIFIERS

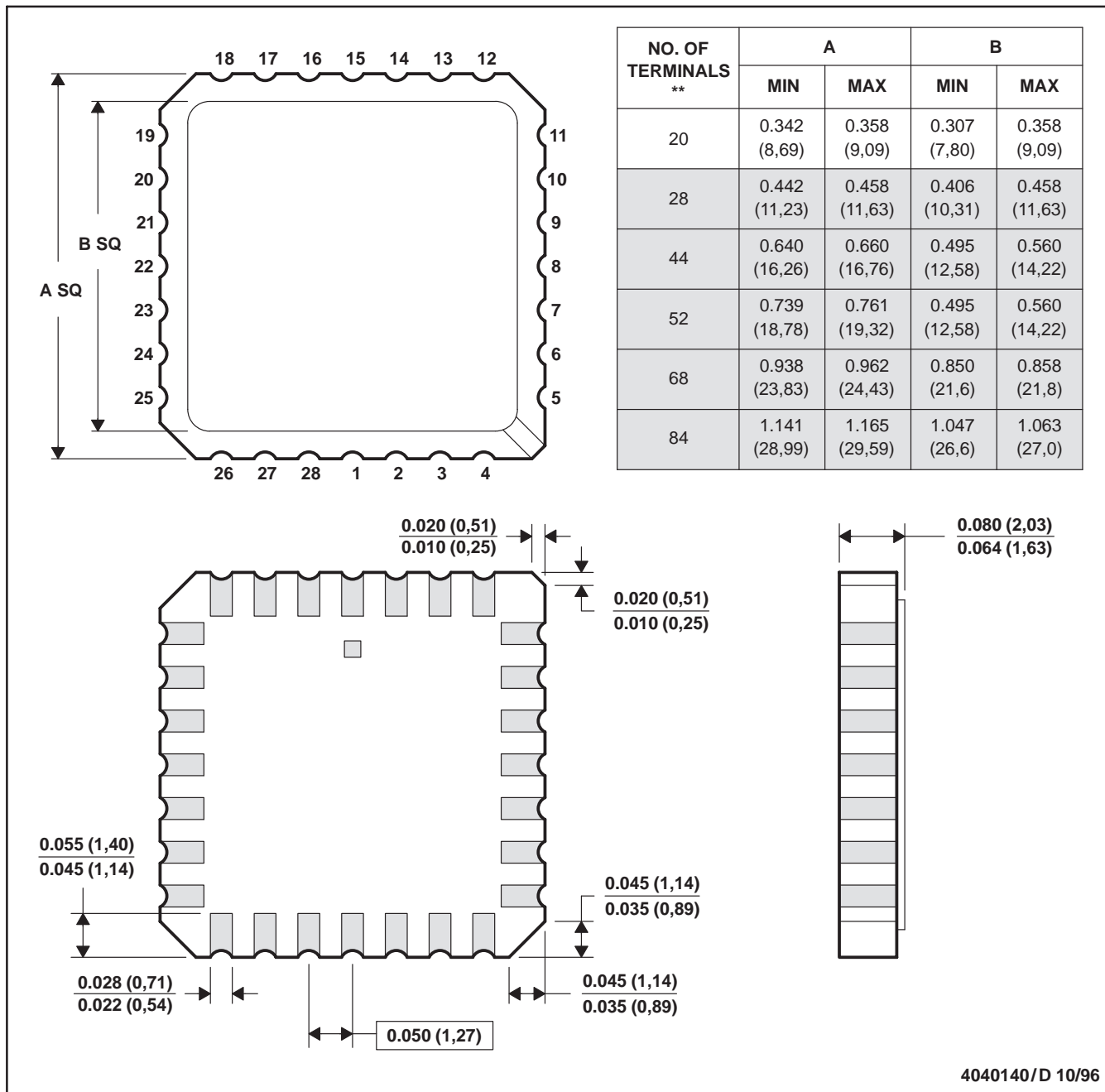
SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MS-004

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

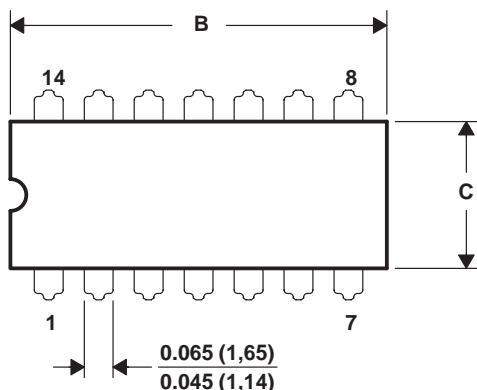
SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

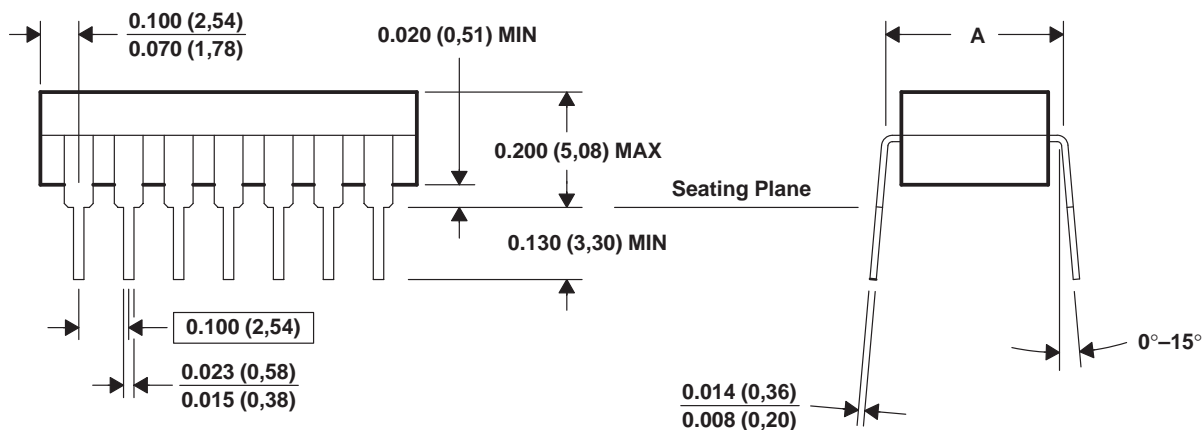
J (R-GDIP-T)**

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	PINS **			
	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)



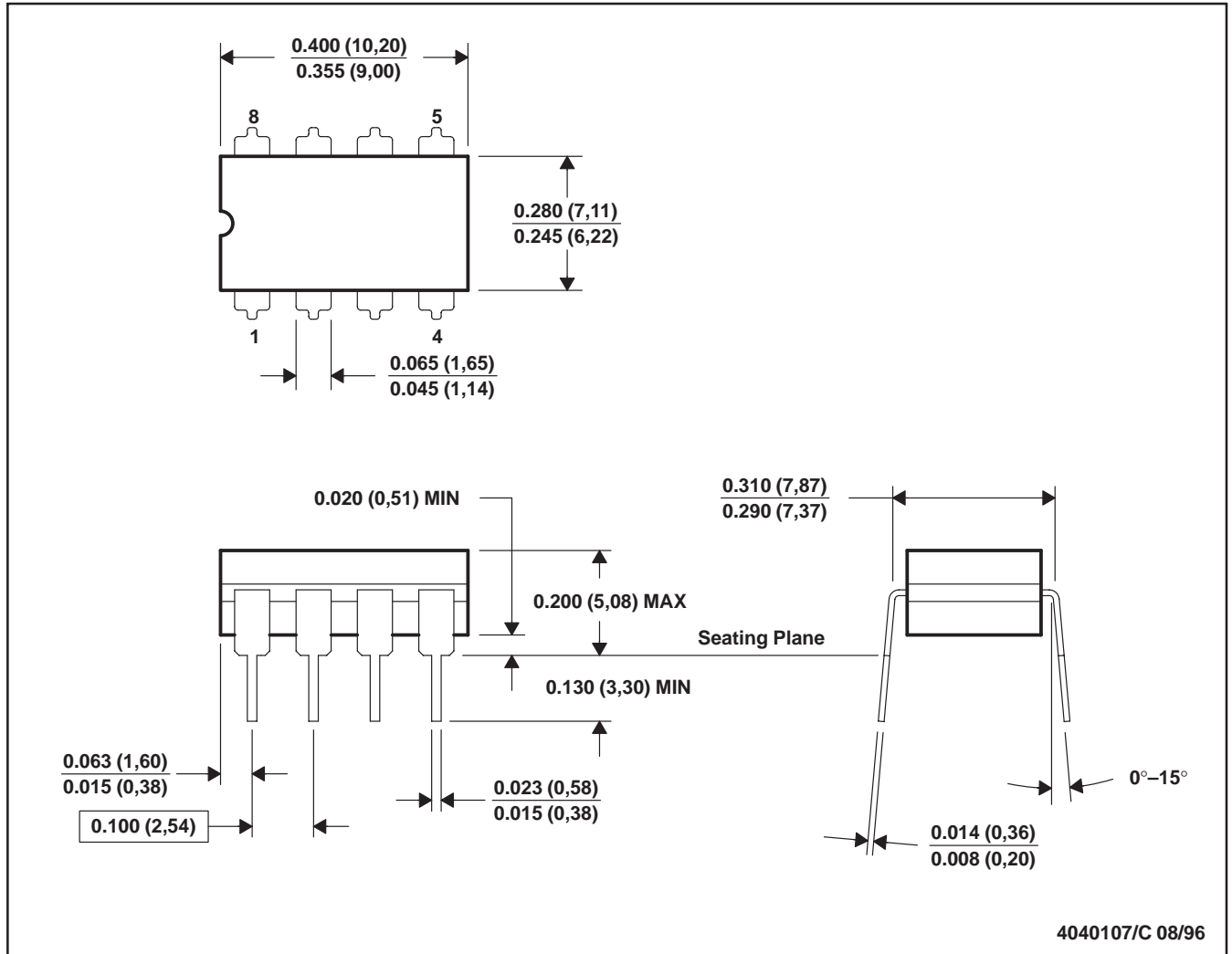
4040083/D 08/98

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

MECHANICAL DATA

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 E. Falls within MIL-STD-1835 GDIP1-T8

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

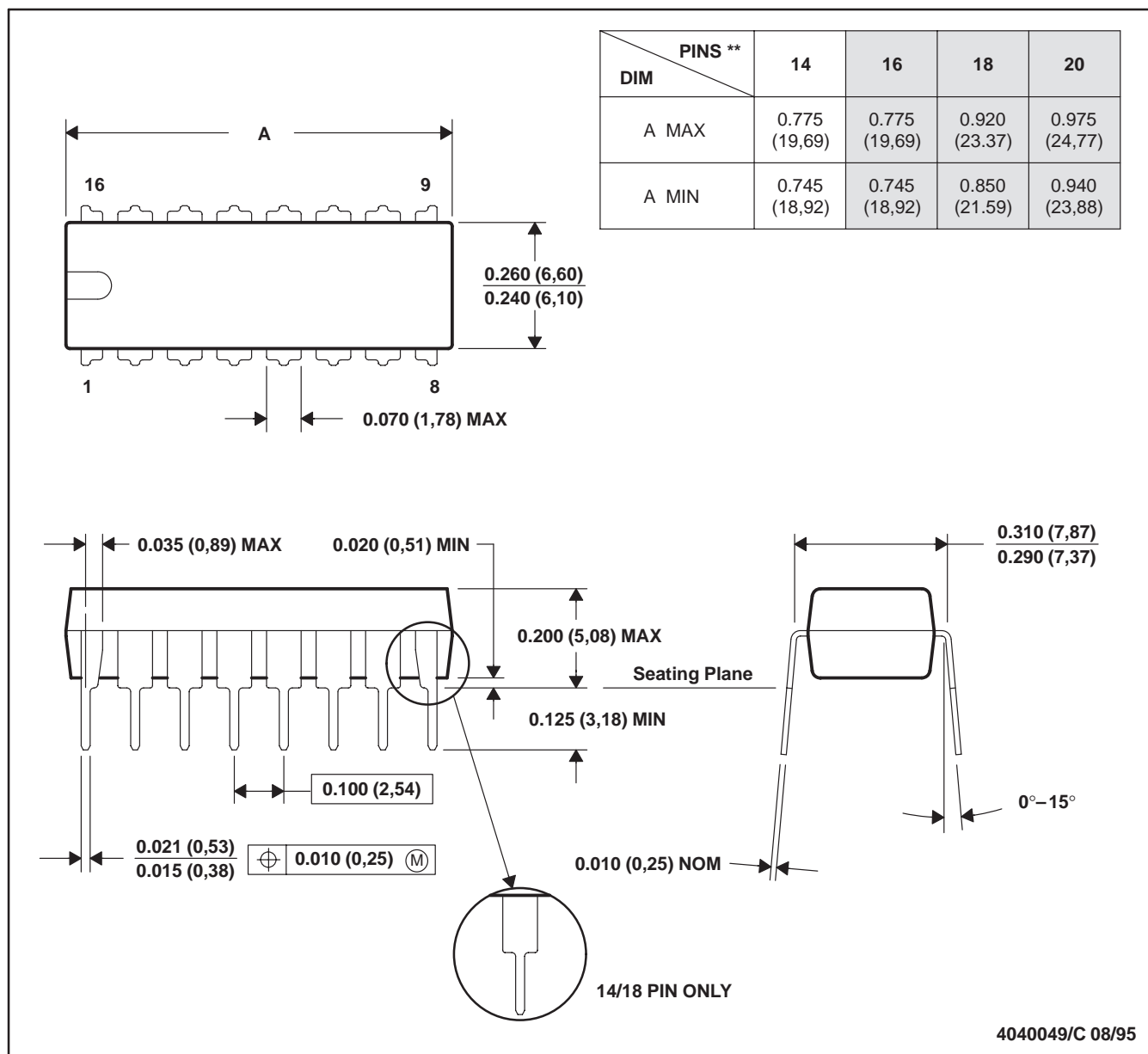
SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN

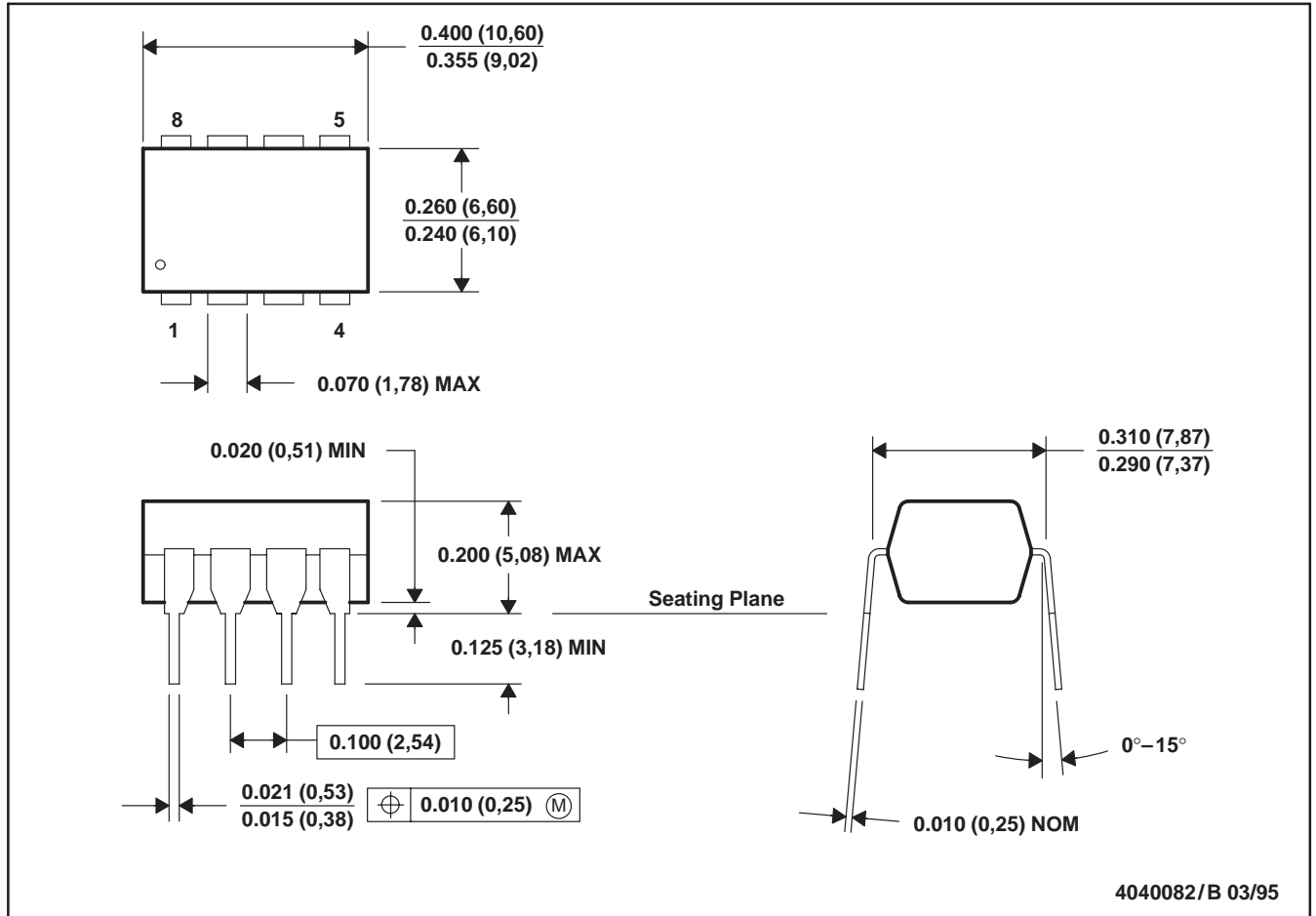


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

MECHANICAL DATA

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

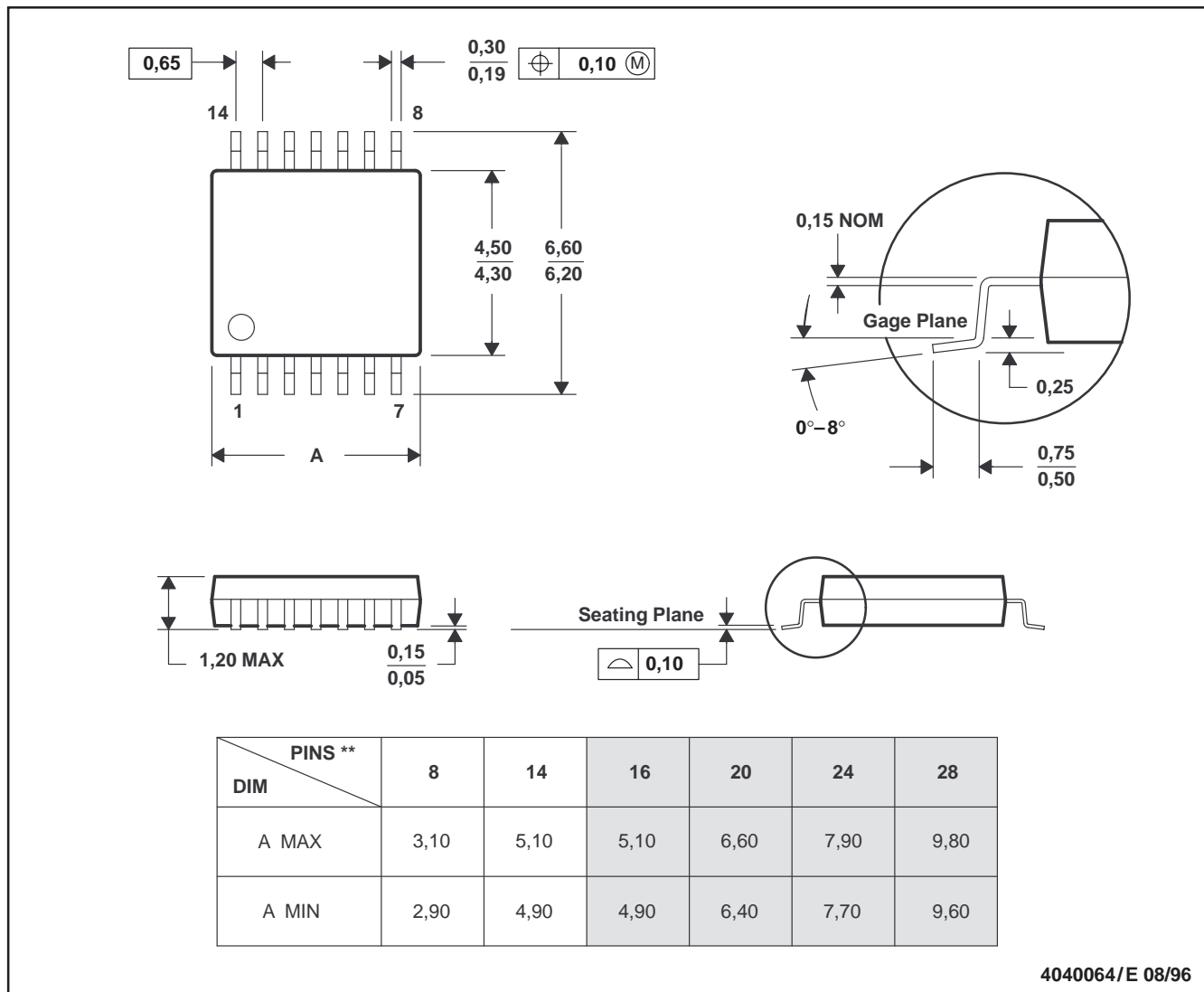
SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

PW (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/E 08/96

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

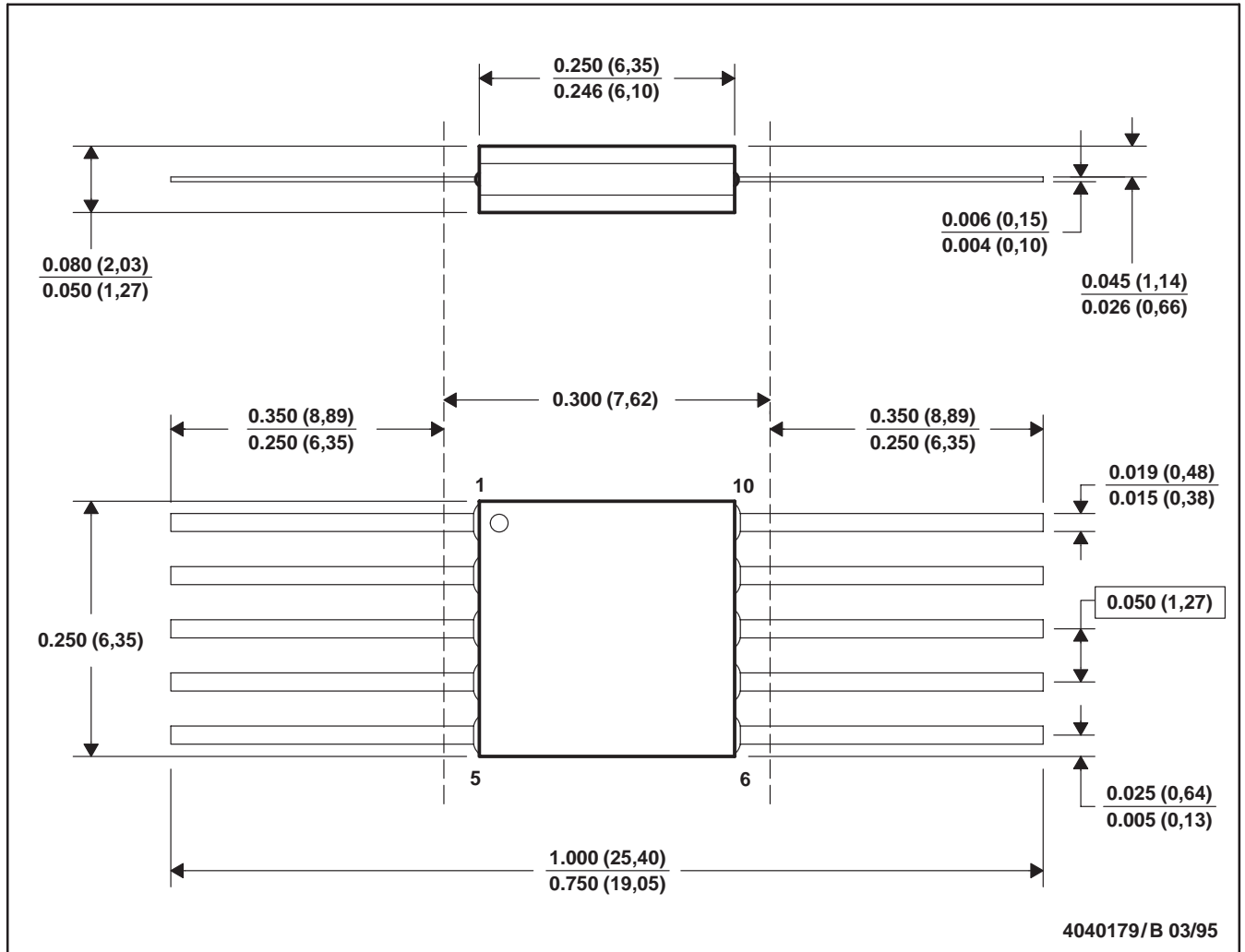
TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
 JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

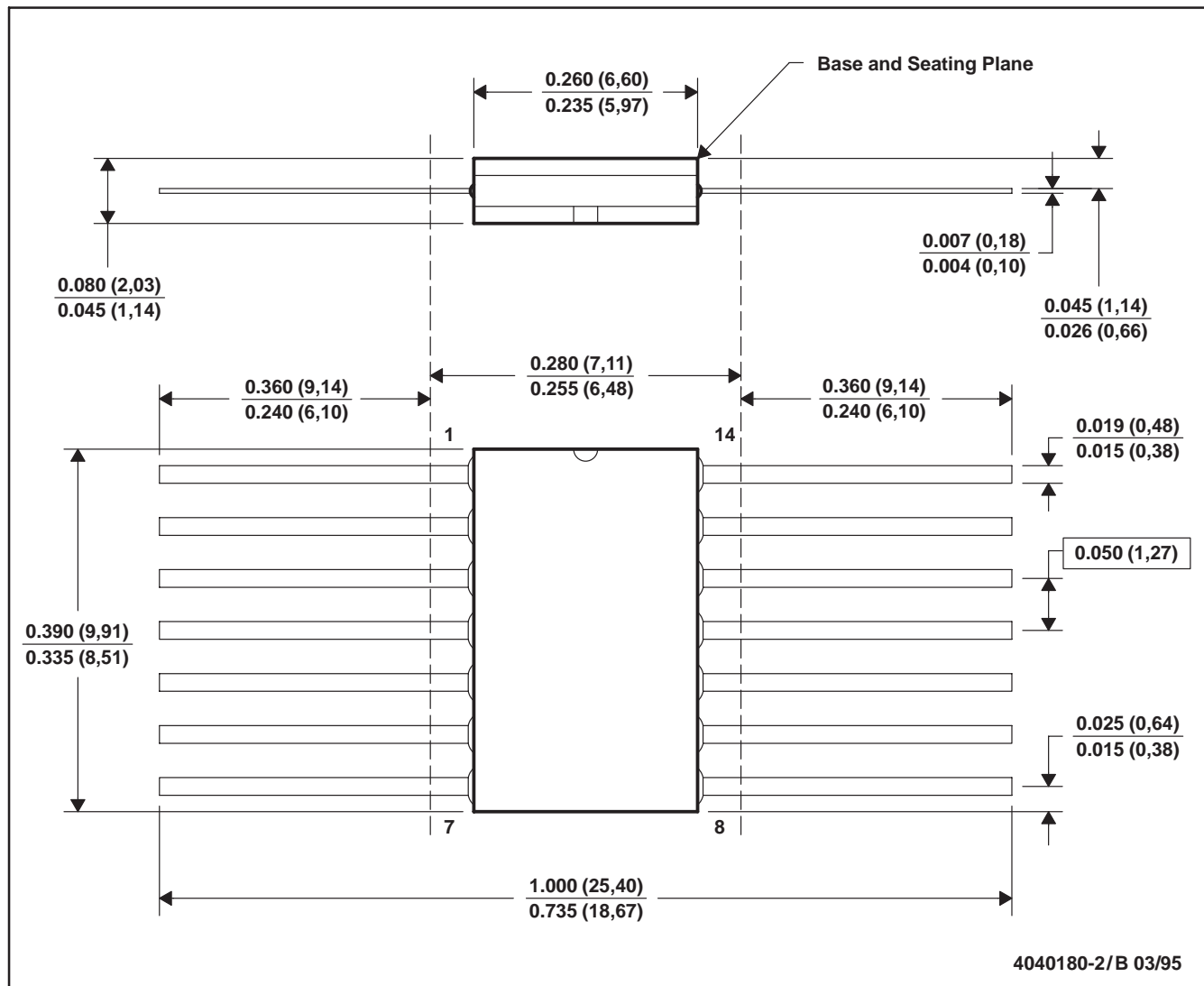
TL081, TL081A, TL081B, TL082, TL082A, TL082B
 TL082Y, TL084, TL084A, TL084B, TL084Y
JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081E – FEBRUARY 1977 – REVISED FEBRUARY 1999

MECHANICAL DATA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

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