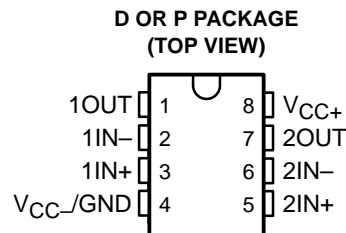


# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/ $\mu$ s**
- **Fast Settling Time . . . 1.1  $\mu$ s to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground ( $V_{CC-}$ )**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**



### description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/ $\mu$ s slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ( $V_{CC-}$ ). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

### ORDERING INFORMATION

$T_A$	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD
		Reel of 2500	TL3472CDR
–40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID
		Reel of 2500	TL3472IDR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

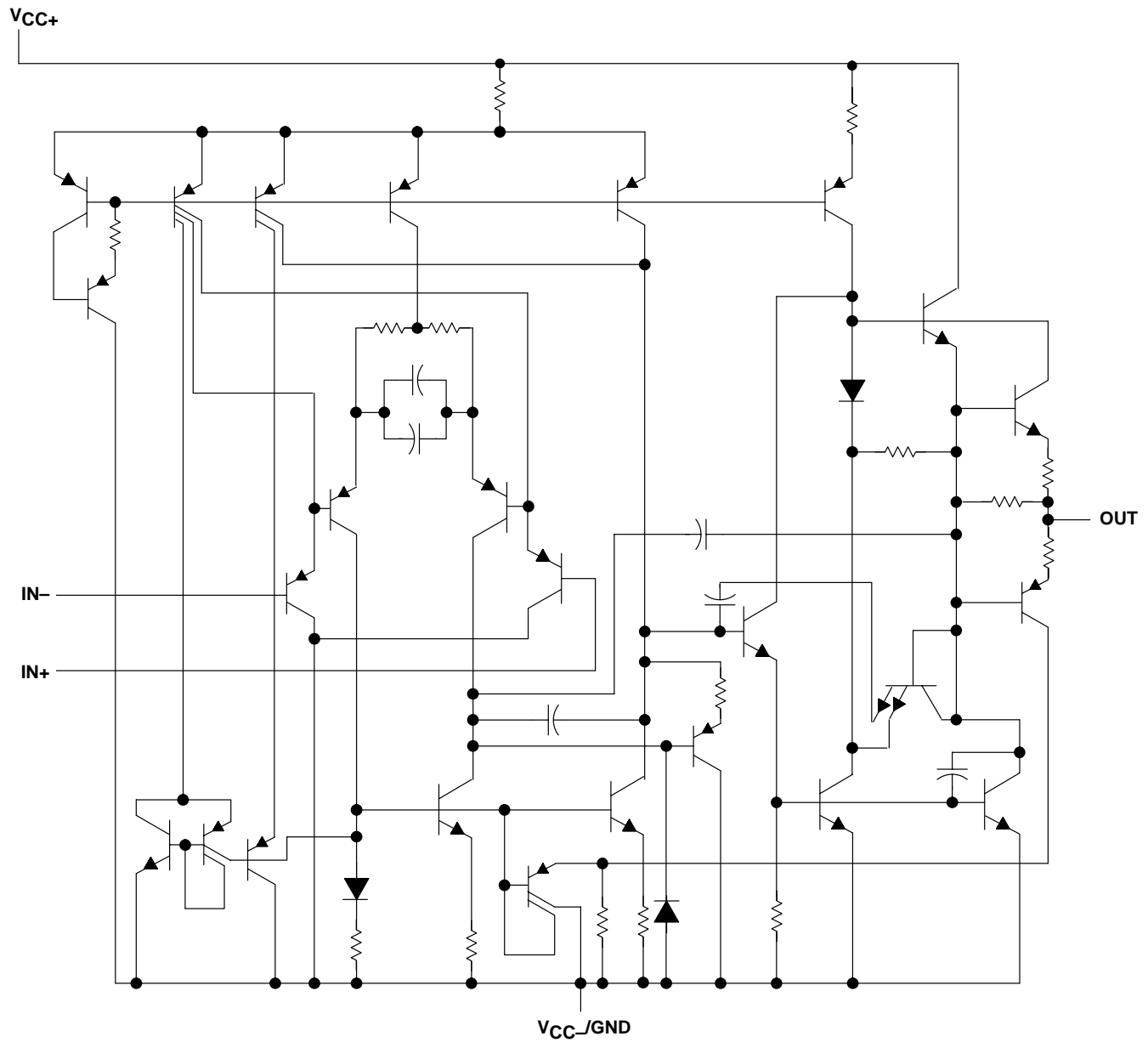
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# TL3472 HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

## schematic (each amplifier)



# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): $V_{CC+}$ .....	18 V
$V_{CC-}$ .....	-18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 36$ V
Input voltage, $V_I$ (any input) .....	$V_{CC\pm}$
Input current, $I_I$ (each input) .....	$\pm 1$ mA
Output current, $I_O$ .....	$\pm 80$ mA
Total current into $V_{CC+}$ .....	80 mA
Total current out of $V_{CC-}$ .....	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .....	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 4 and 5): D package .....	97°C/W
P package .....	85°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....	260°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than  $V_{CC-} - 0.3$  V.
  3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
  4. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		MIN	MAX	UNIT	
$V_{CC\pm}$	Supply voltage	4	36	V	
$V_{IC}$	Common-mode input voltage	$V_{CC} = 5$ V	0	2.8	V
		$V_{CC\pm} = \pm 15$ V	-15	12.8	
$T_A$	Operating free-air temperature	TL3472C	0	70	°C
		TL3472I	-40	105	



# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

### electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP†	MAX	UNIT
$V_{IO}$ Input offset voltage	$V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$	$V_{CC} = 5\text{ V}$	25°C	1.5	10	mV
		$V_{CC} = \pm 15\text{ V}$	25°C	1.0	10	
			Full range‡			
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_{IC} = 0$ , $V_O = 0$ , $R_S = 50\ \Omega$	$V_{CC} = \pm 15\text{ V}$	Full range‡	10		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$ Input offset current		$V_{CC} = \pm 15\text{ V}$	25°C	6	75	nA
			Full range‡			
$I_{IB}$ Input bias current		$V_{CC} = \pm 15\text{ V}$	25°C	100	500	nA
	Full range‡				700	
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C		-15 to 12.8		V
		Full range‡			-15 to 12.8	
$V_{OH}$ High-level output voltage	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0$ , $R_L = 2\text{ k}\Omega$	25°C	3.7	4	V	
		25°C	13.6	14		
		Full range‡	13.4			
$V_{OL}$ Low-level output voltage	$V_{CC+} = 5\text{ V}$ , $V_{CC-} = 0$ , $R_L = 2\text{ k}\Omega$	25°C	0.1	0.3	V	
		25°C	-14.7	-14.3		
		Full range‡	-13.5			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\text{ V}$ , $R_L = 2\text{ k}\Omega$	25°C	25	100	V/mV	
		Full range‡	20			
$I_{OS}$ Short-circuit output current	Source: $V_{ID} = 1\text{ V}$ , $V_O = 0$ Sink: $V_{ID} = -1\text{ V}$ , $V_O = 0$	25°C	-10	-34	mA	
			20	27		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}(\text{min})$ , $R_S = 50\ \Omega$	25°C	65	97	dB	
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 13.5\text{ V}$ to $\pm 16.5\text{ V}$ , $R_S = 100\ \Omega$	25°C	70	97	dB	
$I_{CC}$ Supply current (per channel)	$V_O = 0$ , No load	25°C	3.5	4.5	mA	
		Full range‡	4.5	5.5		
		25°C	3.5	4.5		

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the TL3472C device and  $-40^\circ\text{C}$  to  $105^\circ\text{C}$  for the TL3472I device.

# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

### operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_I = -10\text{ V to } 10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 300\text{ pF}$	$A_V = 1$	8	10		$\text{V}/\mu\text{s}$
SR-	Negative slew rate		$A_V = -1$		13		$\text{V}/\mu\text{s}$
$t_s$	Settling time	$A_{VD} = -1$ , 10-V step	To 0.1%		1.1		$\mu\text{s}$
			To 0.01%		2.2		
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$ ,	$R_S = 100\ \Omega$		49		$\text{nV}/\sqrt{\text{Hz}}$
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$			0.22		$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion	$V_{O(PP)} = 2\text{ V to } 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$			0.02		%
GBW	Gain-bandwidth product	$f = 100\text{ kHz}$		3	4		MHz
BW	Power bandwidth	$V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 1$ , THD = 5.0%			160		kHz
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$	$C_L = 0$		70		deg
			$C_L = 300\text{ pF}$		50		
	Gain margin	$R_L = 2\text{ k}\Omega$	$C_L = 0$		12		dB
			$C_L = 300\text{ pF}$		4		
$r_i$	Differential input resistance	$V_{IC} = 0$			150		$\text{M}\Omega$
$C_i$	Input capacitance	$V_{IC} = 0$			2.5		pF
	Channel separation	$f = 10\text{ kHz}$			101		dB
$z_o$	Open-loop output impedance	$f = 1\text{ MHz}$ ,	$A_V = 1$		20		$\Omega$

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL3472CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL3472CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL3472CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL3472ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL3472IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL3472IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

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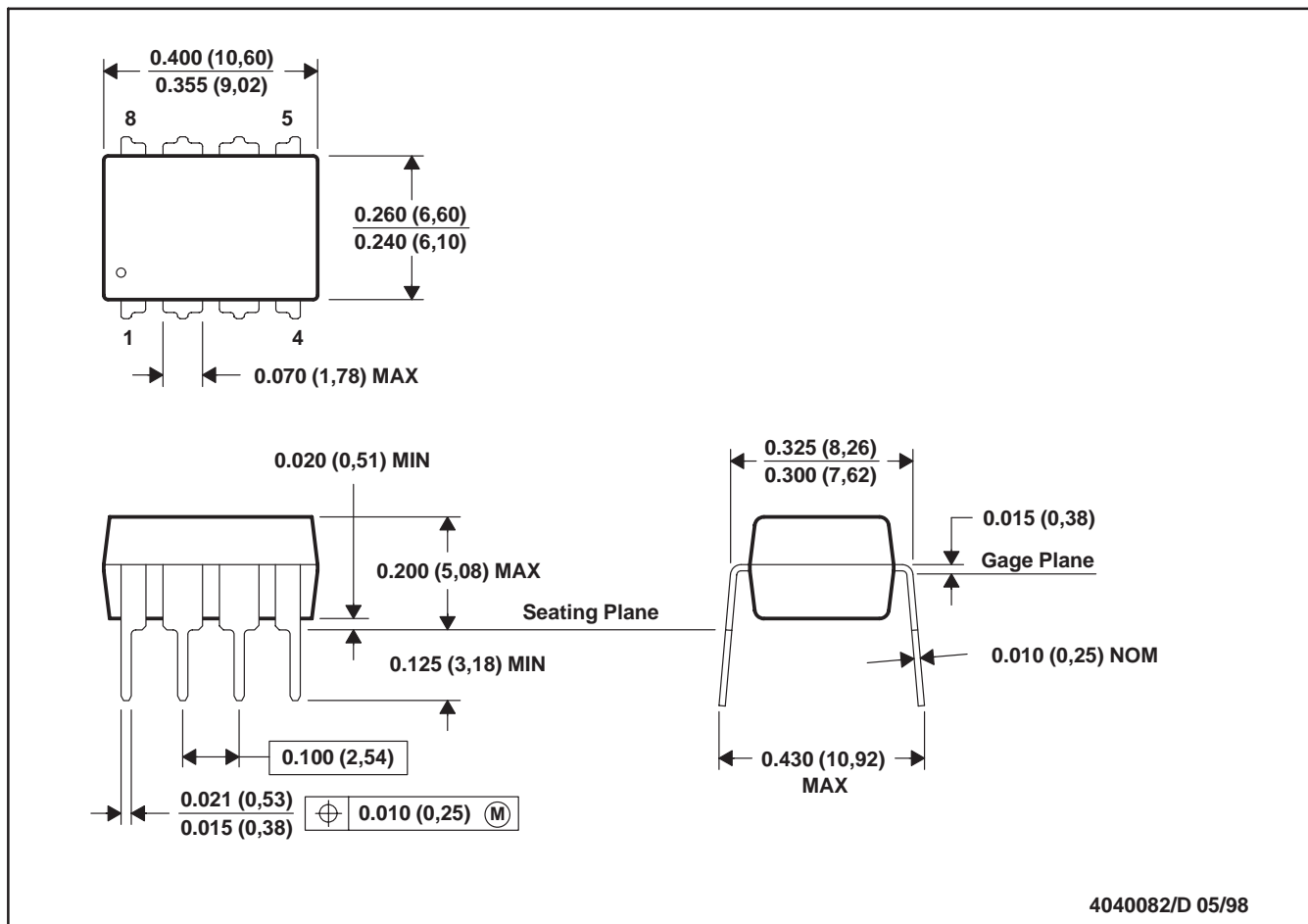
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

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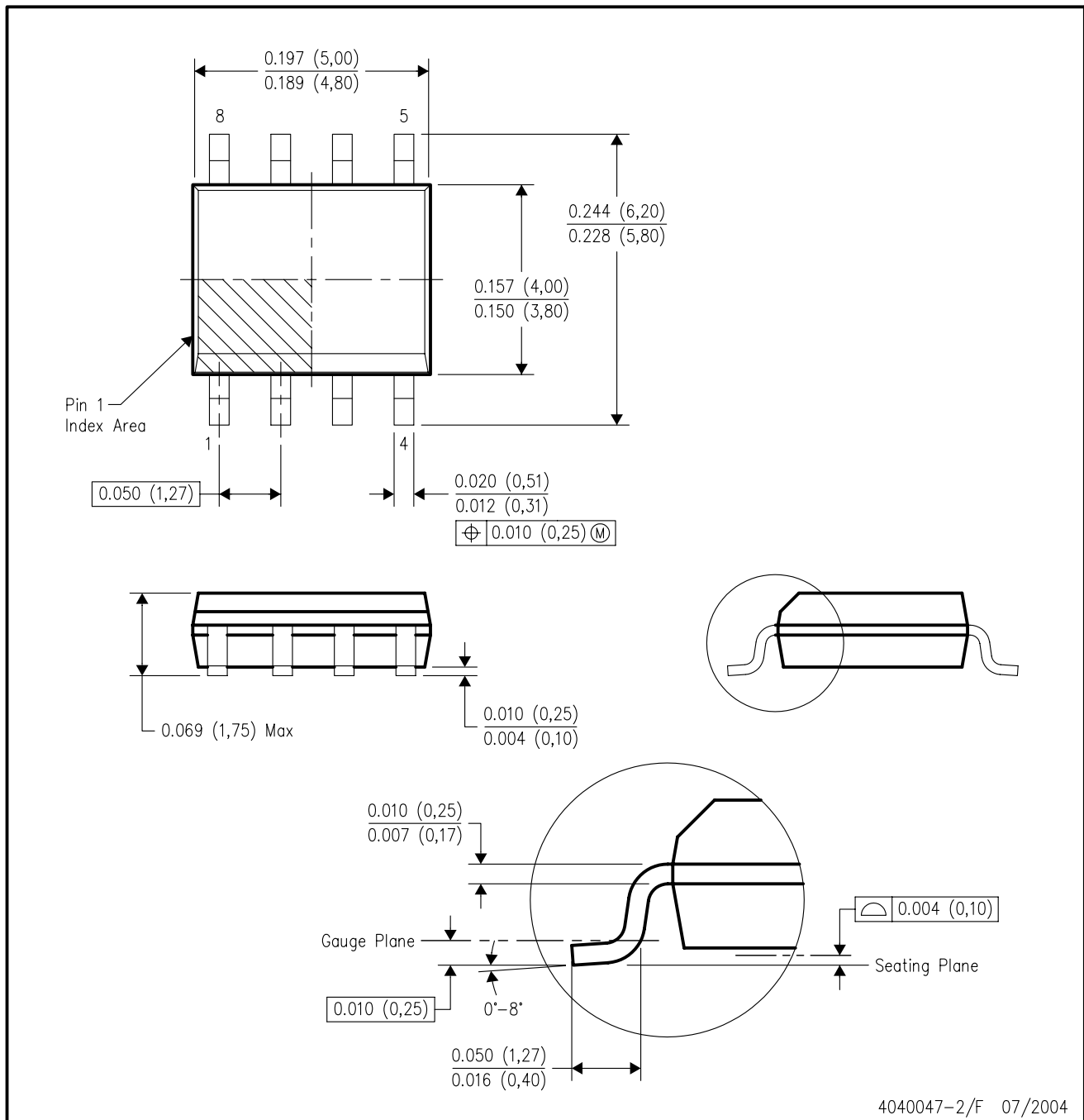


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
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  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AA.

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