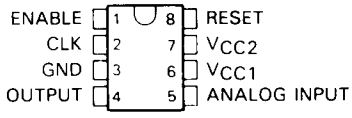
D2503, OCTOBER 1979—REVISED OCTOBER 1988

- Low Cost
- 7-Bit Resolution
- Monotonicity Over Entire A/D Conversion Range
- Ratiometric Conversion
- Conversion Speed . . . Approximately 1 ms
- Single-Supply Operation . . . Either Unregulated 8-V to 18-V (V_{CC2} Input), or Regulated 3.5-V to 6-V (V_{CC1} Input)
- I^2L Technology
- Power Consumption at 5 V . . . 25 mW Typ
- Regulated 5.5 V Output (≤ 1 mA)

P PACKAGE
(TOP VIEW)



FUNCTION TABLE

ANALOG INPUT CONDITION	ENABLE	OUTPUT
X	L†	H
$V_I < 200$ mV	H	L
$V_{ramp} > V_I > 200$ mV	H	H
$V_I > V_{ramp}$	H	L

†Low level on enable also inhibits the reset function.
H = high level, L = low level, X = irrelevant

A high level on the reset pin clears the counter to zero, which sets the internal ramp to 0.75 V_{CC}. Internal pull-down resistors keep the reset and enable pins low when not connected.

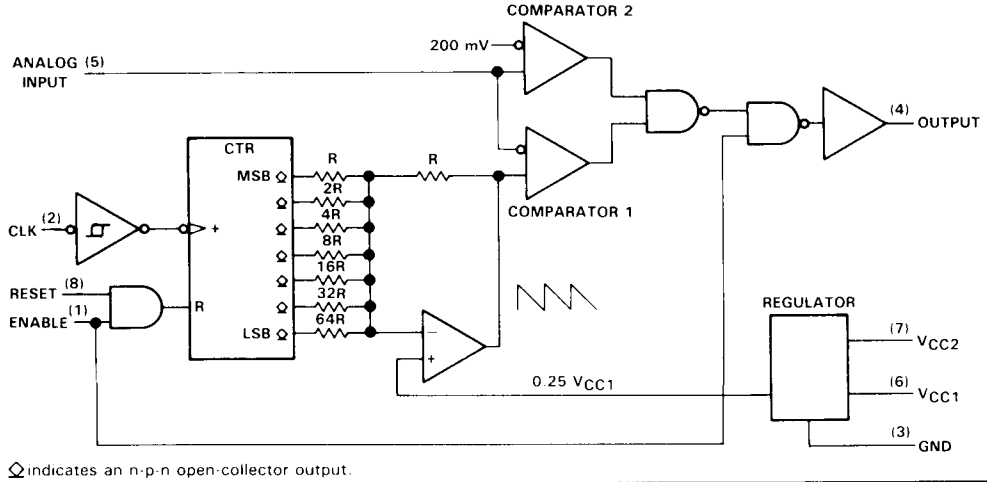
description

The TL507 is a low-cost single-slope analog-to-digital converter designed to convert analog input voltages between 0.25 V_{CC1} and 0.75 V_{CC1} into a pulse-width-modulated output code. The device contains a 7-bit synchronous counter, a binary weighted resistor ladder network, an operational amplifier, two comparators, a buffer amplifier, an internal regulator, and necessary logic circuitry. Integrated-injection logic (I^2L) technology makes it possible to offer this complex circuit at low cost in a small dual-in-line 8-pin package.

In continuous operation, conversion speeds of up to 1000 conversions per second are possible. The TL507 requires external signals for clock, reset, and enable. Versatility and simplicity of operation, coupled with low cost, makes this converter especially useful for a wide variety of applications.

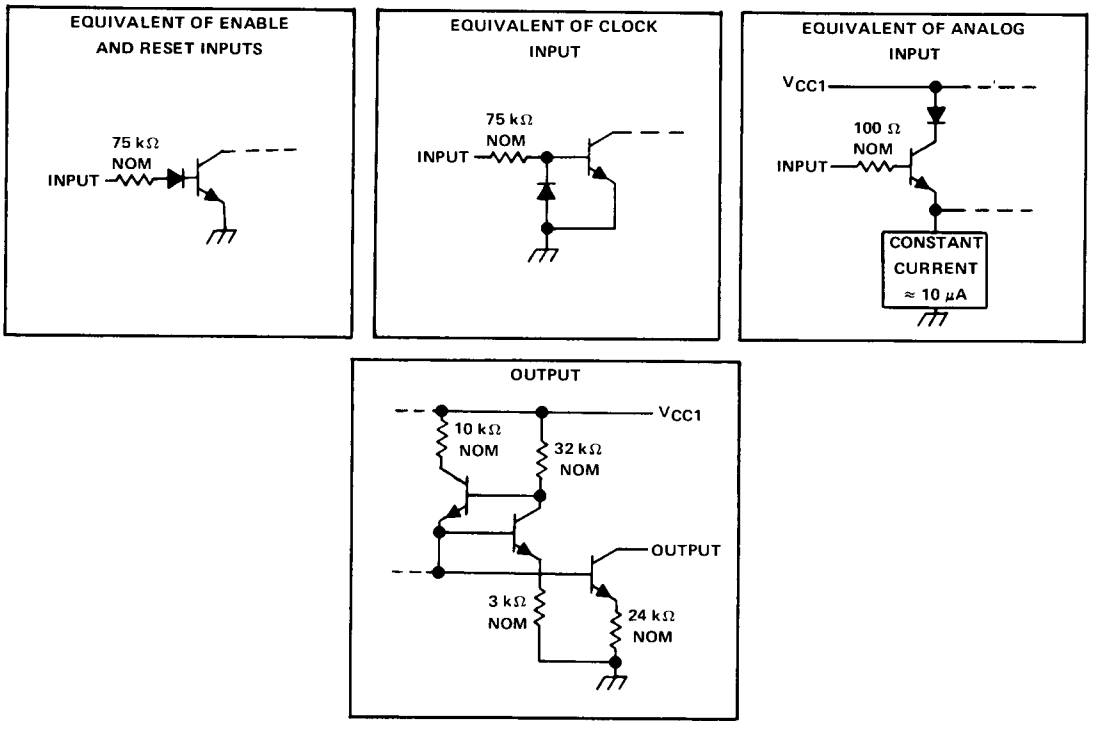
The TL507I is characterized for operation from −40°C to 85°C, and the TL507C is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



◇indicates an n-p-n open-collector output.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	6.5 V
Supply voltage, V_{CC2}	20 V
Input voltage at analog input	6.5 V
Input voltage at enable, clock, and reset inputs	±20 V
On-state output voltage	6 V
Off-state output voltage	20 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range: TL507I	−40°C to 85°C
TL507C	0 to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, derate linearly to 520 mW at 85°C at the rate of 8.0 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	3.5	5	6	V
Supply voltage, V_{CC2}	8	15	18	V
Input voltage at analog input	0		5.5	V
Input voltage at chip enable, clock, and reset inputs			±18	V
High-level input voltage, V_{IH}, reset and enable	2			V
Low-level input voltage, V_{IL}, reset and enable			0.8	V
On-state output voltage			5.5	V
Off-state output voltage			18	V
Clock frequency, f_{clock}	0	125	150	kHz

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = V_{CC2} = 5 V (unless otherwise noted)

regulator section

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{CC1}	Supply voltage (output)	V_{CC2} = 10 to 18 V,	I_{CC1} = 0 to −1mA	5	5.5	6	V
I_{CC1}	Supply current	V_{CC1} = 5 V,	V_{CC2} open		5	8	mA
I_{CC2}	Supply current	V_{CC2} = 15 V,	V_{CC1} open		7	10	mA

inputs

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage‡	Clock Input				4.5	V
V_{T-}	Negative-going threshold voltage‡			0.4			V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			2	2.6	4	V
I_{IH}	High-level input current	Reset, Enable, and Clock	V_I = 2.4 V		17	35	μA
			V_I = 18 V	130	220	320	
I_{IL}	Low-level input current		V_I = 0			±10	μA
I_I	Analog input current		V_I = 4 V		10	300	nA

output section

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current	V_{OH} = 18 V		0.1	100	μA
I_{OL}	Low-level output current	V_{OL} = 5.5 V	5	10	15	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		80	400	mV

operating characteristics over recommended operating free-air temperature range, V_{CC1} = V_{CC2} = 5.12 V

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Overall error				±80	mV
Differential nonlinearity	See Figure 1			±20	mV
Zero error‡	Binary count = 0			±80	mV
Scale error	Binary count = 127			±80	mV
Full scale input voltage‡	Binary count = 127	3.74	3.82	3.9	V
Propagation delay time from reset or enable			2		μs

†All typical values are at T_A = 25°C.
‡These parameters are linear functions of V_{CC1}.

definitions

zero error

The absolute value of the difference between the actual analog voltage at the 01H-to-00H transition and the ideal analog voltage at that transition.

overall error

The magnitude of the deviation from a straight line between the endpoints of the transfer function.

differential nonlinearity

The maximum deviation of an analog-value change associated with a 1-bit code change (1 clock pulse) from its theoretical value of 1 LSB.

PARAMETER MEASUREMENT INFORMATION

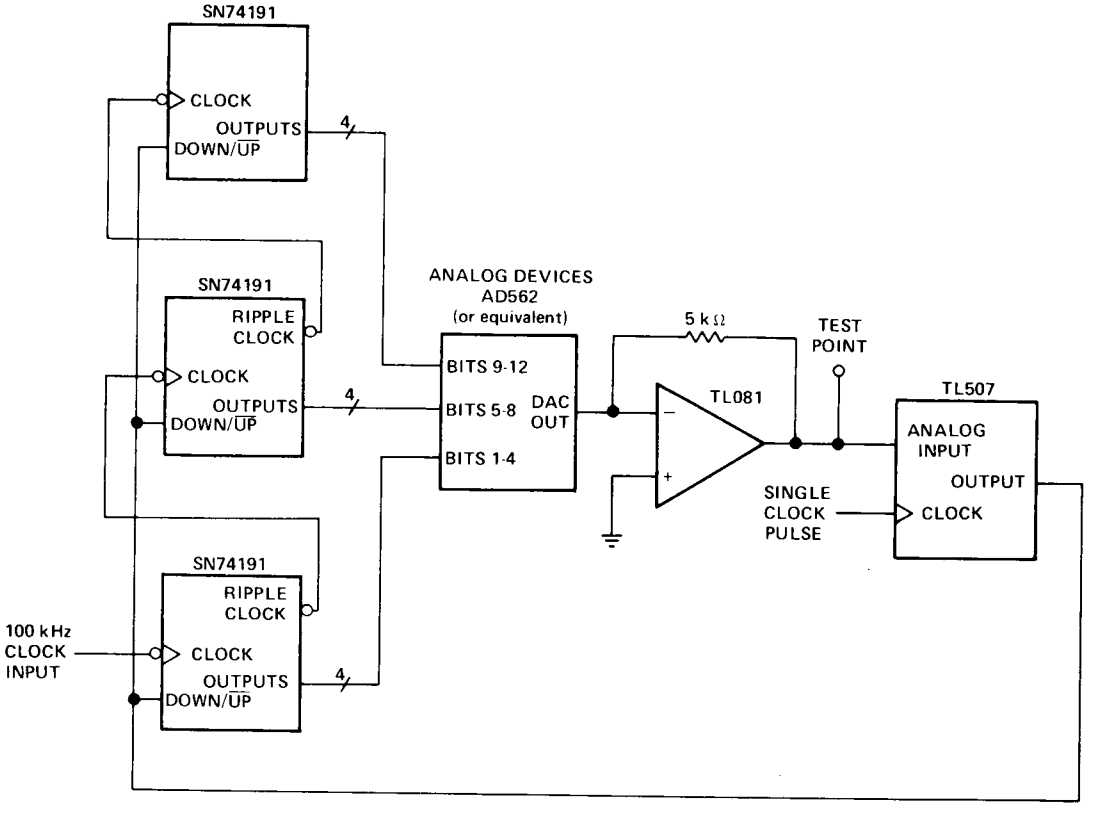


FIGURE 1. MONOTONICITY AND NONLINEARITY TEST CIRCUIT

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PRINCIPLES OF OPERATION

The TL507 is a single-slope analog-to-digital converter. All single-slope converters are basically voltage-to-time or current-to-time converters. A study of the functional block diagram shows the versatility of the TL507.

An external clock signal is applied through a buffer to a negative-edge-triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier used as an adder. The operational amplifier generates a signal that ramps from $0.75 \cdot V_{CC1}$ down to $0.25 \cdot V_{CC1}$. Comparator 1 compares the ramp signal to the analog input signal. Comparator 2 functions as a fault defector. With the analog input voltage in the range $0.25 \cdot V_{CC1}$ to $0.75 \cdot V_{CC1}$, the duty cycle of the output signal is determined by the unknown analog input, as shown in Figure 2 and the Function Table.

For illustration, assume $V_{CC1} = 5.12$ V,

$$0.25 \cdot V_{CC1} = 1.28 \text{ V}$$

$$1 \text{ binary count} = \frac{(0.75 - 0.25)\, V_{CC1}}{128} = 20 \text{ mV}$$

$$0.75 \cdot V_{CC1} - 1 \text{ count} = 3.82 \text{ V}$$

The output is an open-collector n-p-n transistor capable of withstanding up to 18 V in the off state. The output is current limited to the 8- to 12-mA range; however, care must be taken to ensure that the output does not exceed 5.5 V in the on state.

The voltage regulator section allows operation from either an unregulated 8- to 18-V V_{CC2} source or a regulated 3.5- to 6-V V_{CC1} source. Regardless of which external power source is used, the internal circuitry operates at V_{CC1}. When operating from a V_{CC1} source, V_{CC2} may be connected to V_{CC1} or left open. When operating from a V_{CC2} source, V_{CC1} can be used as a reference voltage output.

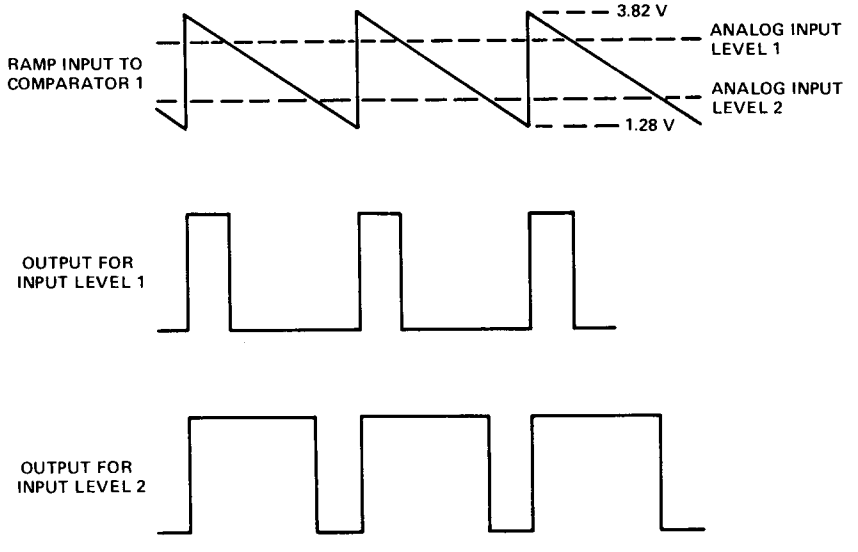

FIGURE 2