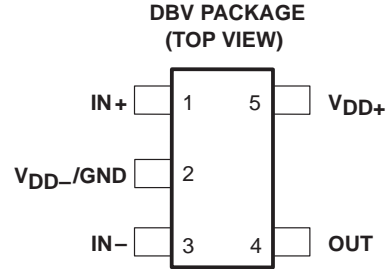


TLV2221, TLV2221Y
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- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Very Low Power . . . 110 μA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**



description

The TLV2221 is a single operational amplifier manufactured using the Texas Instruments Advanced LinCMOS™ process. This device is optimized and fully specified for single-supply 3-V and 5-V operation. For this low-voltage operation combined with micropower dissipation levels, the input noise voltage performance has been dramatically improved using optimized design techniques for CMOS-type amplifiers. Another added benefit is that this amplifier exhibits rail-to-rail output swing. The output dynamic range can be extended using the TLV2221 with loads referenced midway between the rails. The common-mode input voltage range is wider than typical standard CMOS-type amplifiers. To take advantage of this improvement in performance and to make this device available for a wider range of applications, V_{ICR} is specified with a larger maximum input offset voltage test limit of ± 5 mV, allowing a minimum of 0-V to 2-V common-mode input voltage range for a 3-V power supply.

AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM (Y)
		SOT-23 (DBV)†		
0°C to 70°C	3 mV	TLV2221CDBV	VADC	TLV2221Y
-40°C to 85°C	3 mV	TLV2221IDBV	VADI	

† The DBV package available in tape and reel only.

The Advanced LinCMOS process uses a silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. This technology also makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The TLV2221, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the low power dissipation levels combined with 3-V operation, this device works well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split power supplies makes this device an excellent choice when interfacing directly to analog-to-digital converters (ADCs). All of these features combined with its temperature performance make the TLV2221 ideal for remote pressure sensors, temperature control, active voltage-resistive (VR) sensors, accelerometers, hand-held metering devices, and many other applications.



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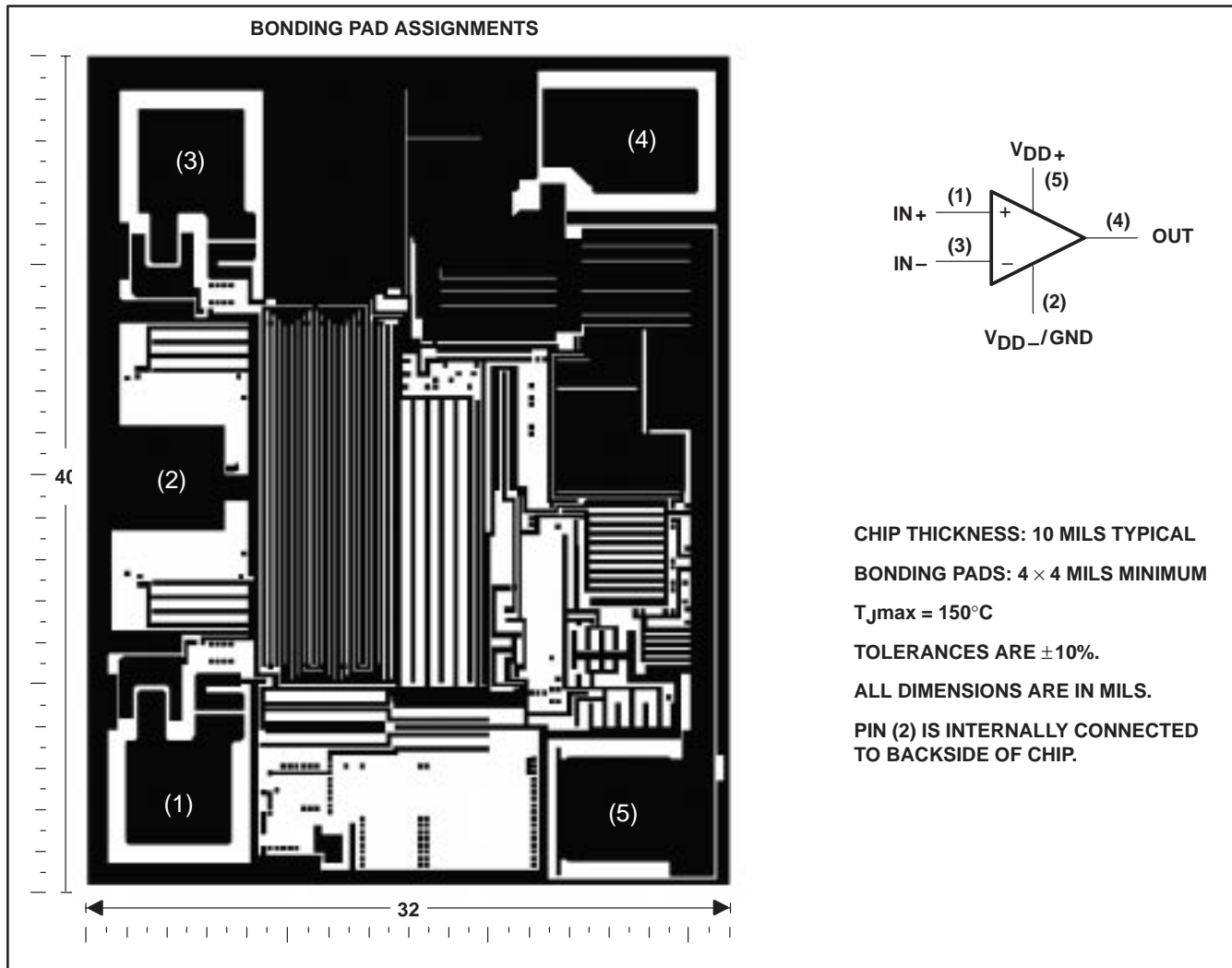
description (continued)

The device inputs and outputs are designed to withstand a 100-mA surge current without sustaining latch-up. In addition, internal ESD-protection circuits prevent functional failures up to 2000 V as tested under MIL-PRF-38535; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. Additional care should be exercised to prevent V_{DD+} supply-line transients under powered conditions. Transients of greater than 20 V can trigger the ESD-protection structure, inducing a low-impedance path to V_{DD-}/GND . Should this condition occur, the sustained current supplied to the device must be limited to 100 mA or less. Failure to do so could result in a latched condition and device failure.



TLV2221Y chip information

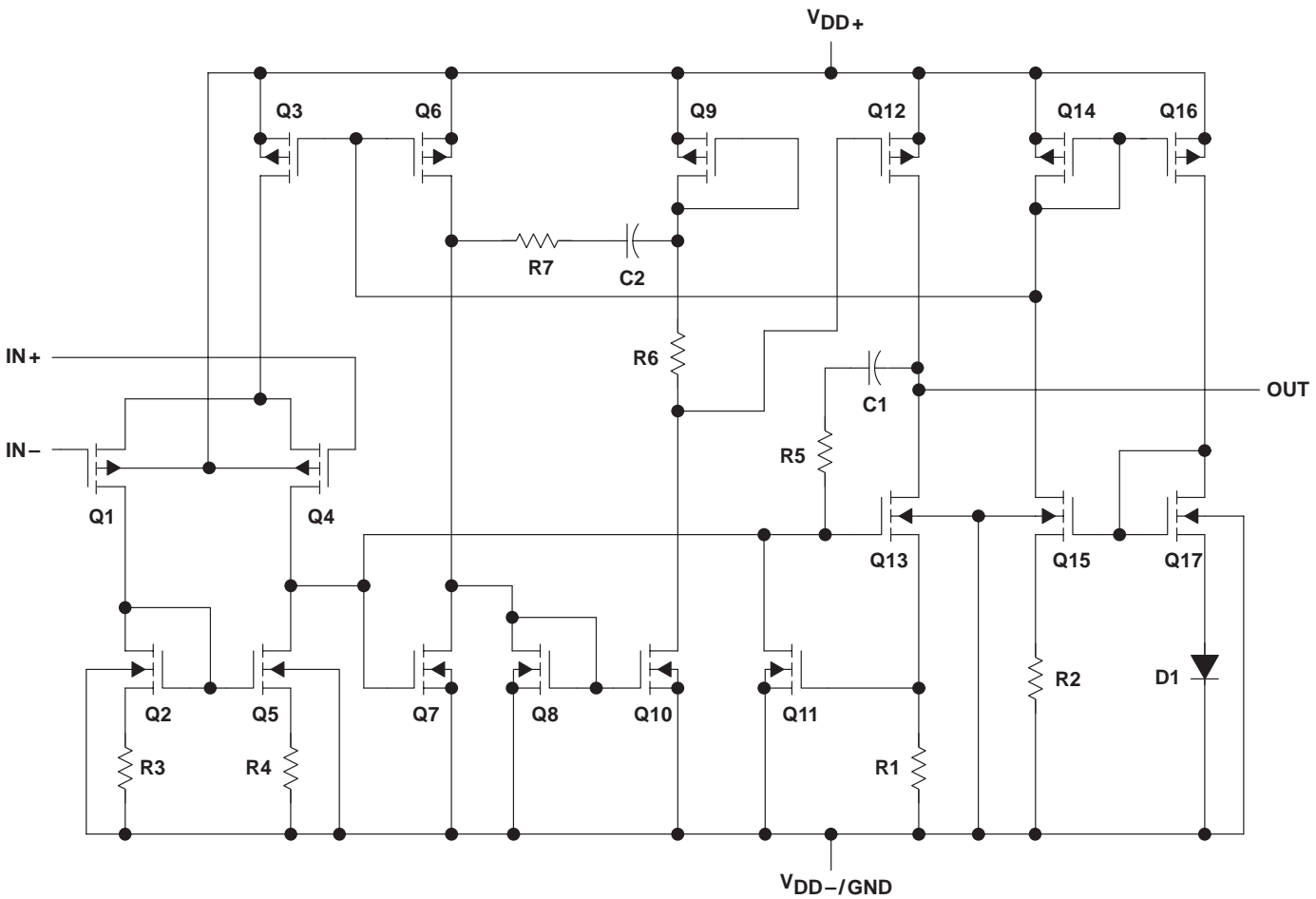
This chip, when properly assembled, displays characteristics similar to the TLV2221C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.



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COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

equivalent schematic

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : TLV2221C	0°C to 70°C
TLV2221I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to V_{DD-} .
 2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
 3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2221C		TLV2221I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-} .

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electrical characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2221C			TLV2221I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	Full range	0.62		3	0.62		3	mV
α_{VIO} Temperature coefficient of input offset voltage			1		1		$\mu\text{V}/^\circ\text{C}$		
Input offset voltage long-term drift (see Note 4)		25°C	0.003		0.003		$\mu\text{V}/\text{mo}$		
I_{IO} Input offset current		25°C	0.5		0.5		pA		
		Full range	150		150				
I_{IB} Input bias current	25°C	1		1		pA			
	Full range	150		150					
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 2	-0.3 to 2.2	0 to 2	-0.3 to 2.2	V		
		Full range	0 to 1.7	0 to 1.7	0 to 1.7	0 to 1.7			
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -400\ \mu\text{A}$	25°C	2.97		2.97		V		
		25°C	2.88		2.88				
		Full range	2.5		2.5				
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	15		15		mV		
		25°C	150		150				
		Full range	500		500				
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 1.5\text{ V}$, $V_O = 1\text{ V to } 2\text{ V}$	25°C	$R_L = 2\text{ k}\Omega$ ‡	2	3	2	3	V/mV	
			Full range	1		1			
		25°C	$R_L = 1\text{ M}\Omega$ ‡		250		250		
r_{id} Differential input resistance		25°C	10^{12}		10^{12}		Ω		
r_{ic} Common-mode input resistance		25°C	10^{12}		10^{12}		Ω		
C_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	6		6		pF		
z_o Closed-loop output impedance	$f = 10\text{ kHz}$, $A_V = 10$	25°C	90		90		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	82	70	82	dB		
		Full range	65		65				
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95	80	95	dB		
		Full range	80		80				
I_{DD} Supply current	$V_O = 1.5\text{ V}$, No load	25°C	100	150	100	150	μA		
		Full range	200		200				

† Full range for the TLV2221C is 0°C to 70°C. Full range for the TLV2221I is -40°C to 85°C.

‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2221C			TLV2221I			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
SR	Slew rate at unity gain $V_O = 1.1\text{ V to }1.9\text{ V}$, $R_L = 2\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	0.1	0.18		0.1	0.18		V/ μs	
		Full range	0.05			0.05				
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C	120			120			nV/ $\sqrt{\text{Hz}}$	
		25°C	20			20				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C	680			680			mV	
		25°C	860			860				
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$	
THD+N	$V_O = 1\text{ V to }2\text{ V}$, $f = 20\text{ kHz}$, $R_L = 2\text{ k}\Omega$ ‡	$A_V = 1$	25°C	2.52%			2.52%			
		$A_V = 10$		7.01%			7.01%			
	$V_O = 1\text{ V to }2\text{ V}$, $f = 20\text{ kHz}$, $R_L = 2\text{ k}\Omega$ §	$A_V = 1$	25°C	0.076%			0.076%			
		$A_V = 10$		0.147%			0.147%			
Gain-bandwidth product	$f = 1\text{ kHz}$, $R_L = 2\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	480			480			kHz	
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 1\text{ V}$, $R_L = 2\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C	30			30			kHz	
t_s	Settling time $A_V = -1$, Step = $1\text{ V to }2\text{ V}$, $R_L = 2\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	To 0.1%	25°C	4.5			4.5			μs
		To 0.01%	25°C	6.8			6.8			μs
ϕ_m	Phase margin at unity gain $R_L = 2\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	51°			51°				
		25°C	12			12			dB	

† Full range is -40°C to 85°C .

‡ Referenced to 1.5 V

§ Referenced to 0 V

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLV2221C			TLV2221I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD\pm} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	Full range	0.61 3			0.61 3			mV
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage			1			1			$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C	0.5			0.5			pA
I_{IB} Input bias current		Full range	150			150			
	25°C	1			1			pA	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2	0 to 4	-0.3 to 4.2	V		
		Full range	0 to 3.5		0 to 3.5				
V_{OH} High-level output voltage	$I_{OH} = -500\ \mu\text{A}$	25°C	4.75	4.88	4.75	4.88	V		
	$I_{OH} = -1\text{ mA}$		4.5	4.76	4.5	4.76			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C	12			12			mV
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C	120			120			
		Full range	500			500			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	25°C	$R_L = 2\text{ k}\Omega$ ‡		3 5		V/mV		
			Full range		1				
		25°C	$R_L = 1\text{ M}\Omega$ ‡		800		800		
r_{id} Differential input resistance		25°C	10 ¹²			10 ¹²			Ω
r_{ic} Common-mode input resistance		25°C	10 ¹²			10 ¹²			Ω
C_{ic} Common-mode input capacitance	$f = 10\text{ kHz}$	25°C	6			6			pF
z_o Closed-loop output impedance	$f = 10\text{ kHz}$, $A_V = 10$	25°C	70			70			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 1.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	85	70	85	dB		
		Full range	65			65			
kSVR Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }8\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95	80	95	dB		
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C	110	150	110	150	μA		
		Full range	200			200			

† Full range for the TLV2221C is 0°C to 70°C. Full range for the TLV2221I is -40°C to 85°C.

‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLV2221C			TLV2221I			UNIT		
			MIN	TYP	MAX	MIN	TYP	MAX			
SR	Slew rate at unity gain $V_O = 1.5\text{ V to }3.5\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	0.1	0.18		0.1	0.18		V/ μs		
		Full range	0.05			0.05					
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$	25°C	90			90			nV/ $\sqrt{\text{Hz}}$		
		$f = 1\text{ kHz}$	19			19					
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$	25°C	800			800			mV		
		$f = 0.1\text{ Hz to }10\text{ Hz}$	960			960					
I_n	Equivalent input noise current	25°C	0.6			0.6			fA/ $\sqrt{\text{Hz}}$		
THD+N	Total harmonic distortion plus noise $V_O = 1.5\text{ V to }3.5\text{ V}, f = 20\text{ kHz}, R_L = 2\text{ k}\Omega^\ddagger$	25°C	$A_V = 1$	2.45%			2.45%				
			$A_V = 10$	5.54%			5.54%				
		25°C	$V_O = 1.5\text{ V to }3.5\text{ V}, f = 20\text{ kHz}, R_L = 2\text{ k}\Omega^\S$	$A_V = 1$	0.142%			0.142%			
			$A_V = 10$	0.257%			0.257%				
Gain-bandwidth product	$f = 1\text{ kHz}, C_L = 100\text{ pF}^\ddagger, R_L = 2\text{ k}\Omega^\ddagger$	25°C	510			510			kHz		
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 1\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, A_V = 1, C_L = 100\text{ pF}^\ddagger$	25°C	40			40			kHz		
t_s	Settling time $A_V = -1, \text{ Step} = 1.5\text{ V to }3.5\text{ V}, R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	To 0.1%	6.8			6.8			μs	
		25°C	To 0.01%	9.2			9.2				
ϕ_m	Phase margin at unity gain $R_L = 2\text{ k}\Omega^\ddagger, C_L = 100\text{ pF}^\ddagger$	25°C	52°			52°					
	Gain margin	25°C	12			12			dB		

† Full range is -40°C to 85°C .

‡ Referenced to 2.5 V

§ Referenced to 0 V

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electrical characteristics at $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2221Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	620			μV
I_{IO} Input offset current		0.5			pA
I_{IB} Input bias current		1			pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	-0.3 to 2.2			V
V_{OH} High-level output voltage	$I_{OH} = -100\ \mu\text{A}$	2.97			V
V_{OL} Low-level output voltage	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	15			mV
	$V_{IC} = 1.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	150			
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to } 2\text{ V}$	$R_L = 2\ \text{k}\Omega^\dagger$	3		V/mV
		$R_L = 1\ \text{M}\Omega^\dagger$	250		
r_{id} Differential input resistance		10^{12}			Ω
r_{ic} Common-mode input resistance		10^{12}			Ω
c_{ic} Common-mode input capacitance	$f = 10\ \text{kHz}$	6			pF
z_o Closed-loop output impedance	$f = 10\ \text{kHz}$, $A_V = 10$	90			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$	82			dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = 0$, No load	95			dB
I_{DD} Supply current	$V_O = 0$, No load	100			μA

† Referenced to 1.5 V

electrical characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TLV2221Y			UNIT
		MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 1.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	610			μV
I_{IO} Input offset current		0.5			pA
I_{IB} Input bias current		1			pA
V_{ICR} Common-mode input voltage range	$ V_{IO} \leq 5\text{ mV}$, $R_S = 50\ \Omega$	-0.3 to 4.2			V
V_{OH} High-level output voltage	$I_{OH} = -500\ \mu\text{A}$	4.88			V
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	12			mV
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	120			
A_{VD} Large-signal differential voltage amplification	$V_O = 1\text{ V to } 4\text{ V}$	$R_L = 2\ \text{k}\Omega^\dagger$	5		V/mV
		$R_L = 1\ \text{M}\Omega^\dagger$	800		
r_{id} Differential input resistance		10^{12}			Ω
r_{ic} Common-mode input resistance		10^{12}			Ω
c_{ic} Common-mode input capacitance	$f = 10\ \text{kHz}$	6			pF
z_o Closed-loop output impedance	$f = 10\ \text{kHz}$, $A_V = 10$	70			Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to } 1.7\text{ V}$, $V_O = 0$, $R_S = 50\ \Omega$	85			dB
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7\text{ V to } 8\text{ V}$, $V_{IC} = 0$, No load	95			dB
I_{DD} Supply current	$V_O = 0$, No load	110			μA

† Referenced to 2.5 V



TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage
		1, 2 3, 4
α_{VIO}	Input offset voltage temperature coefficient	Distribution
		5, 6
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature
		7
V_I	Input voltage	vs Supply voltage vs Free-air temperature
		8 9
V_{OH}	High-level output voltage	vs High-level output current
		10, 13
V_{OL}	Low-level output voltage	vs Low-level output current
		11, 12, 14
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency
		15
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature
		16 17
V_O	Output voltage	vs Differential input voltage
		18, 19
A_{VD}	Differential voltage amplification	vs Load resistance
		20
A_{VD}	Large signal differential voltage amplification	vs Frequency vs Free-air temperature
		21, 22 23, 24
z_o	Output impedance	vs Frequency
		25, 26
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature
		27 28
kSVR	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature
		29, 30 31
I_{DD}	Supply current	vs Supply voltage
		32
SR	Slew rate	vs Load capacitance vs Free-air temperature
		33 34
V_O	Inverting large-signal pulse response	vs Time
		35, 36
V_O	Voltage-follower large-signal pulse response	vs Time
		37, 38
V_O	Inverting small-signal pulse response	vs Time
		39, 40
V_O	Voltage-follower small-signal pulse response	vs Time
		41, 42
V_n	Equivalent input noise voltage	vs Frequency
		43, 44
	Input noise voltage (referred to input)	Over a 10-second period
		45
THD + N	Total harmonic distortion plus noise	vs Frequency
		46
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage
		47 48
ϕ_m	Phase margin	vs Frequency vs Load capacitance
		21, 22 51, 52
	Gain margin	vs Load capacitance
		49, 50
B_1	Unity-gain bandwidth	vs Load capacitance
		53, 54

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2221
 INPUT OFFSET VOLTAGE

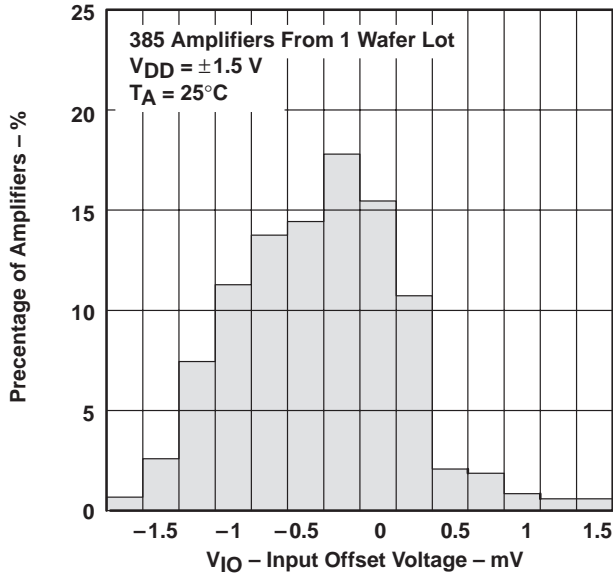


Figure 1

DISTRIBUTION OF TLV2221
 INPUT OFFSET VOLTAGE

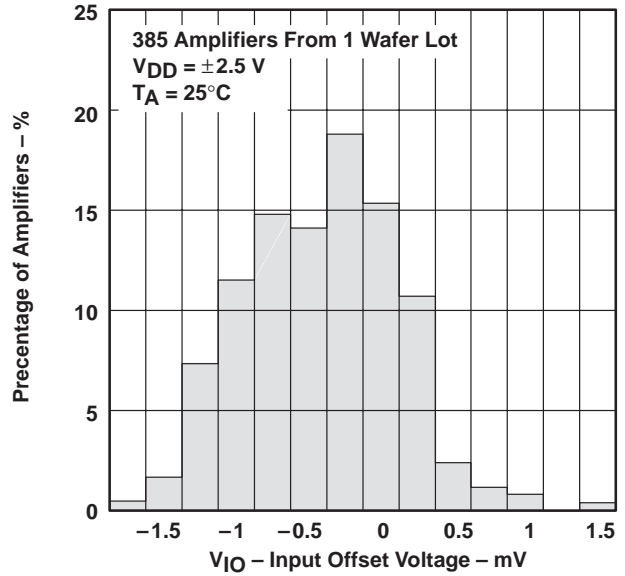


Figure 2

INPUT OFFSET VOLTAGE†
 vs
 COMMON-MODE INPUT VOLTAGE

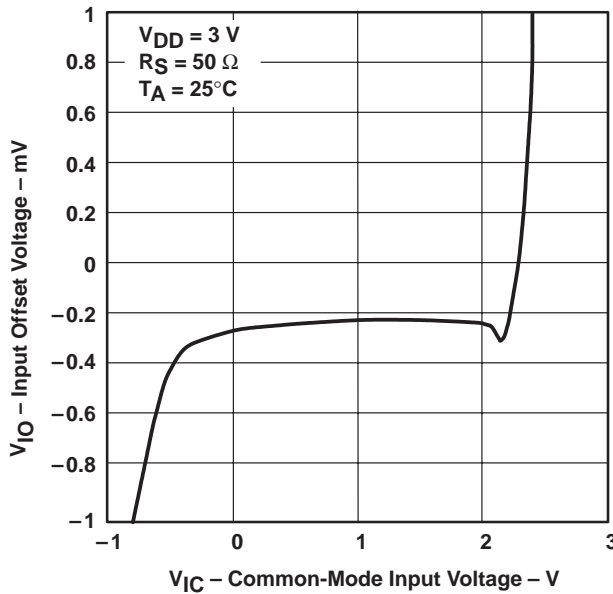


Figure 3

INPUT OFFSET VOLTAGE†
 vs
 COMMON-MODE INPUT VOLTAGE

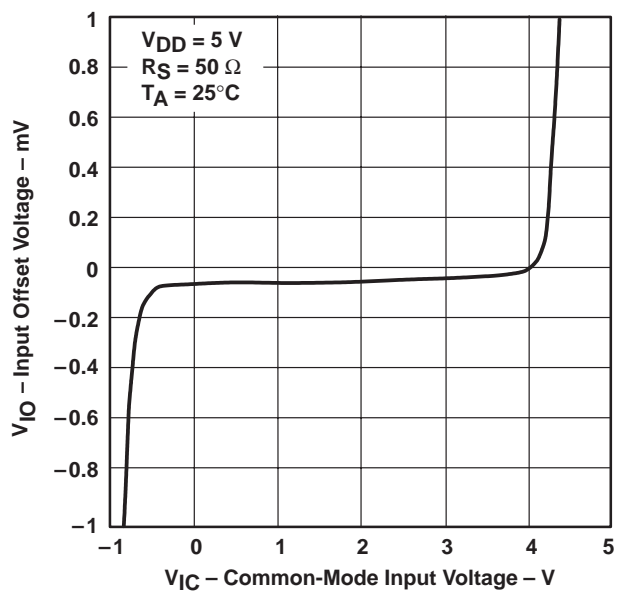
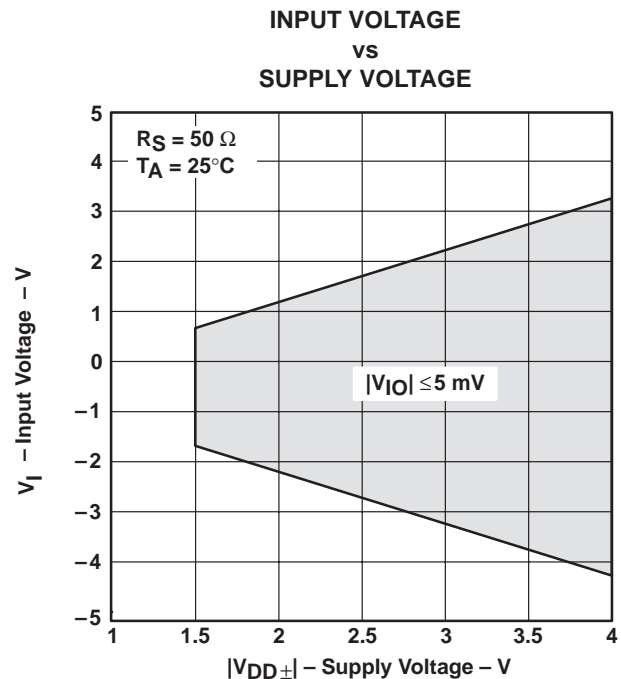
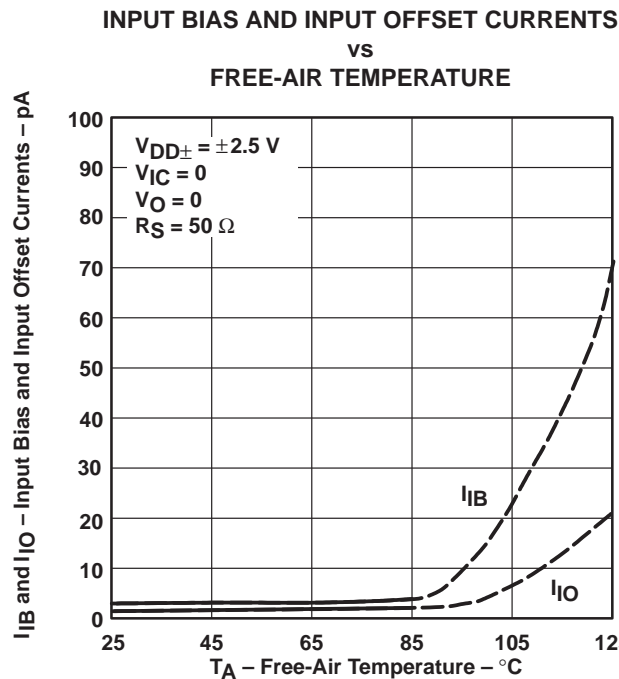
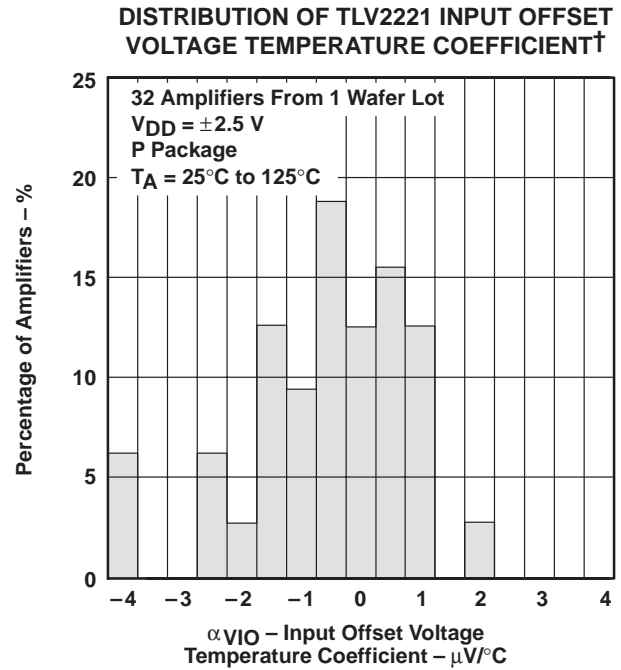
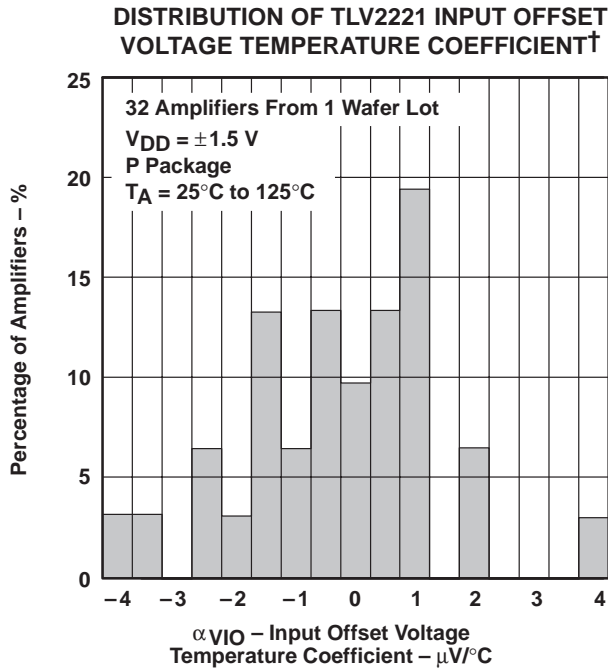


Figure 4

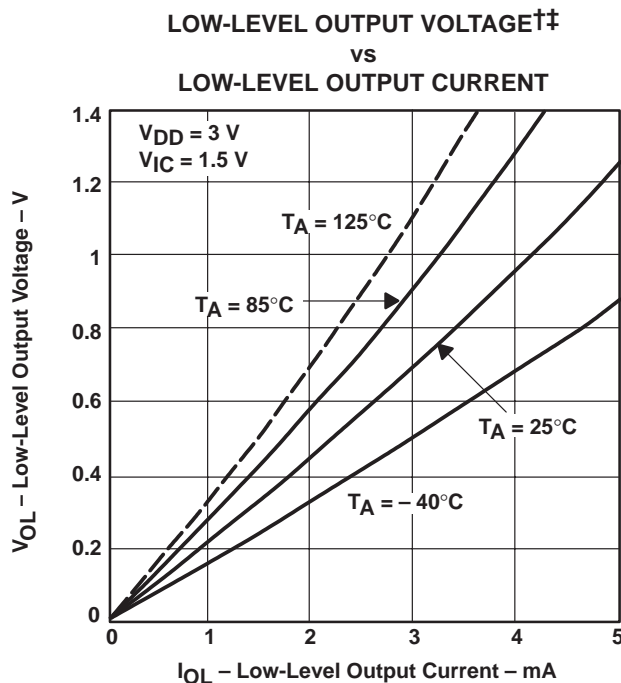
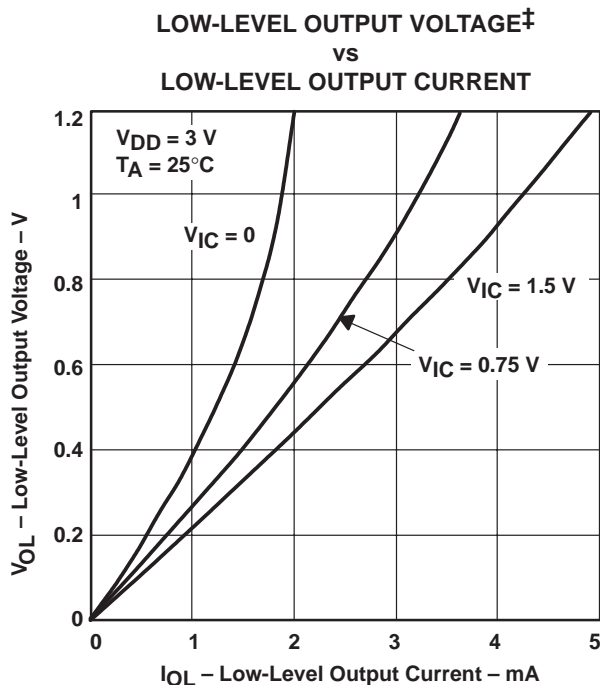
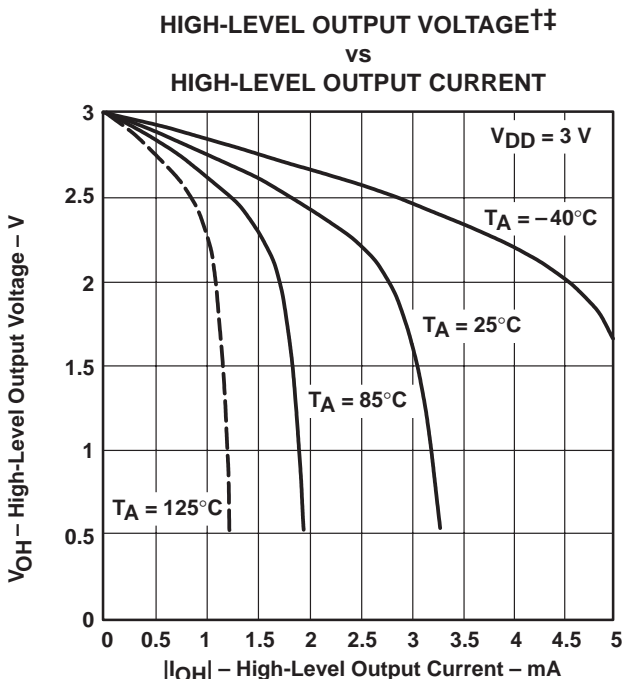
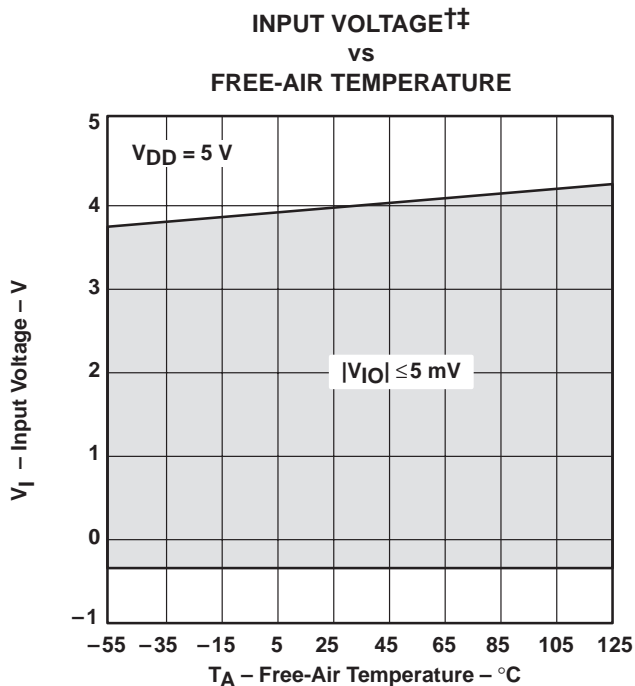
† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



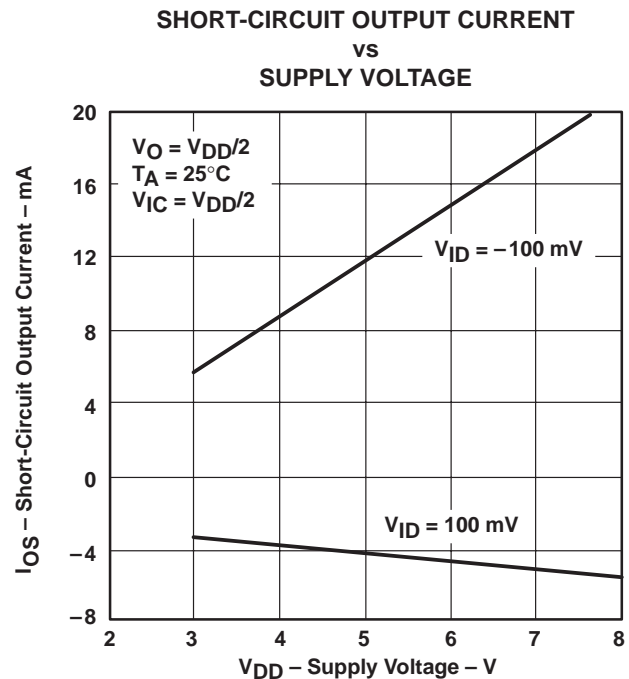
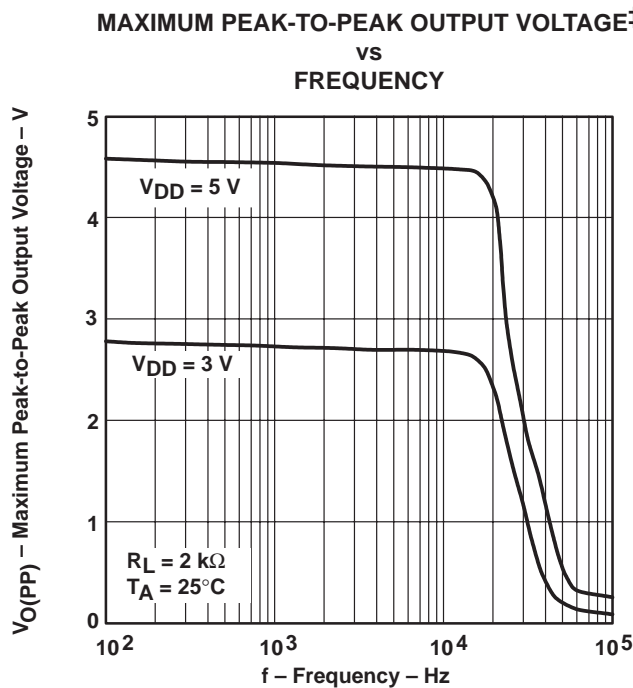
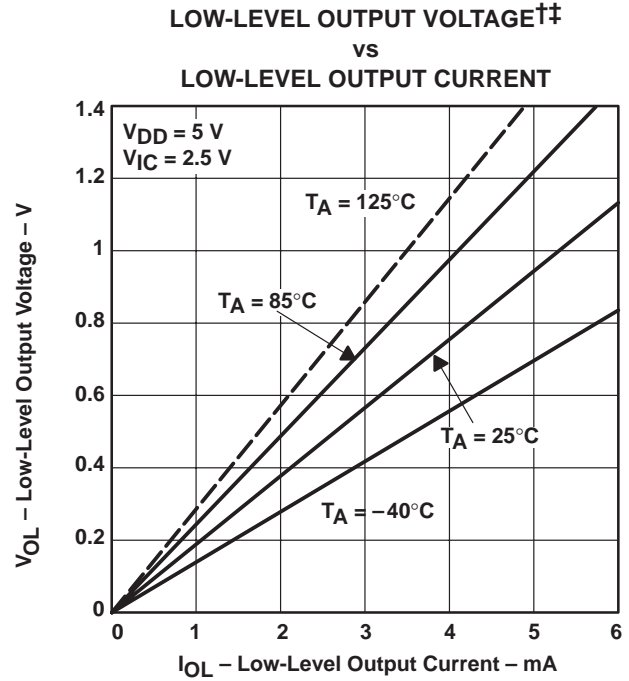
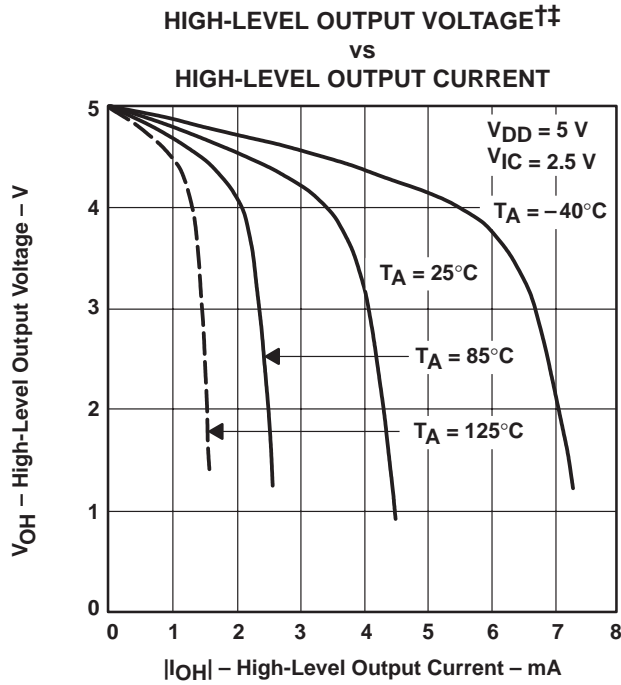
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V . For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V .

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

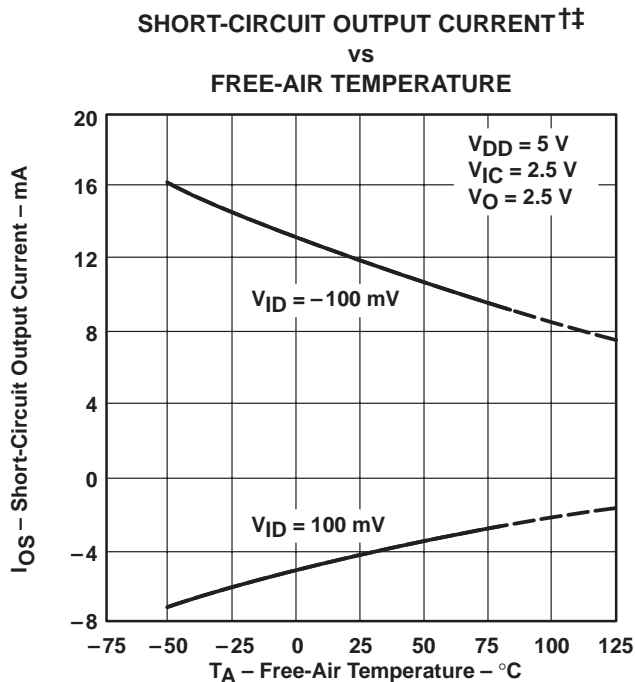


Figure 17

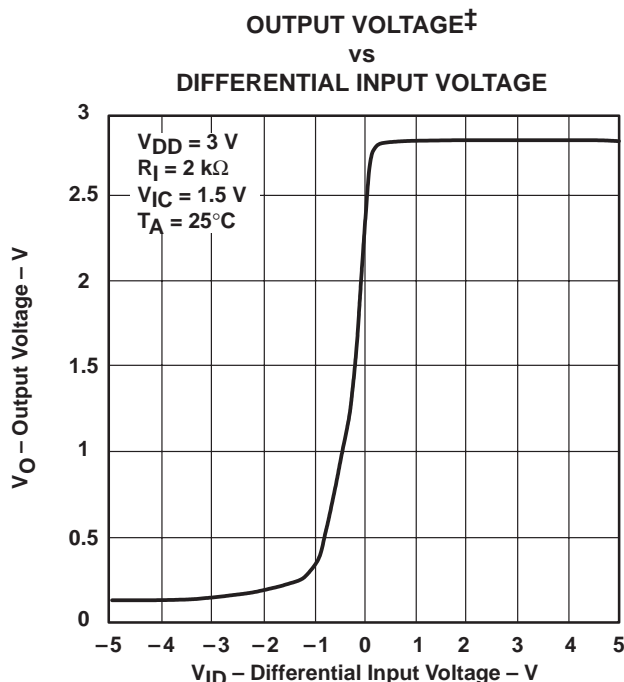


Figure 18

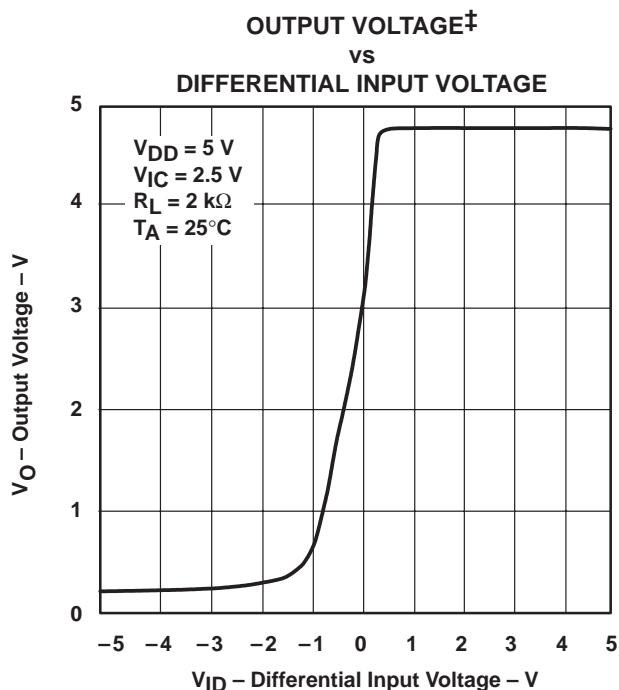


Figure 19

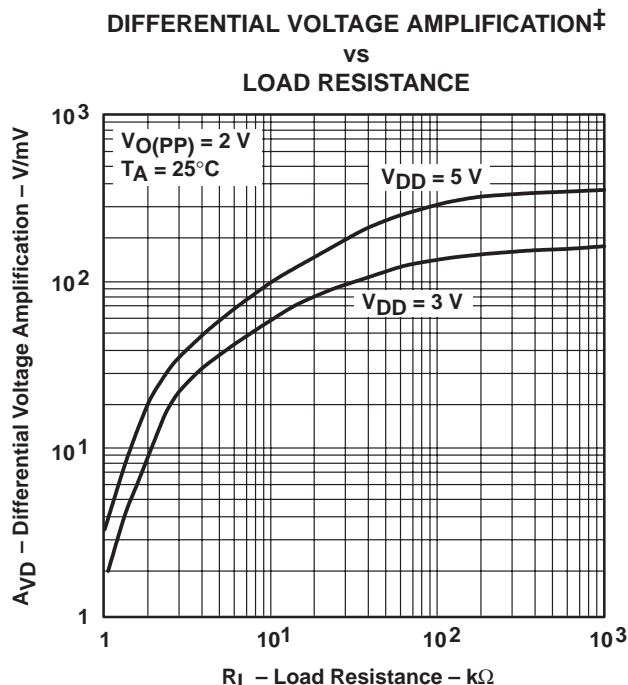


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE†
 AMPLIFICATION AND PHASE MARGIN
 VS
 FREQUENCY**

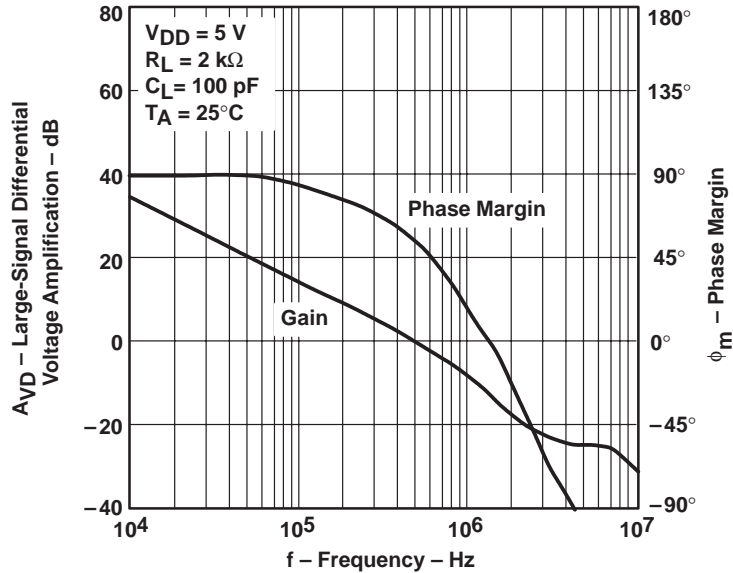


Figure 21

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
 AMPLIFICATION AND PHASE MARGIN†
 VS
 FREQUENCY**

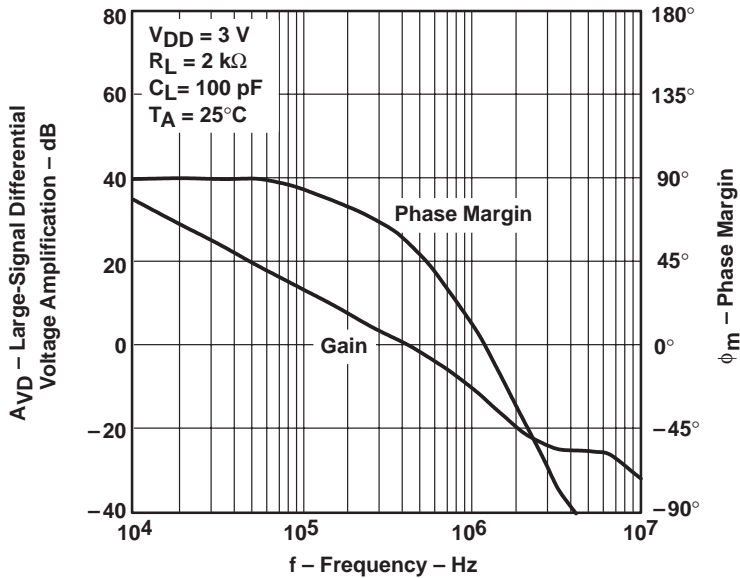


Figure 22

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION†‡
 vs
 FREE-AIR TEMPERATURE

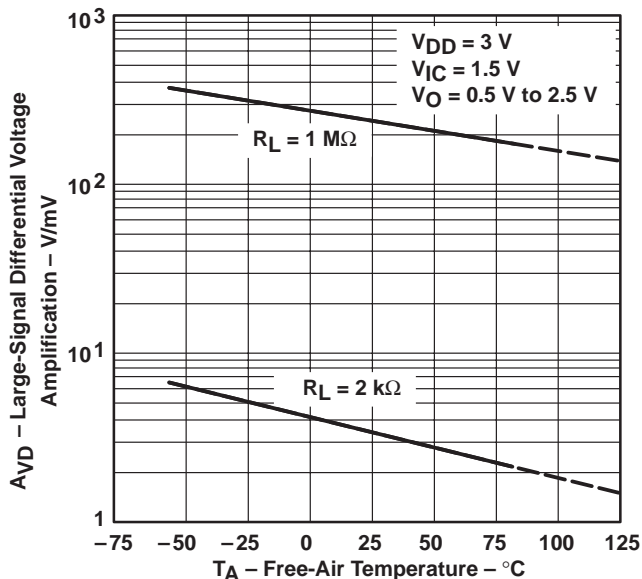


Figure 23

LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION†‡
 vs
 FREE-AIR TEMPERATURE

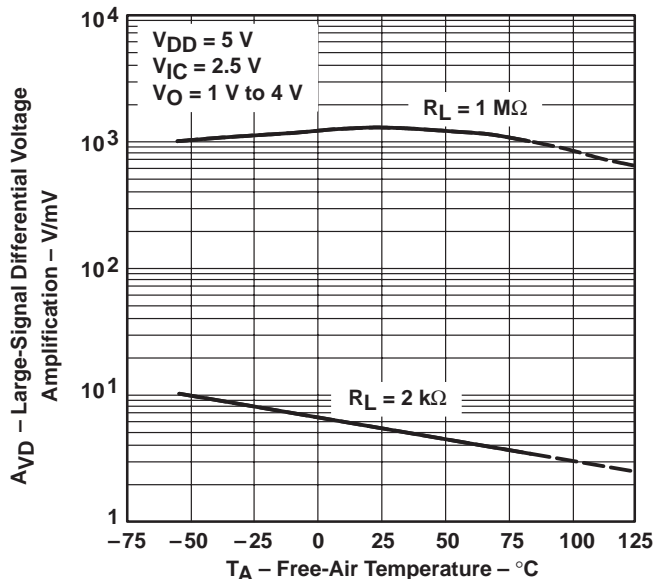


Figure 24

OUTPUT IMPEDANCE†‡
 vs
 FREQUENCY

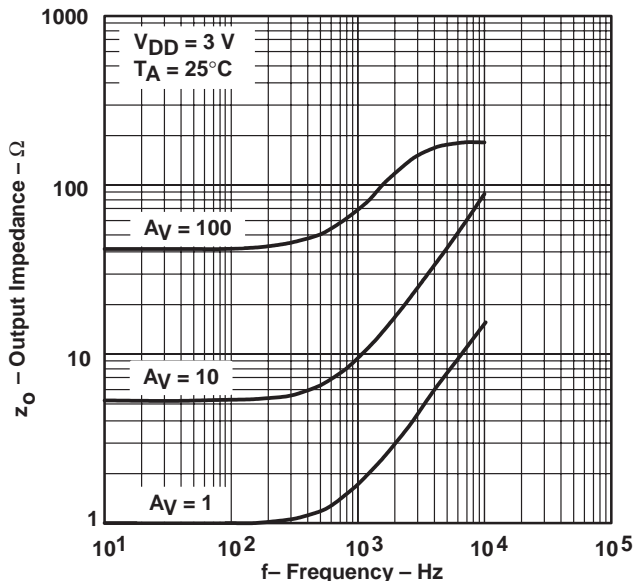


Figure 25

OUTPUT IMPEDANCE†‡
 vs
 FREQUENCY

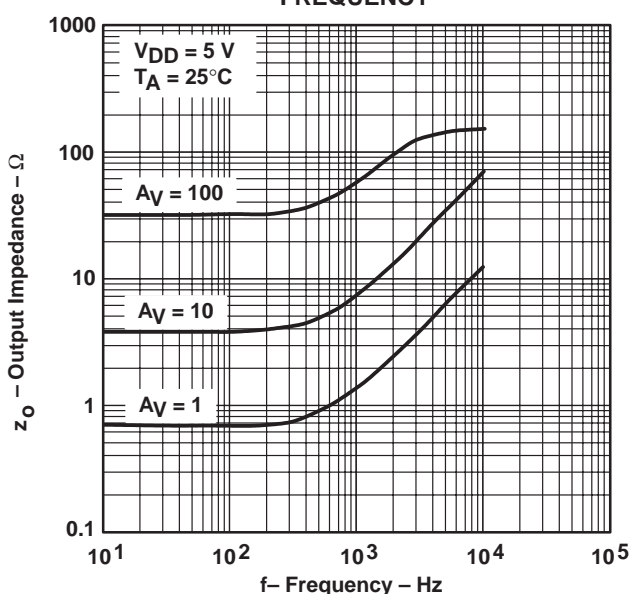
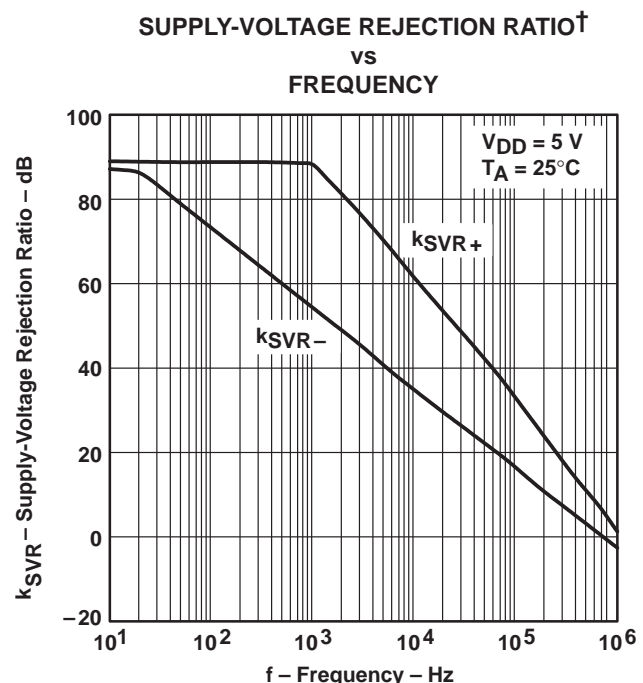
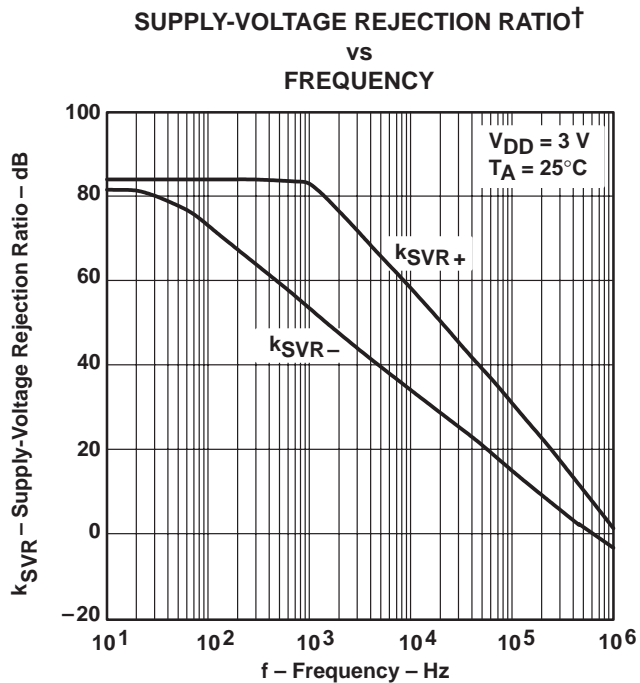
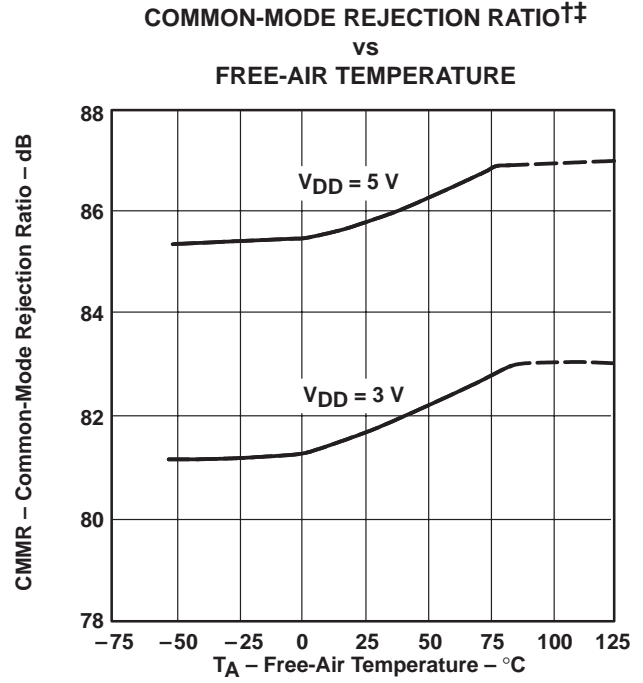
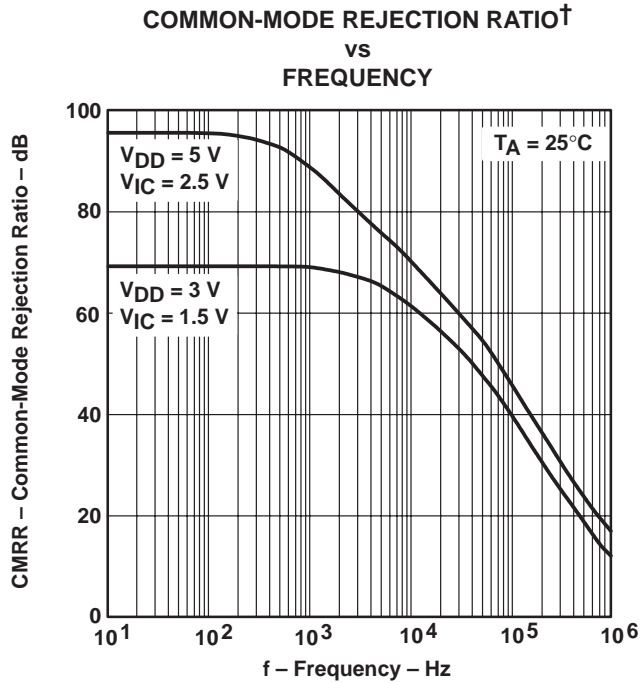


Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where VDD = 5 V, all loads are referenced to 2.5 V. For all curves where VDD = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.
 ‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

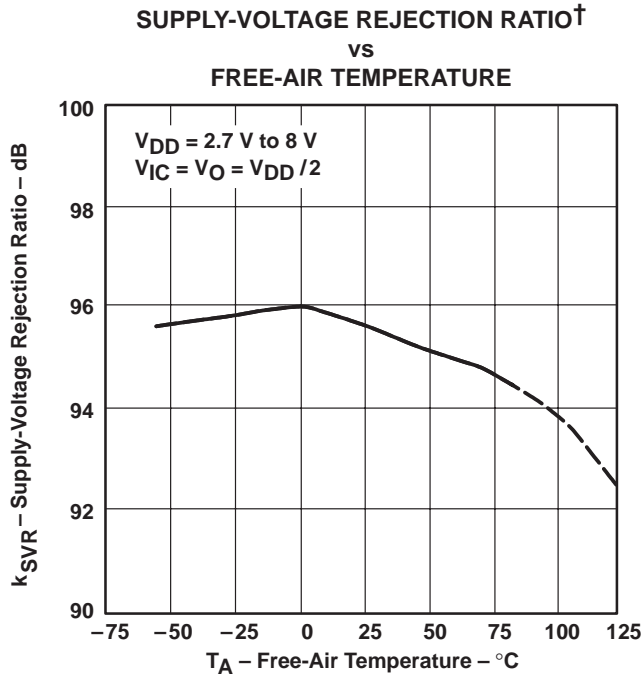


Figure 31

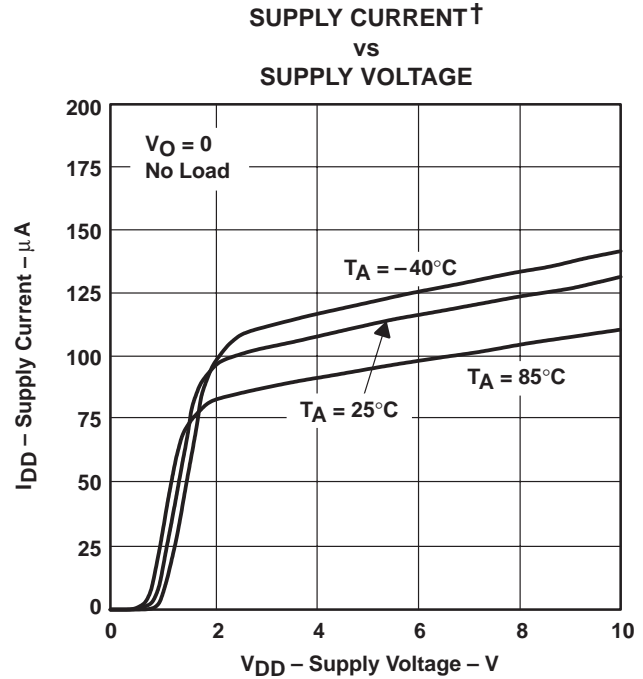


Figure 32

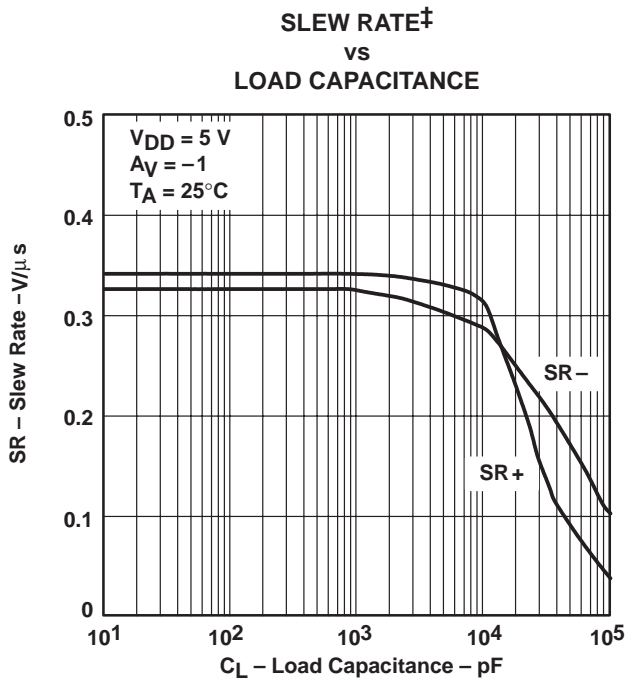


Figure 33

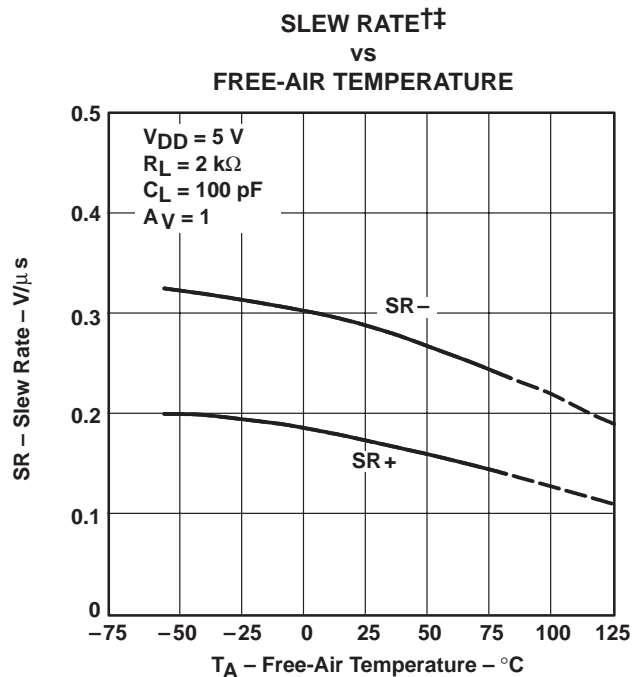


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3 \text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

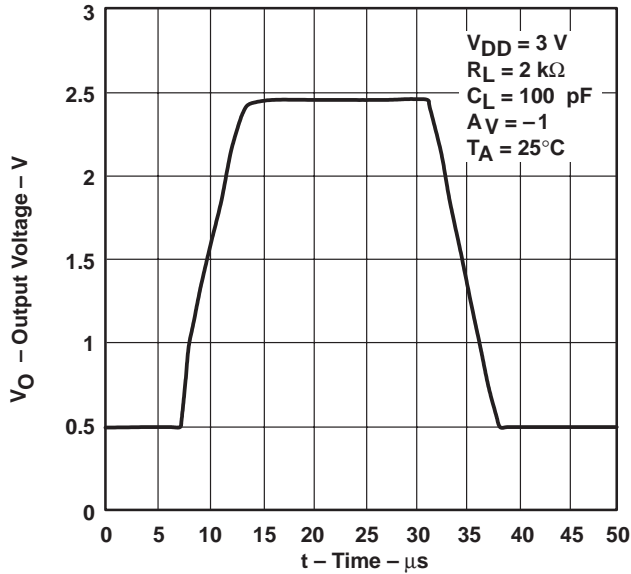


Figure 35

INVERTING LARGE-SIGNAL PULSE RESPONSE†

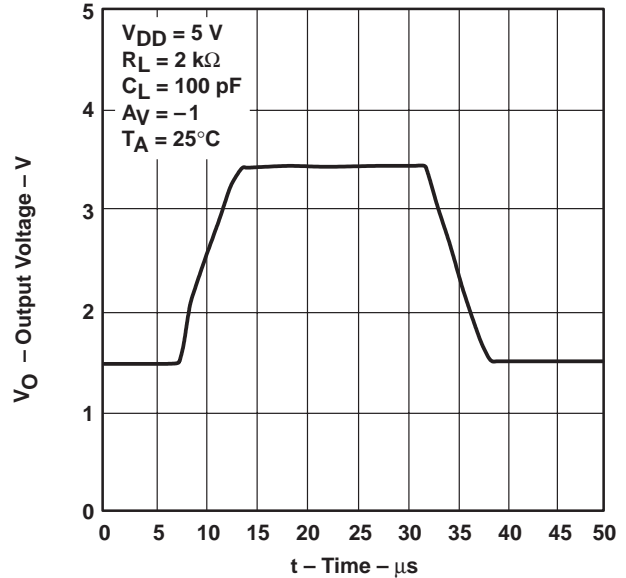


Figure 36

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

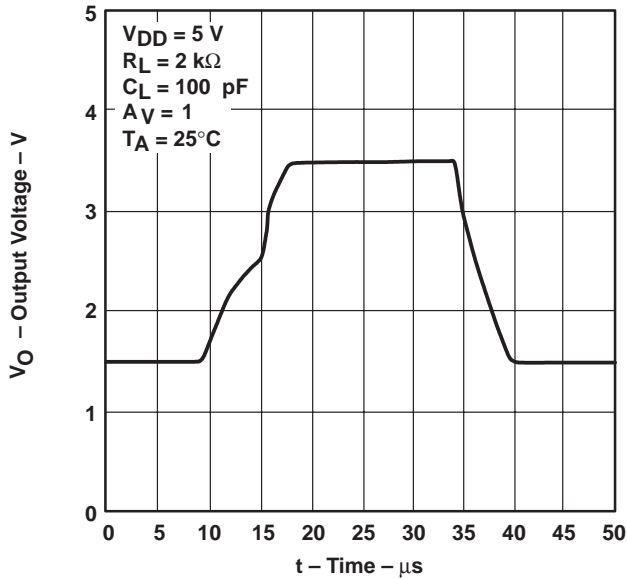


Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

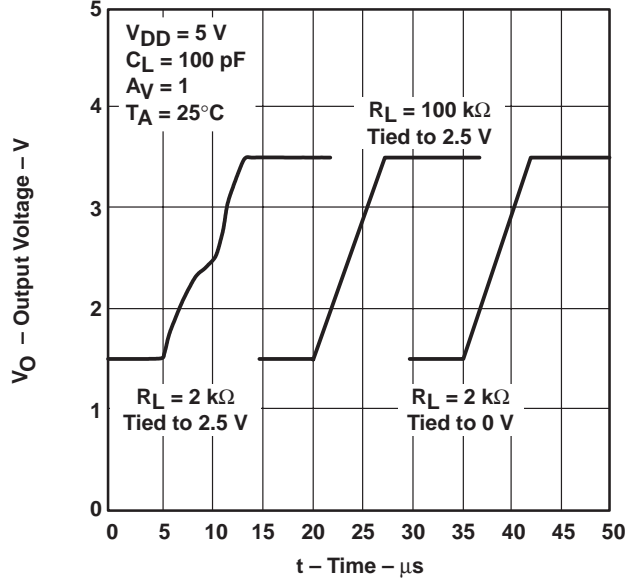


Figure 38

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL
 PULSE RESPONSE†

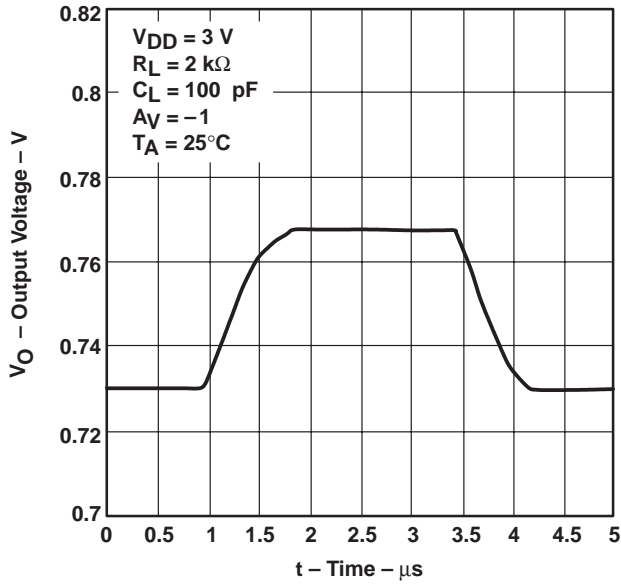


Figure 39

INVERTING SMALL-SIGNAL
 PULSE RESPONSE†

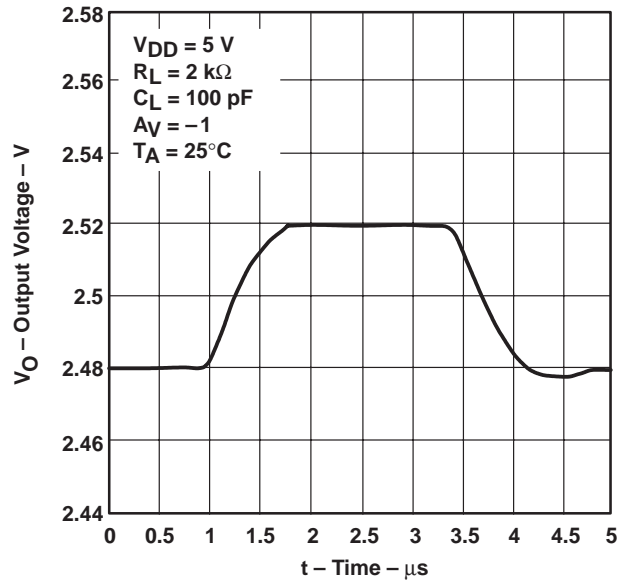


Figure 40

VOLTAGE-FOLLOWER SMALL-SIGNAL
 PULSE RESPONSE†

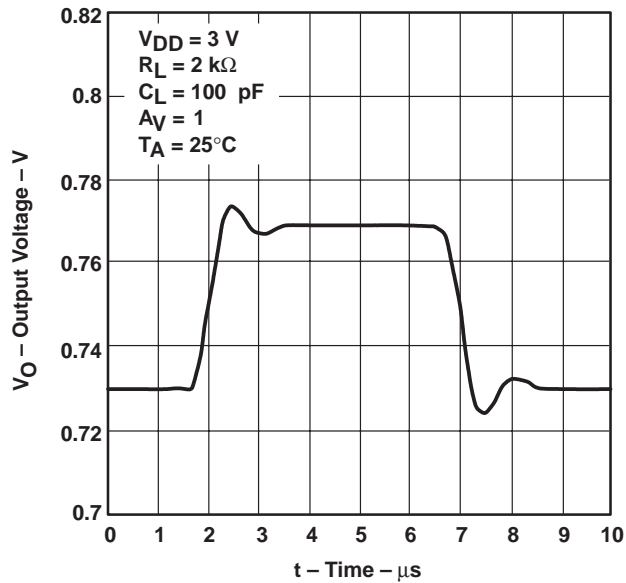


Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
 PULSE RESPONSE†

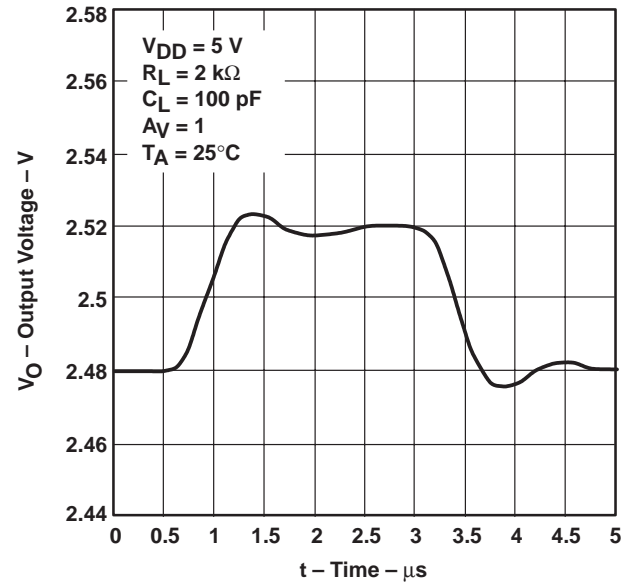
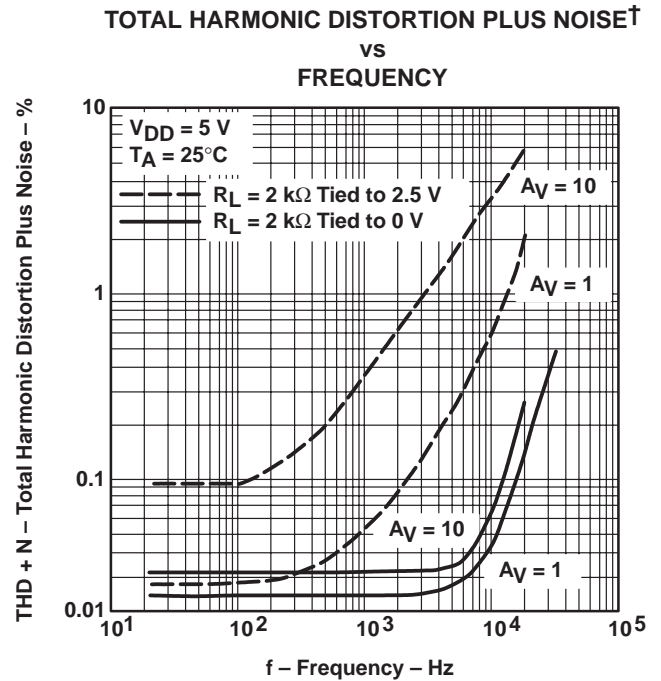
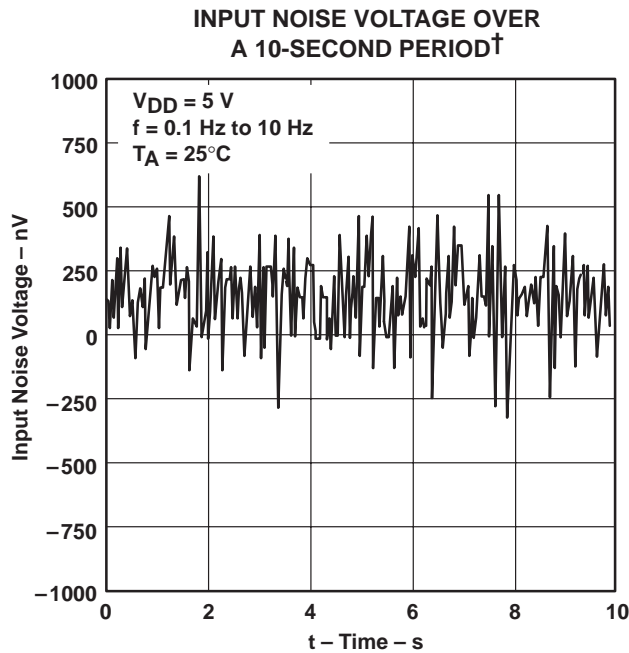
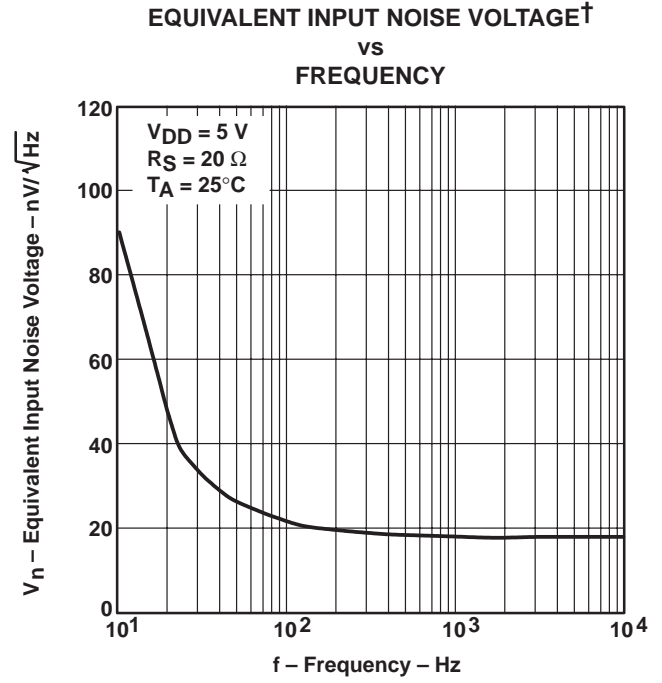
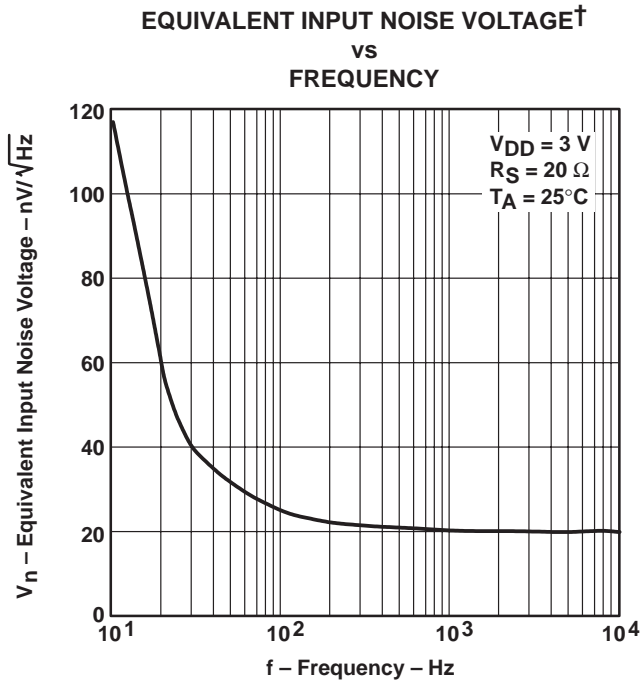


Figure 42

† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



† For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

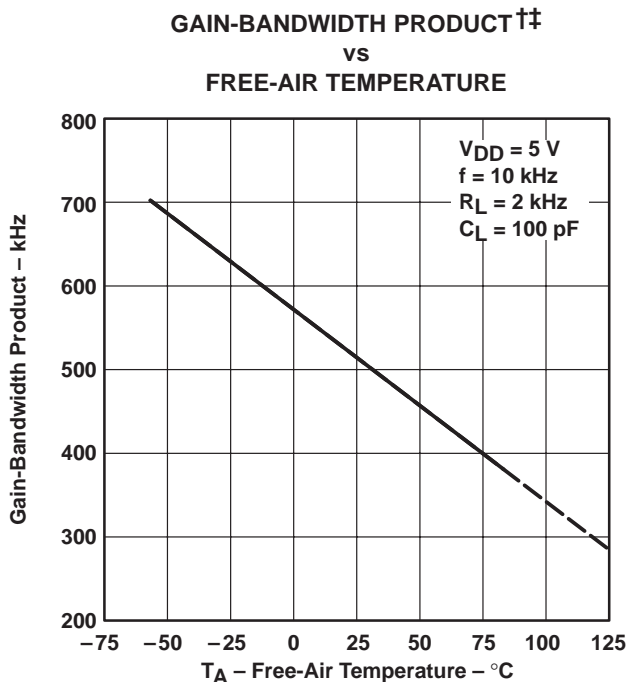


Figure 47

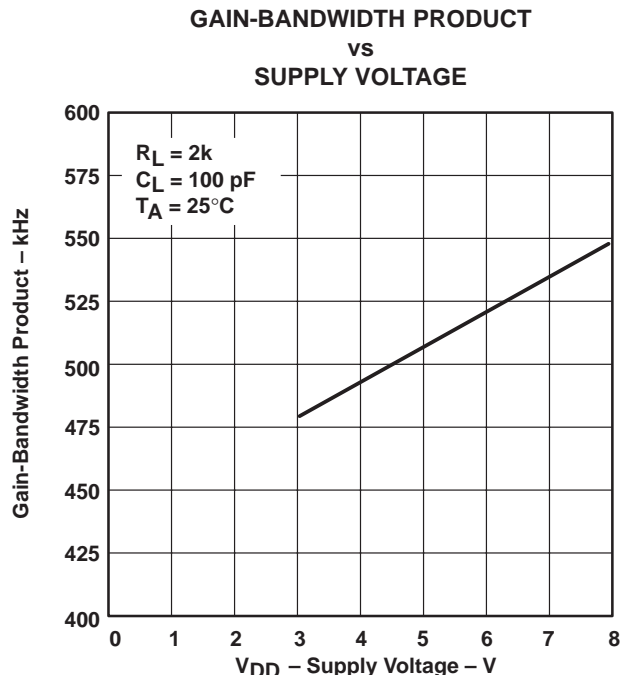


Figure 48

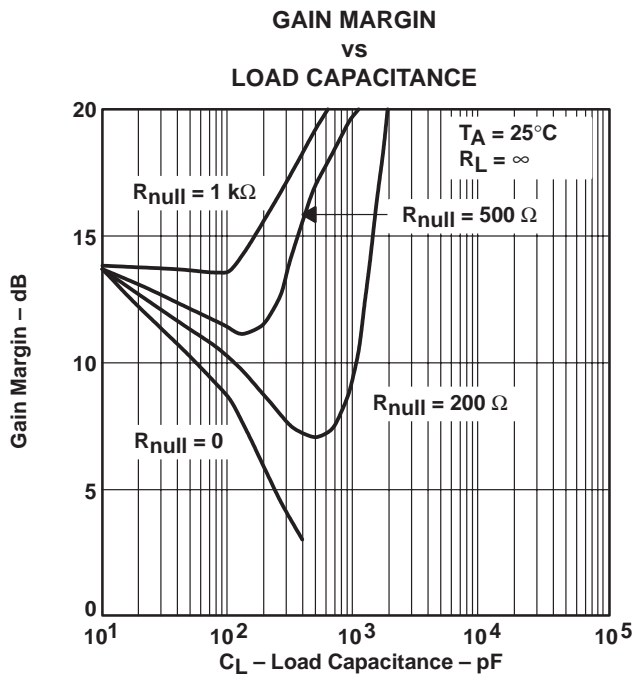


Figure 49

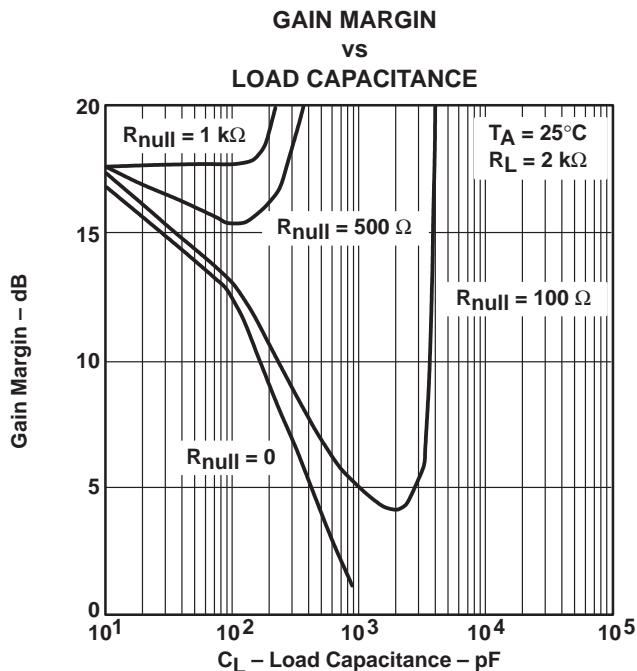
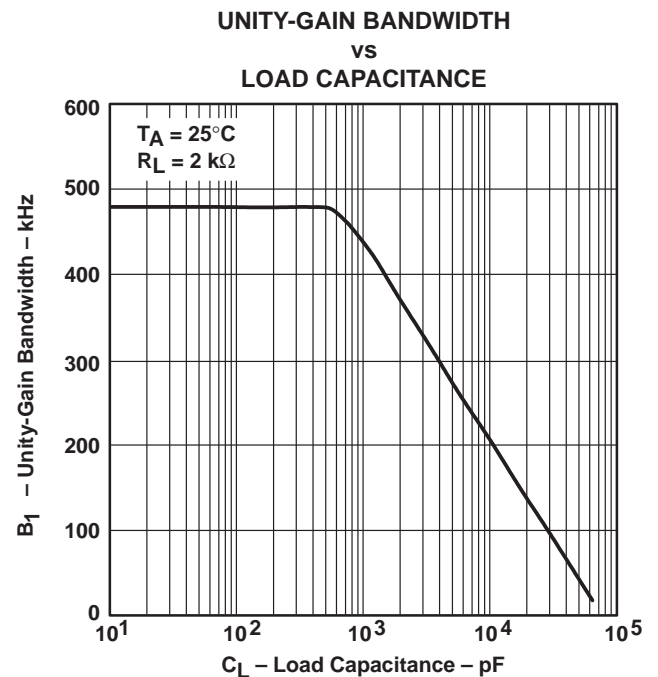
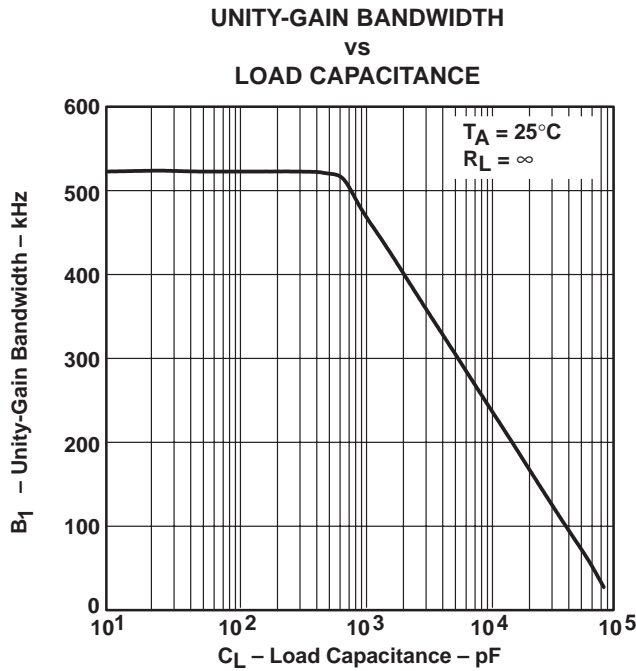
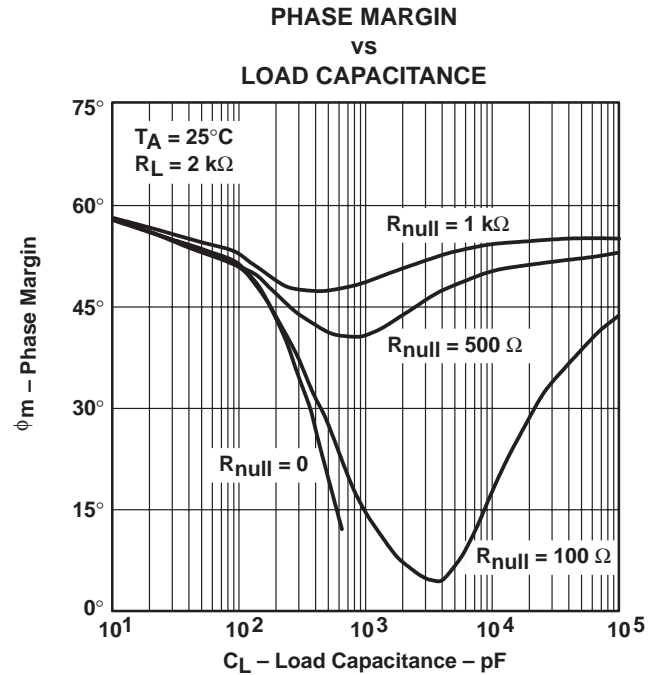
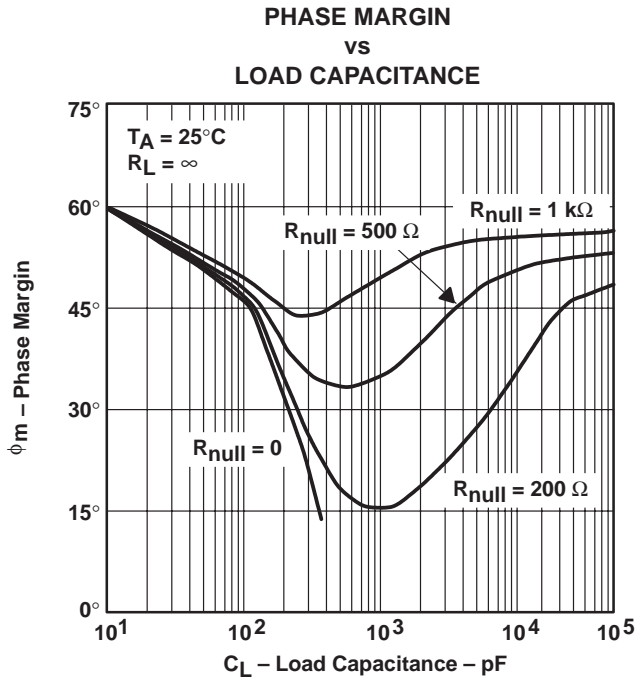


Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
 ‡ For all curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3\text{ V}$, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

driving large capacitive loads

The TLV2221 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 49 through Figure 54 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A small series resistor (R_{null}) at the output of the device (Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 49 through Figure 52 show the effects of adding series resistances of 100 Ω , 200 Ω , 500 Ω , and 1 k Ω . The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation (1) can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \tag{1}$$

where :

- $\Delta\phi_{m1}$ = improvement in phase margin
- UGBW = unity-gain bandwidth frequency
- R_{null} = output series resistance
- C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (Figure 53 and Figure 54). To use equation (1), UGBW must be approximated from Figure 53 and Figure 54.

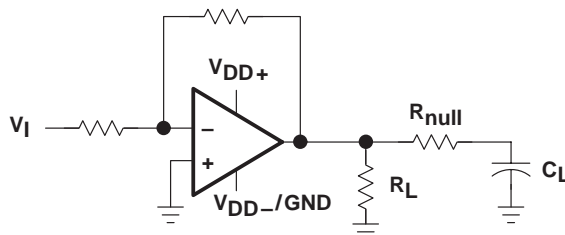


Figure 55. Series-Resistance Circuit

The TLV2221 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 μA and source 1 mA at $V_{DD} = 5\text{ V}$ at a maximum quiescent I_{DD} of 200 μA . This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as 2 k Ω , the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 37. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 38 illustrates two 2-k Ω load conditions. The first load condition shows the distortion seen for a 2-k Ω load tied to 2.5 V. The third load condition in Figure 38 shows no distortion for a 2-k Ω load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 38 illustrates the difference seen on the output for a 2-k Ω load and a 100-k Ω load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 56 are generated using the TLV2221 typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

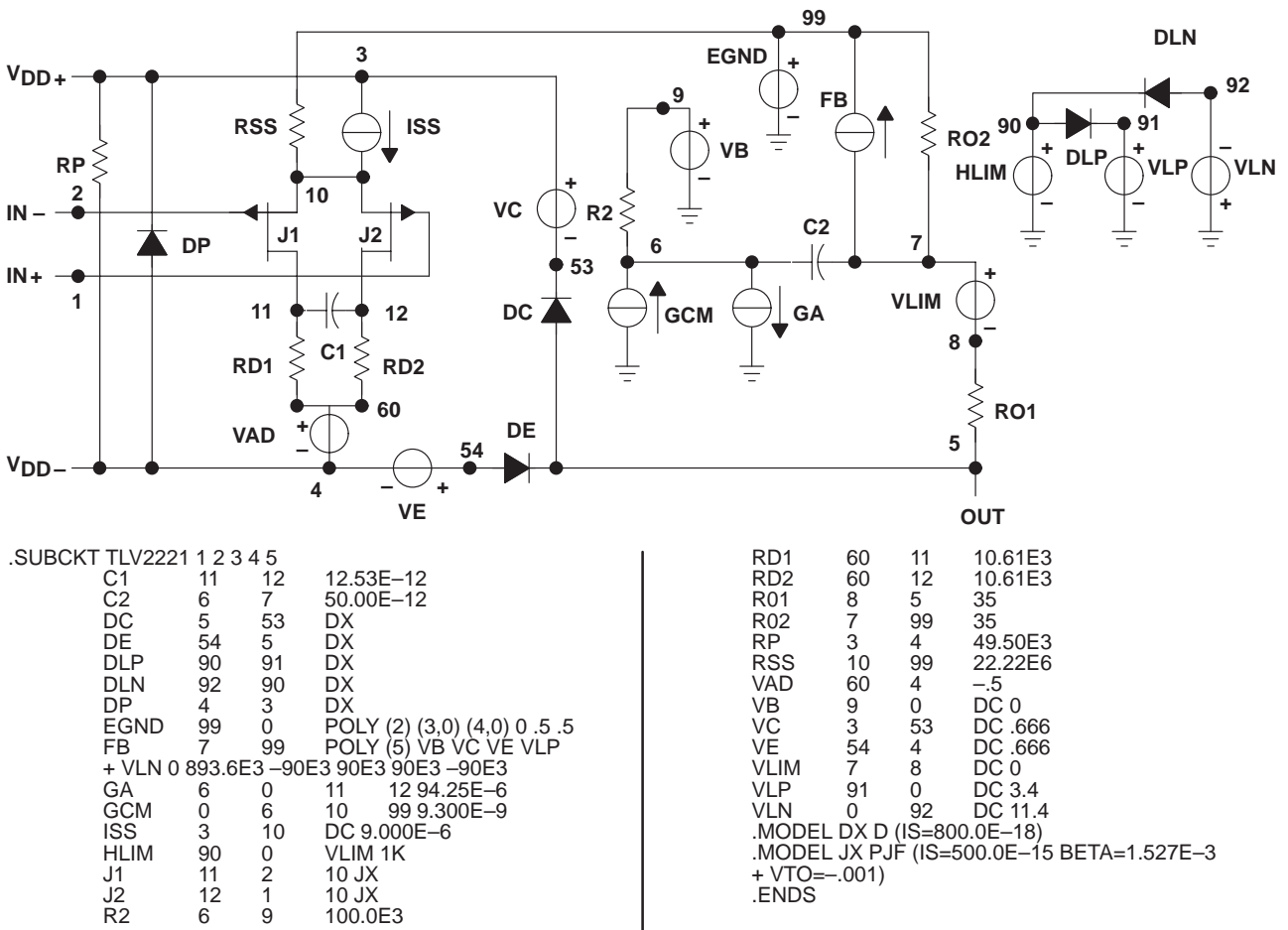


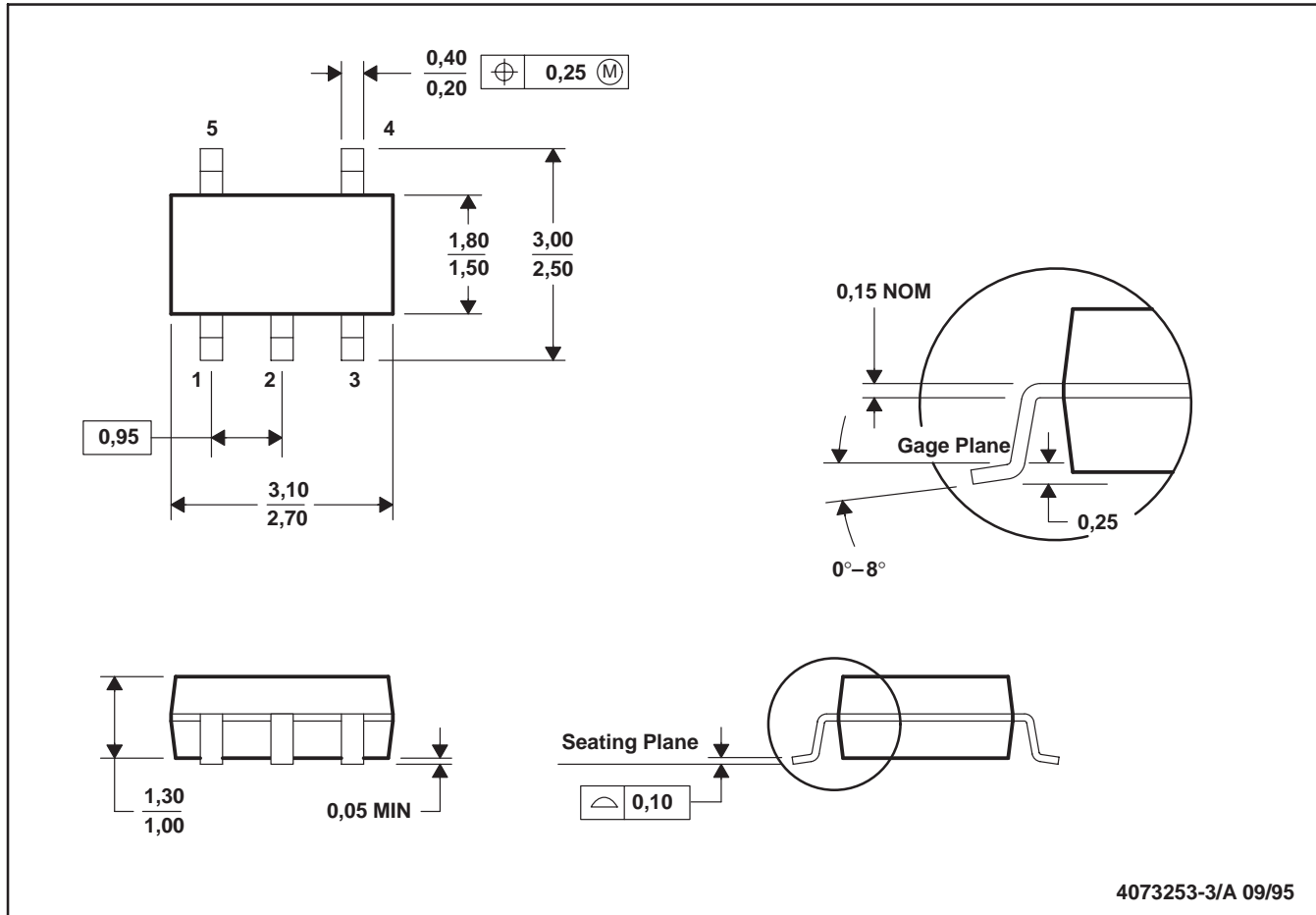
Figure 56. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademark of MicroSim Corporation.

MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2221CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2221CDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2221CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2221IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2221IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2221IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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