- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range . . . 0 V to 4.25 V (Min) at 5-V Single Supply**
- **No Phase Inversion**
- **Low Noise . . . 16 nV/√Hz Typ at f = 1 kHz**
- **Low Input Offset Voltage 950 μV Max at T_A = 25°C (TLV244xA)**
- **Low Input Bias Current . . . 1 pA Typ**
- **600-Ω Output Drive**
- **High-Gain Bandwidth . . . 1.8 MHz Typ**
- **Low Supply Current . . . 750 μA Per Channel Typ**
- **Macromodel Included**

† Contact factory for details. Q100 qualification data available on request.

description

The TLV244x and TLV244xA are low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range of these devices has been extended over typical standard CMOS amplifiers, making them suitable for a wide range of applications. In addition, these devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. Both devices offer comparable ac performance while having lower noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLV244x has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecommunications applications.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

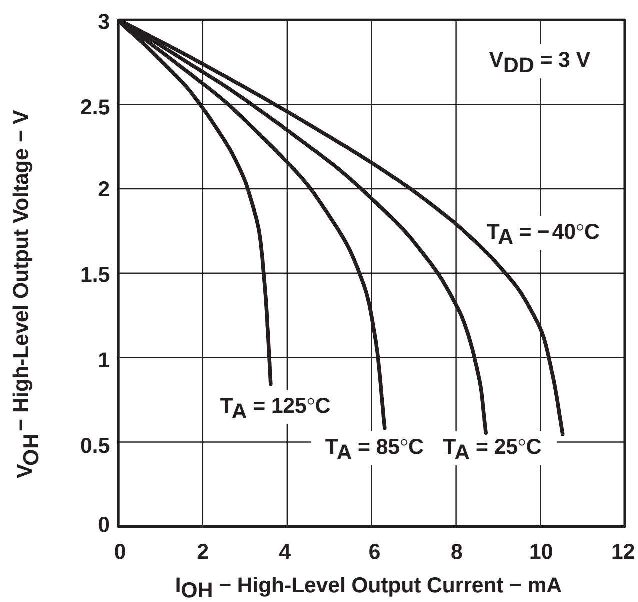


Figure 1

The other members in the TLV244x family are the low-power, TLV243x, and micro-power, TLV2422, versions.

The TLV244x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV244xA is available with a maximum input offset voltage of 950 μV.

description (continued)

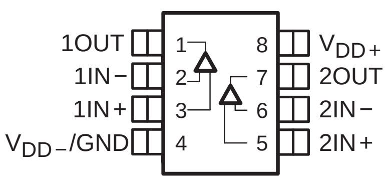
If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

ORDERING INFORMATION†

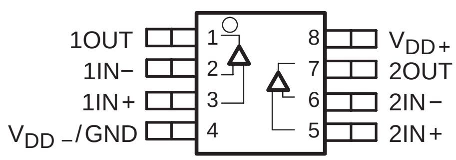
T_A	V_{IO}max AT 25°C	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	950 µV	SOIC (D)	Tape and reel	TLV2442AQDRQ1	2442AQ
		TSSOP (PW)	Tape and reel	TLV2442AQPWRQ1	2442AQ
	2.5 mV	SOIC (D)	Tape and reel	TLV2442QDRQ1	2442Q1
		TSSOP (PW)	Tape and reel	TLV2442QPWRQ1	2442Q1
−40°C to 125°C	950 µV	SOIC (D)	Tape and reel	TLV2444AQDRQ1‡	
		TSSOP (PW)	Tape and reel	TLV2444AQPWRQ1‡	
	2.5 mV	SOIC (D)	Tape and reel	TLV2444QDRQ1‡	
		TSSOP (PW)	Tape and reel	TLV2444QPWRQ1‡	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ Product Preview.

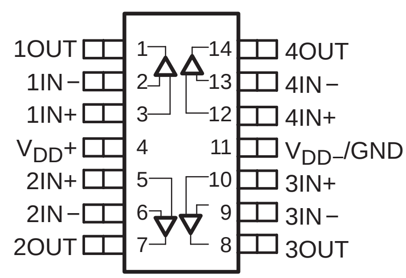
TLV2442
D PACKAGE
(TOP VIEW)



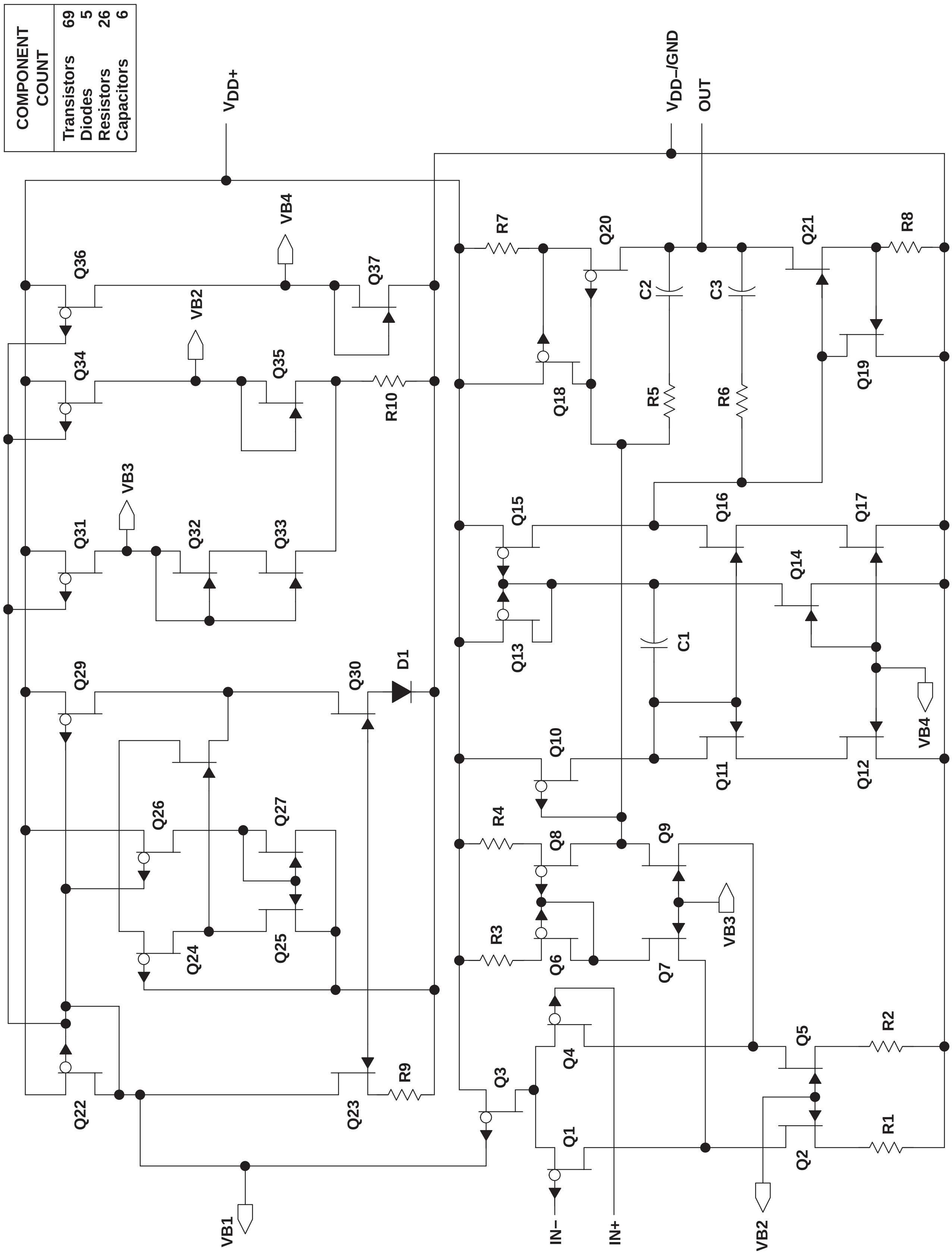
TLV2442
PW PACKAGE
(TOP VIEW)



TLV2444
D OR PW PACKAGE
(TOP VIEW)



equivalent schematic (each amplifier)



COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage, V_I (any input, see Note 1) . . . . . −0.3 V to V_{DD}
Input current, I_I (any input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: Q suffix . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current will flow if input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14)	1022 mW	7.6 mW/°C	900 mW	777 mW	450 mW
PW (8)	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW (14)	720 mW	5.6 mW/°C	634 mW	547 mW	317 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1$	V
Operating free-air temperature, T_A	−40	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2442-Q1 MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 1.5 V, V_O = 1.5 V, R_S = 50 Ω	TLV244x	25°C		300	2000	µV
				Full range			2500	
			TLV244xA	25°C		300	950	
				Full range			1600	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			260	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤ 8 mV, R_S = 50 Ω		25°C	0 to 2.25	−0.25 to 2.5		V
				Full range	0.2 to 2			
V_{OH}	High-level output voltage	I_O = −100 µA		25°C		2.98		V
		I_O = −3 mA		25°C		2.5		
				Full range	2.25			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V, I_O = 100 µA		25°C		0.02		V
		V_{IC} = 1.5 V, I_O = 3 mA		25°C		0.63		
				Full range			1	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 600 Ω	25°C	0.7	1		V/mV
				Full range	0.4			
			R_L = 1 MΩ	25°C		750		
r_{id}	Differential input resistance			25°C		1000		GΩ
r_i	Common-mode input resistance			25°C		1000		GΩ
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} MIN, V_O = V_{DD}/2, R_S = 50 Ω		25°C	65	75		dB
				Full range	50			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load		25°C		725	1100	µA
				Full range			1100	

† Full range for the Q suffix is −40°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV244x-Q1			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1 V to 2 V, R_L = 600 Ω, C_L = 100 pF		25°C	0.65	1.3		V/µs
				Full range	0.4			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		170		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.6		µV
		f = 0.1 Hz to 10 Hz		25°C		5.1		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.08%		
			A_V = 10			0.3%		
			A_V = 100			2%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω, C_L = 100 pF		25°C		1.75		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω, A_V = 1, C_L = 100 pF		25°C		0.9		MHz
t_s	Settling time	A_V = −1, Step = −2.3 V to 2.3 V, R_L = 600 Ω, C_L = 100 pF	To 0.1%	25°C		1.5		µs
			To 0.01%			3.2		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		65°		
	Gain margin			25°C		9		dB

† Full range for the Q suffix is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV244x-Q1 MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm} = \pm2.5$ V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	TLV244x	25°C		300	2000	µV
				Full range			2500	
			TLV244xA	25°C		300	950	
				Full range			1600	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.002		µV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			260	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le 5$ mV, R_S = 50 Ω		25°C	0 to 4.25	−0.25 to 4.5		V
				Full range	0 to 4			
V_{OH}	High-level output voltage	I_{OH} = −100 µA		25°C		4.97		V
		I_{OH} = −5 mA		25°C	4	4.35		
				Full range	4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 µA		25°C		0.01		V
		V_{IC} = 2.5 V, I_{OL} = 5 mA		25°C		0.8		
				Full range			1.25	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 600 Ω‡	25°C	0.9	1.3		V/mV
				Full range	0.5			
			R_L = 1 MΩ‡	25°C		950		
r_{id}	Differential input resistance			25°C		1000		GΩ
r_i	Common-mode input resistance			25°C		1000		GΩ
c_i	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10		25°C		140		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ MIN, $V_O = V_{DD}/2$, R_S = 50 Ω		25°C	70	75		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		750	1100	µA
				Full range			1100	

† Full range for the Q suffix is −40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV244x-Q1			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡		25°C	0.75	1.4		V/μs
				Full range	0.5			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		130		nV/√Hz
		f = 1 kHz		25°C		16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.8		μV
		f = 0.1 Hz to 10 Hz		25°C		3.6		
I_n	Equivalent input noise current			25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.017%		
			A_V = 10			0.17%		
			A_V = 100			1.5%		
	Gain-bandwidth product	f =10 kHz, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		1.81		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 600 Ω‡, C_L = 100 pF‡		25°C		0.5		MHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		1.5		μs
			To 0.01%			2.6		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡, C_L = 100 pF‡		25°C		68°		
	Gain margin			25°C		8		dB

† Full range for the Q suffix is −40°C to 125°C.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs†

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode input voltage	2, 3 4, 5
α_{VIO}	Input offset voltage temperature coefficient	Distribution	6, 7
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	8
V_{OH}	High-level output voltage	vs High-level output current	9, 10
V_{OL}	Low-level output voltage	vs Low-level output current	11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	14 15
V_O	Output voltage	vs Differential Input voltage	16, 17
A_{VD}	Differential voltage amplification	vs Load resistance	18
A_{VD}	Large-signal differential voltage amplification and phase margin	vs Frequency	19, 20
	Large-signal differential voltage amplification	vs Free-air temperature	21, 22
z_o	Output impedance	vs Frequency	23, 24
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	25 26
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	27, 28 29
I_{DD}	Supply current	vs Supply voltage	30
SR	Slew rate	vs Load capacitance vs Free-air temperature	31 32
V_O	Inverting large-signal pulse response		33, 34
	Voltage-follower large-signal pulse response		35, 36
	Inverting small-signal pulse response		37, 38
	Voltage-follower small-signal pulse response		39, 40
V_n	Equivalent input noise voltage	vs Frequency	41, 42
	Noise voltage	Over a 10-second period	43
THD + N	Total harmonic distortion plus noise	vs Frequency	44, 45
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	46 47
ϕ_m	Phase margin	vs Frequency vs Load capacitance	19, 20 48
	Gain margin	vs Load capacitance	49
B_1	Unity-gain bandwidth	vs Load capacitance	50

† For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE

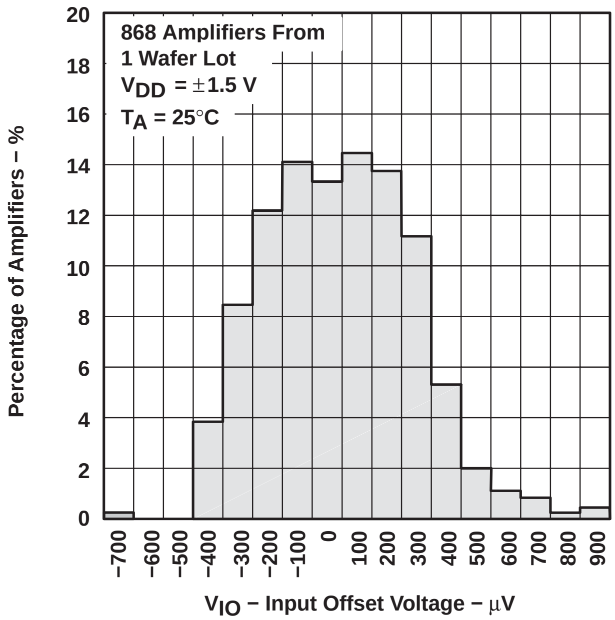


Figure 2

DISTRIBUTION OF TLV2442 INPUT OFFSET VOLTAGE

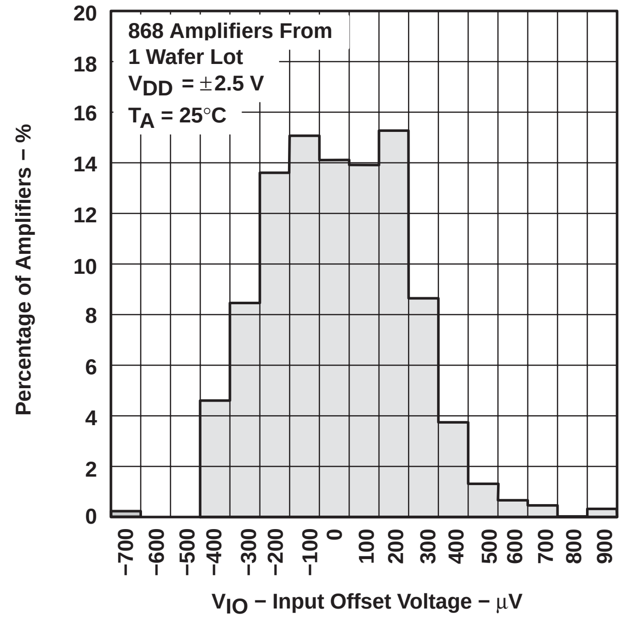


Figure 3

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

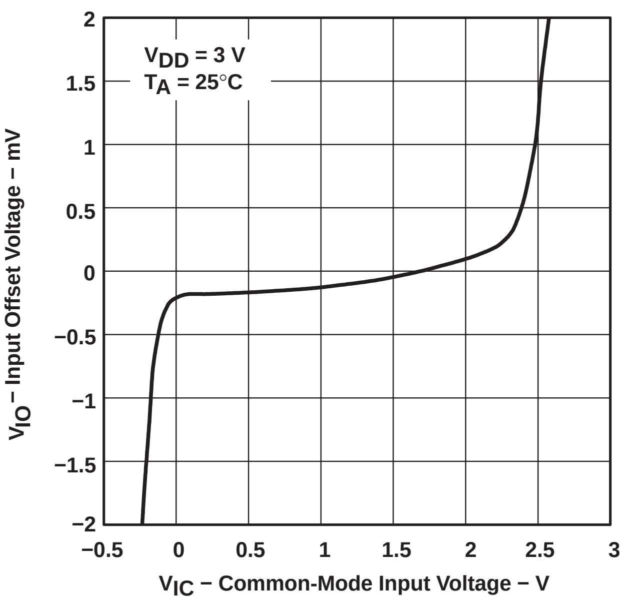


Figure 4

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

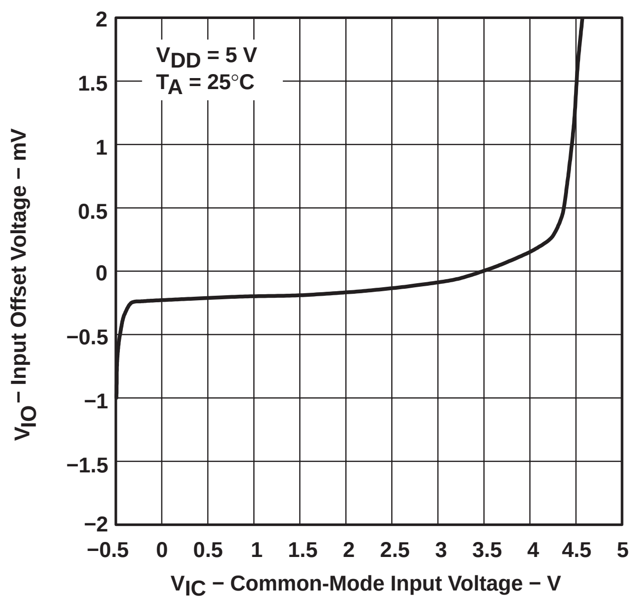


Figure 5

TYPICAL CHARACTERISTICS

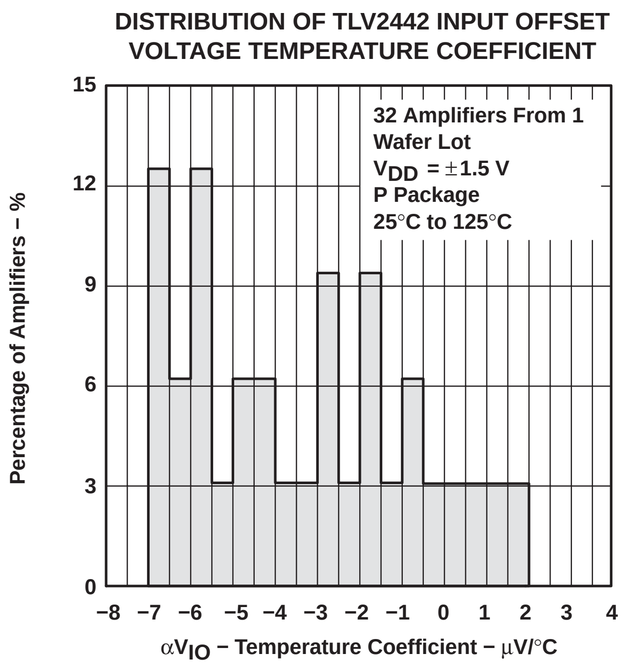


Figure 6

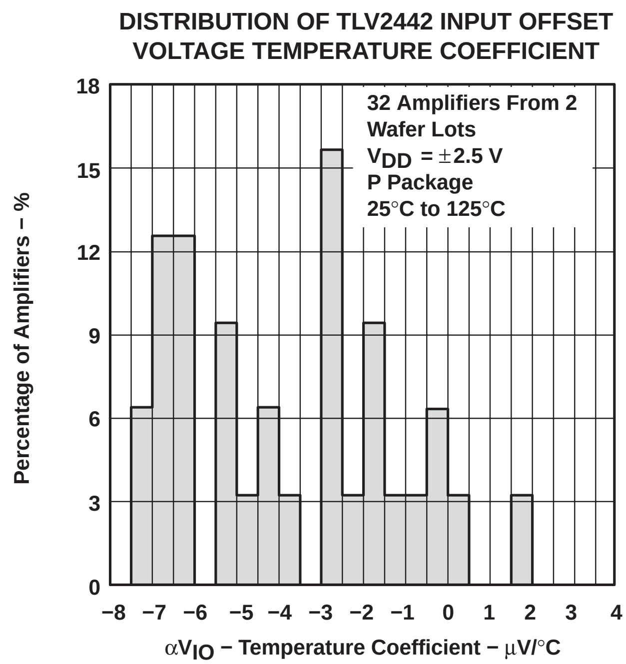


Figure 7

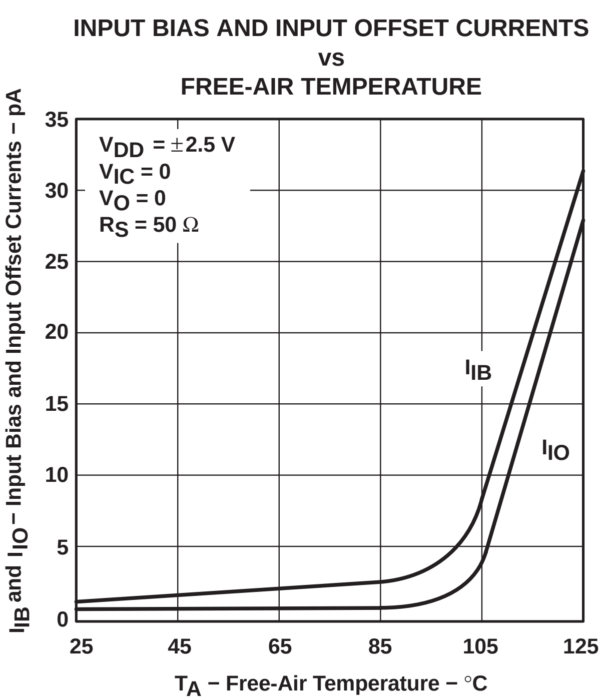


Figure 8

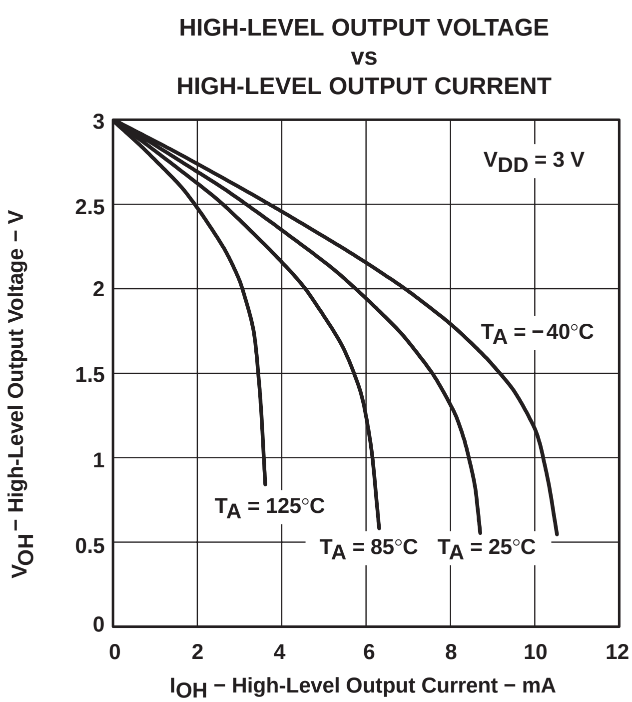


Figure 9

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

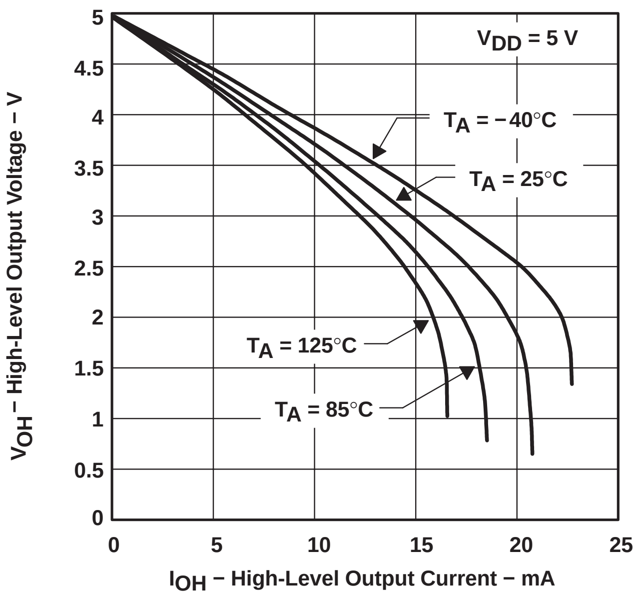


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

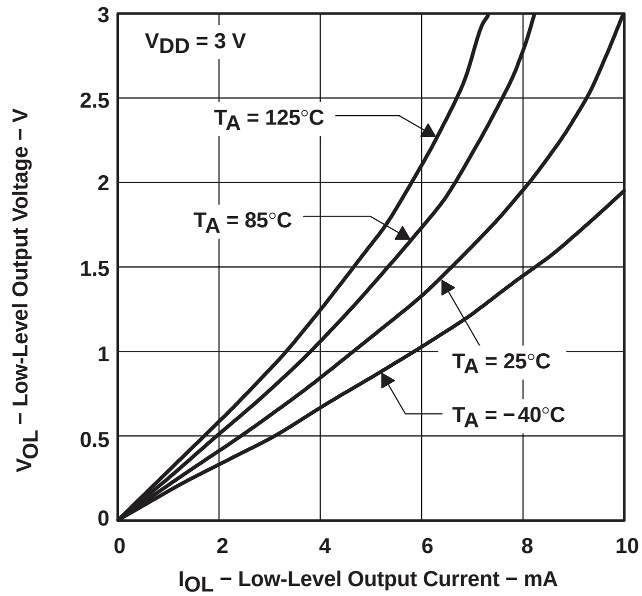


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

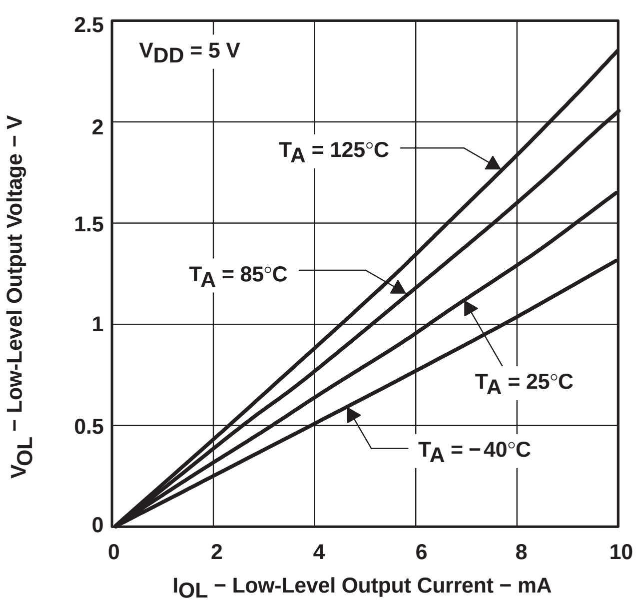


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

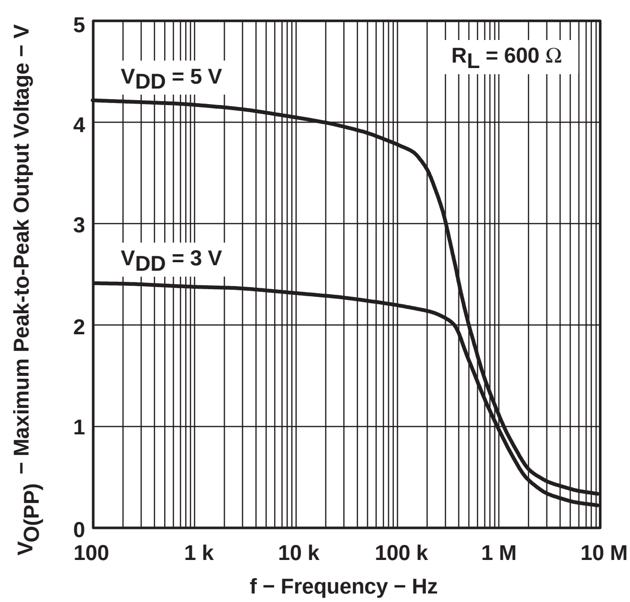


Figure 13

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

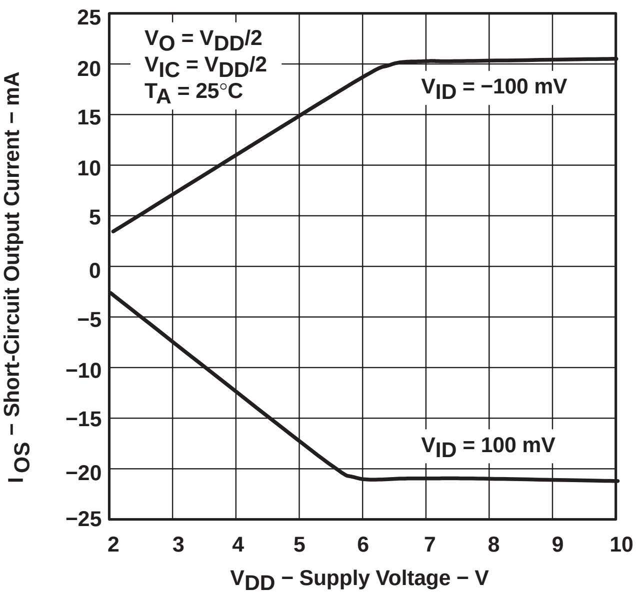


Figure 14

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

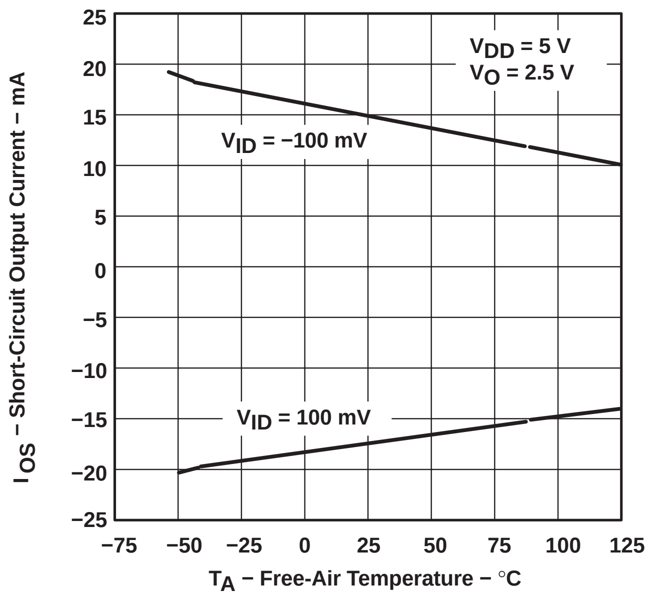


Figure 15

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

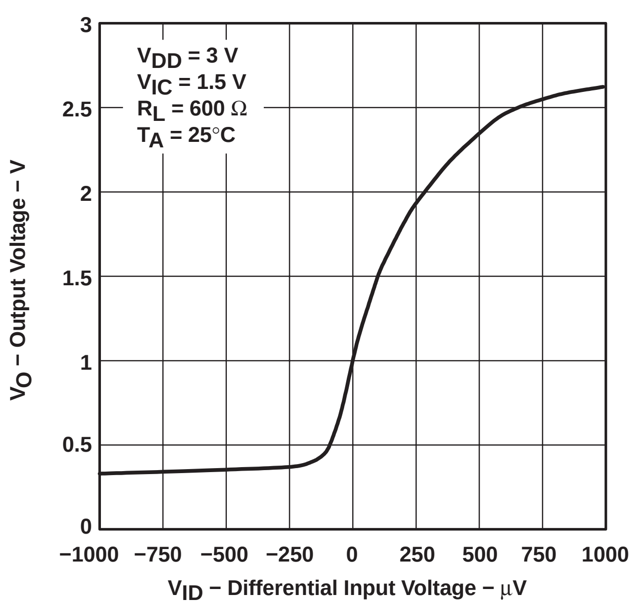


Figure 16

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

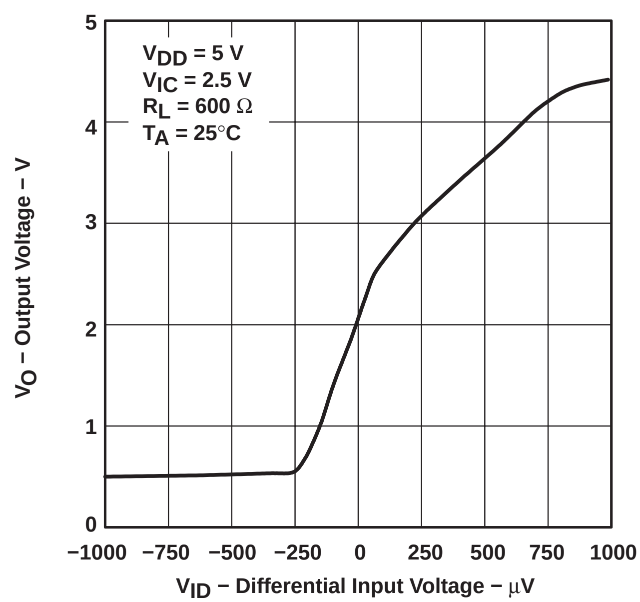


Figure 17

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION vs LOAD RESISTANCE

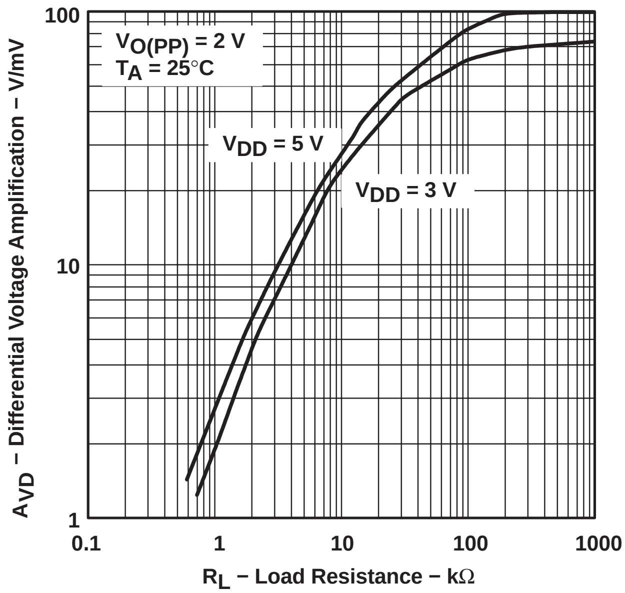


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

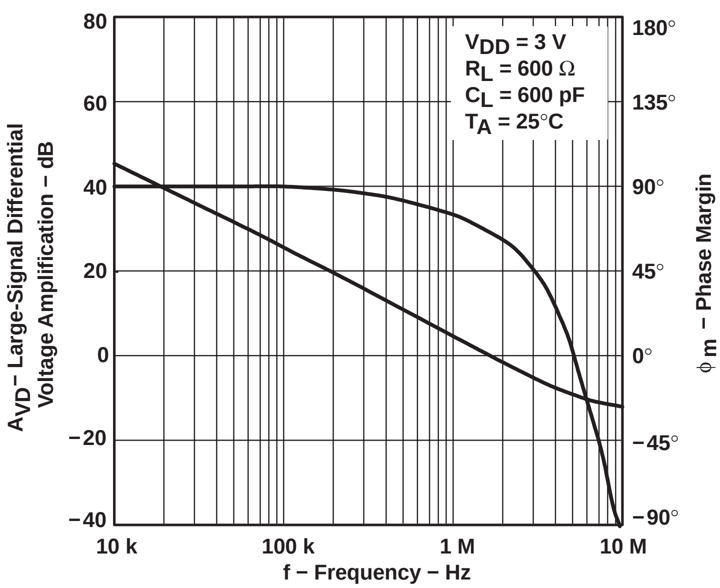


Figure 19

TYPICAL CHARACTERISTICS

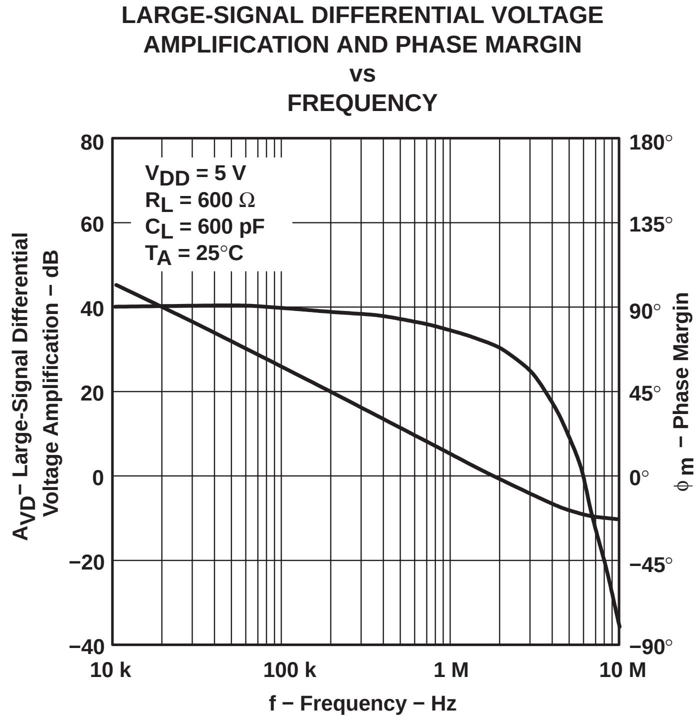


Figure 20

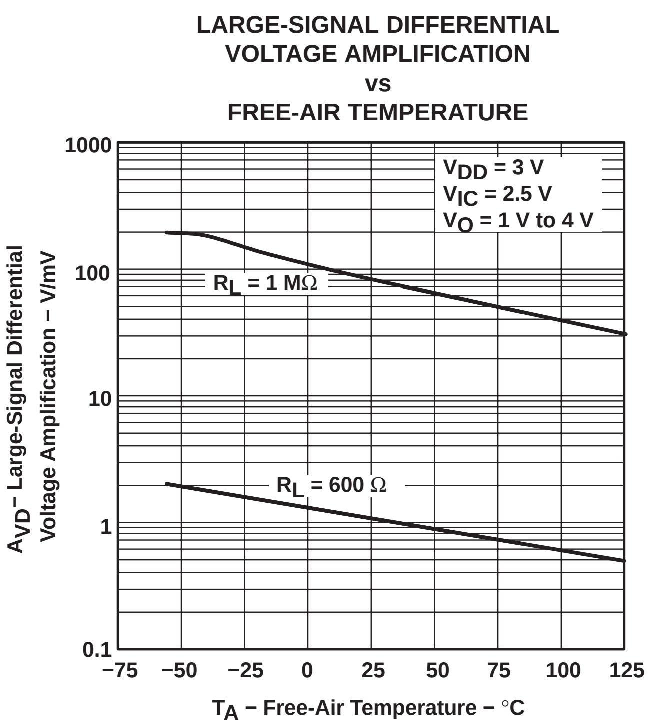


Figure 21

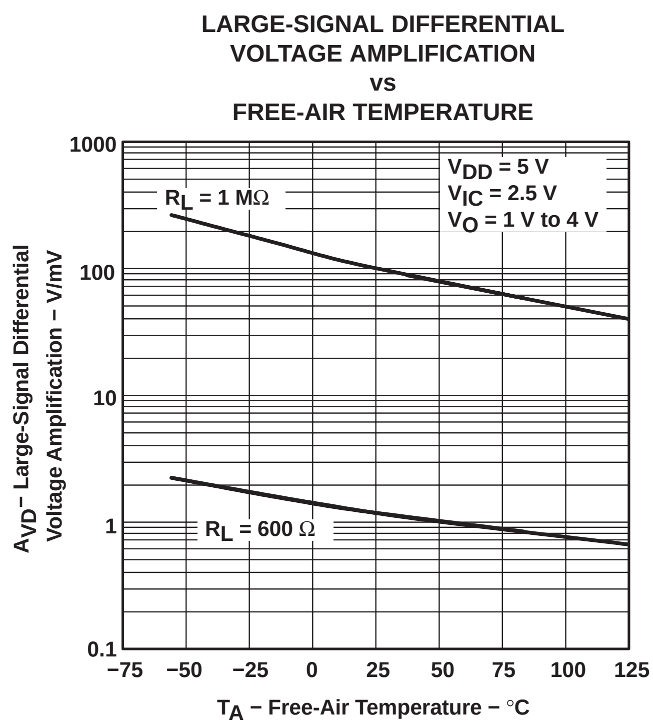


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

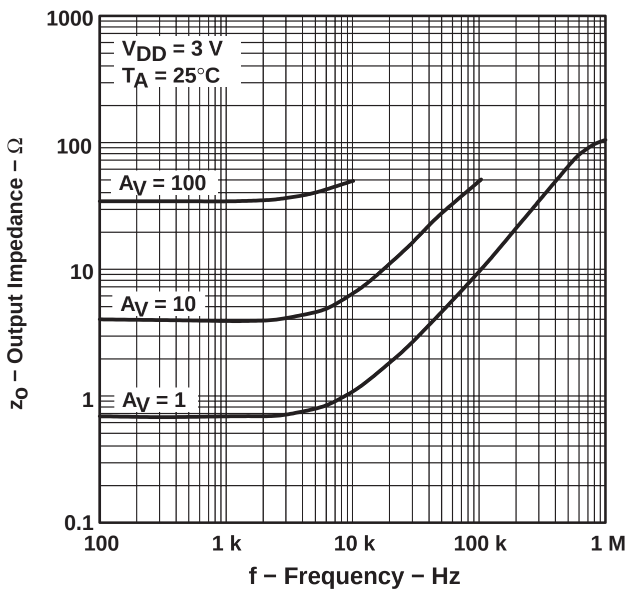


Figure 23

OUTPUT IMPEDANCE vs FREQUENCY

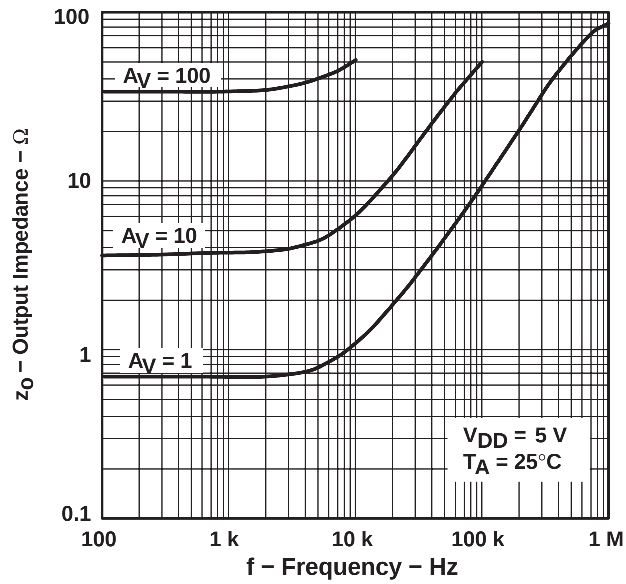


Figure 24

COMMON-MODE REJECTION RATIO vs FREQUENCY

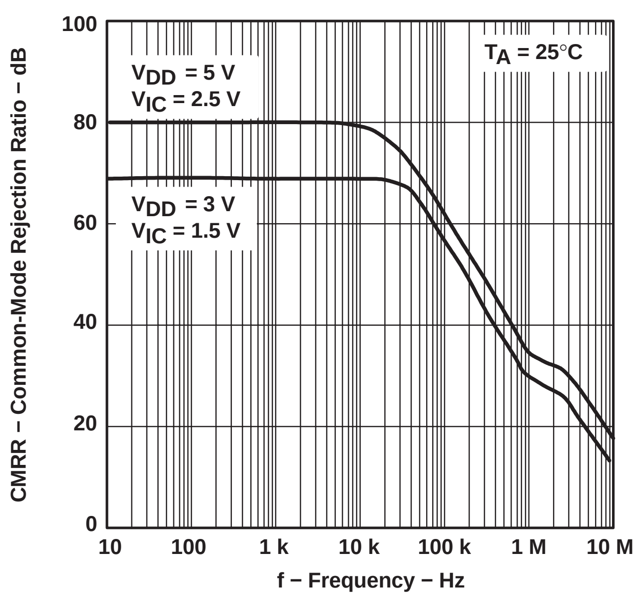


Figure 25

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

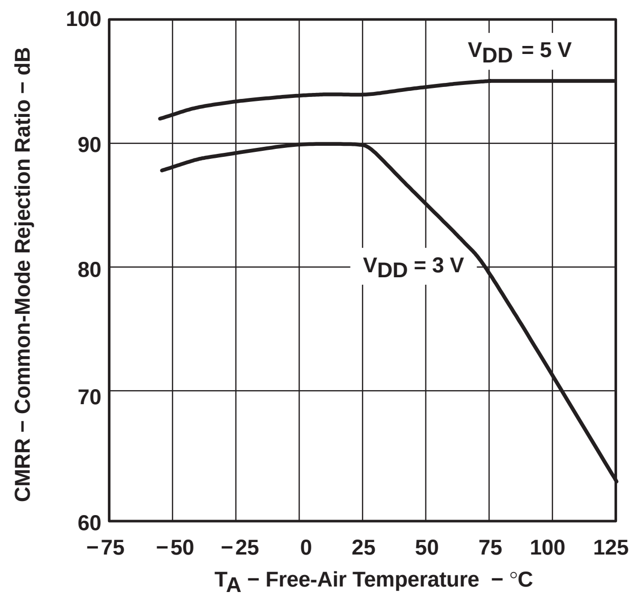


Figure 26

TYPICAL CHARACTERISTICS

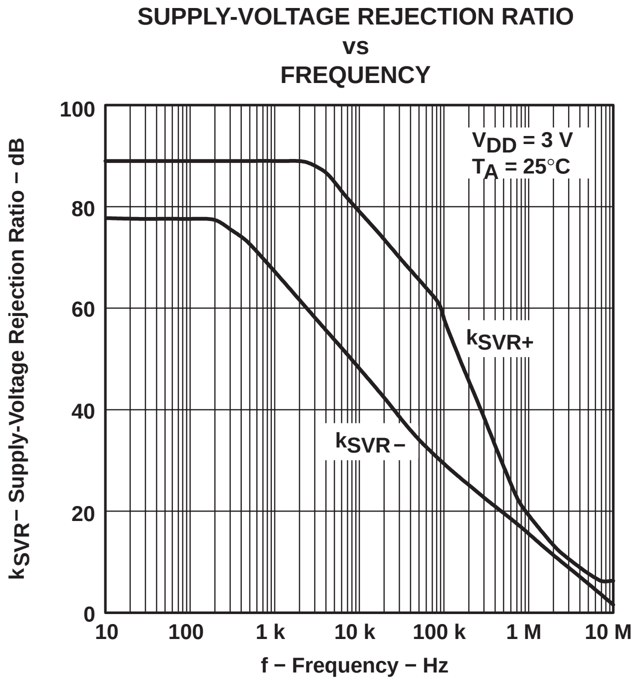


Figure 27

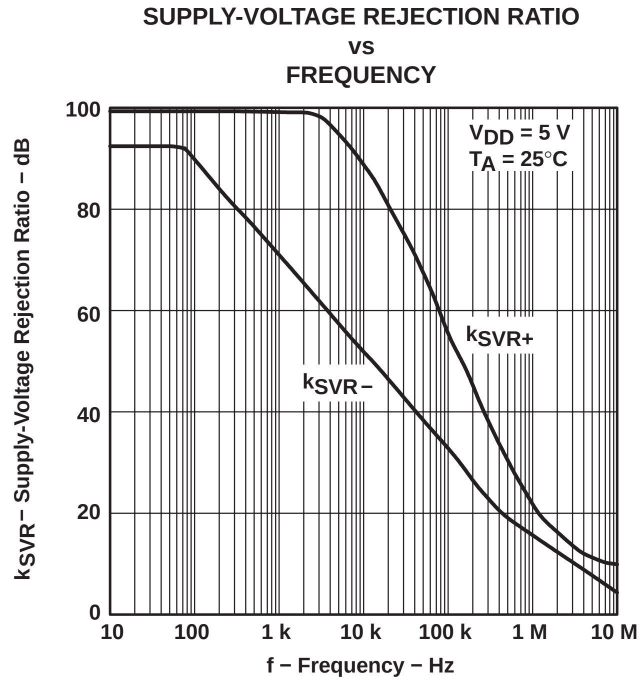


Figure 28

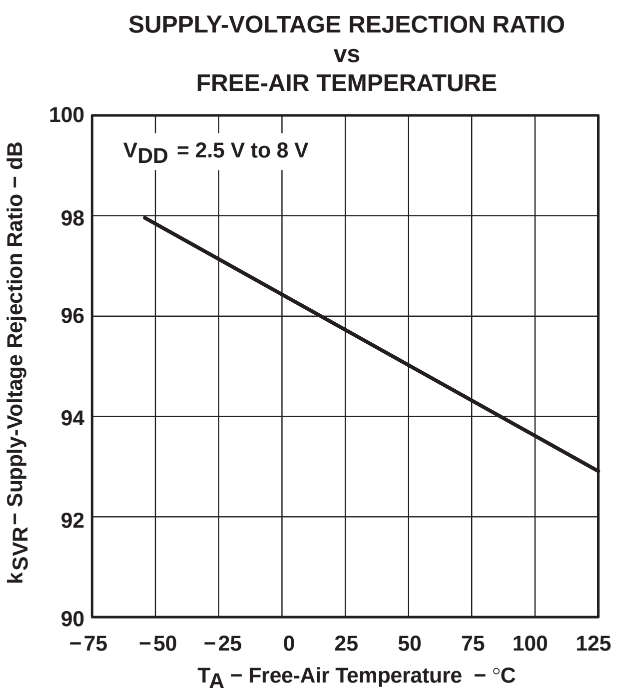


Figure 29

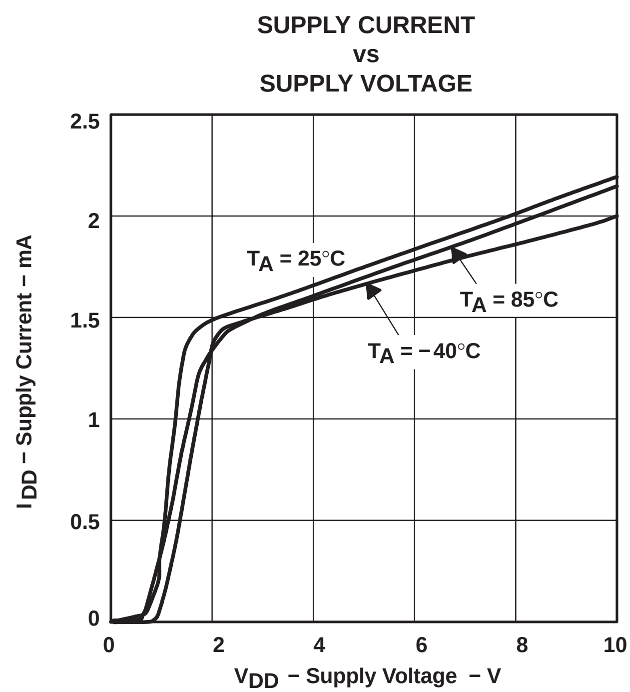


Figure 30

TYPICAL CHARACTERISTICS

SLEW RATE vs LOAD CAPACITANCE

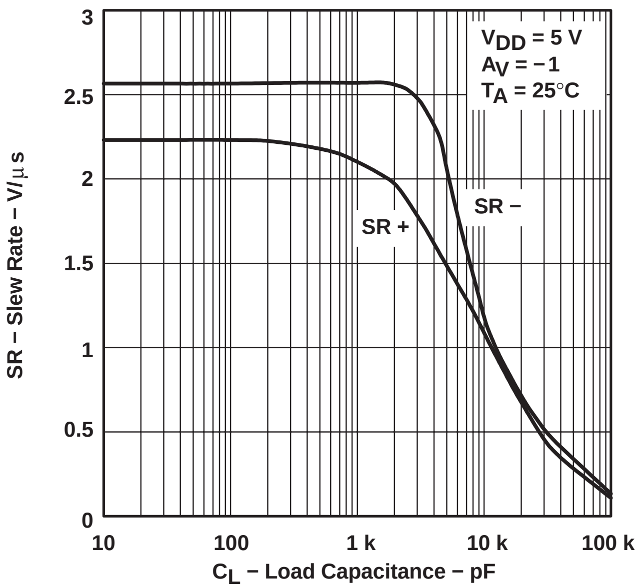


Figure 31

SLEW RATE vs FREE-AIR TEMPERATURE

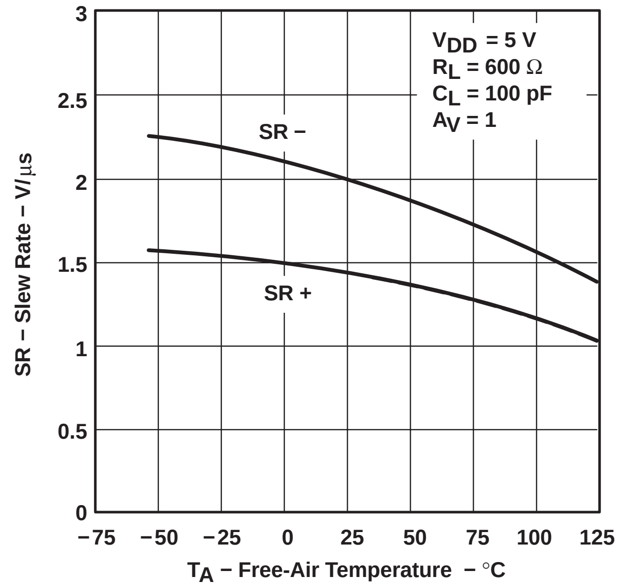


Figure 32

INVERTING LARGE-SIGNAL PULSE RESPONSE

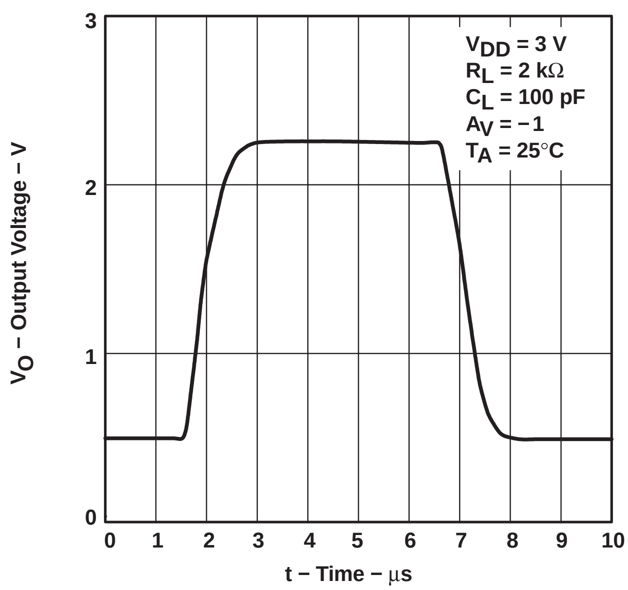


Figure 33

INVERTING LARGE-SIGNAL PULSE RESPONSE

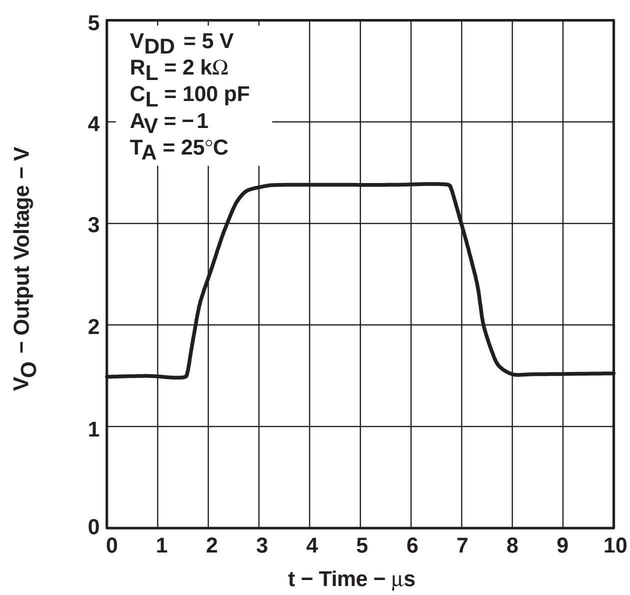


Figure 34

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

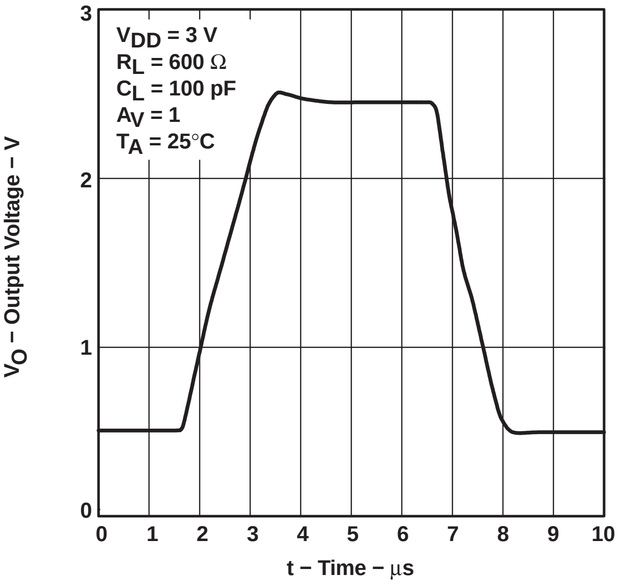


Figure 35

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

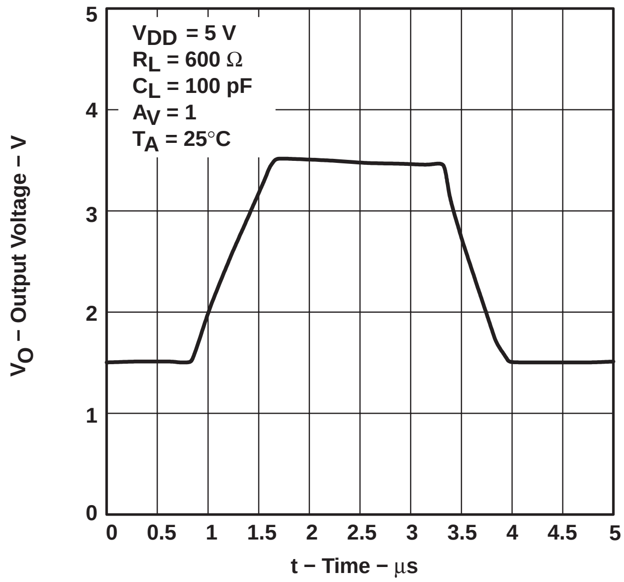


Figure 36

INVERTING SMALL-SIGNAL PULSE RESPONSE

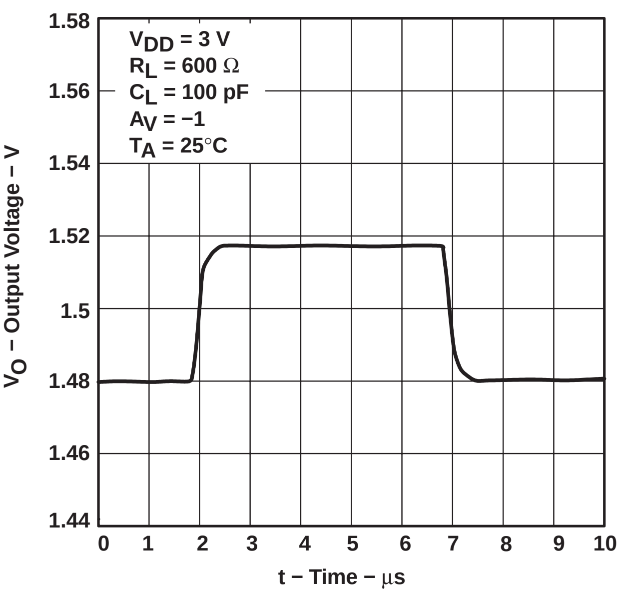


Figure 37

INVERTING SMALL-SIGNAL PULSE RESPONSE

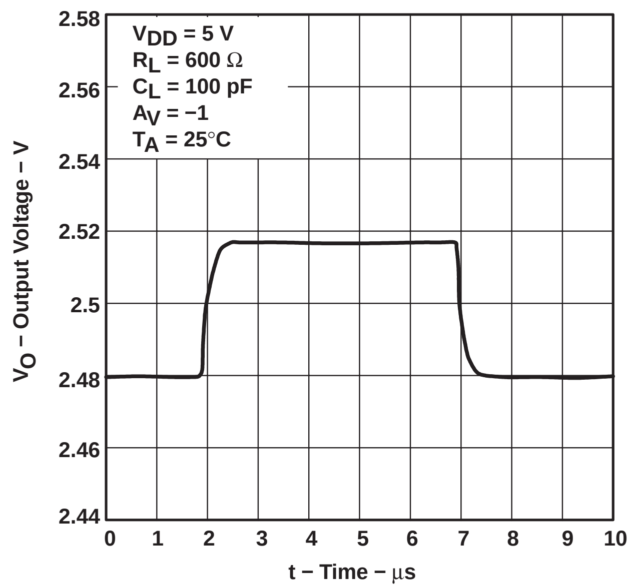


Figure 38

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

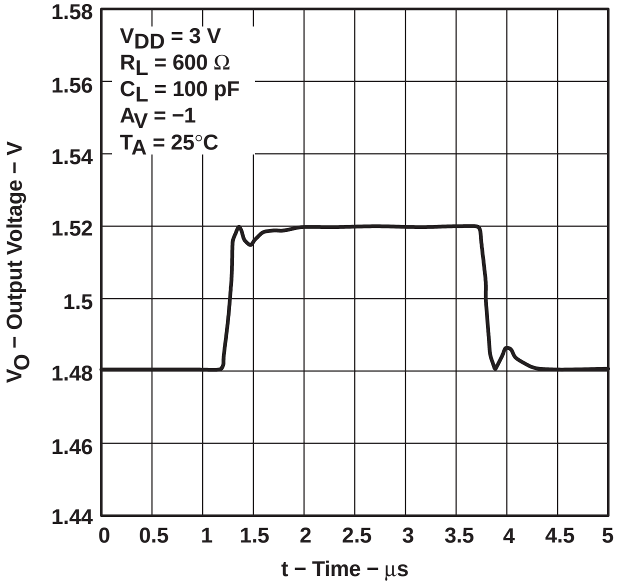


Figure 39

VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

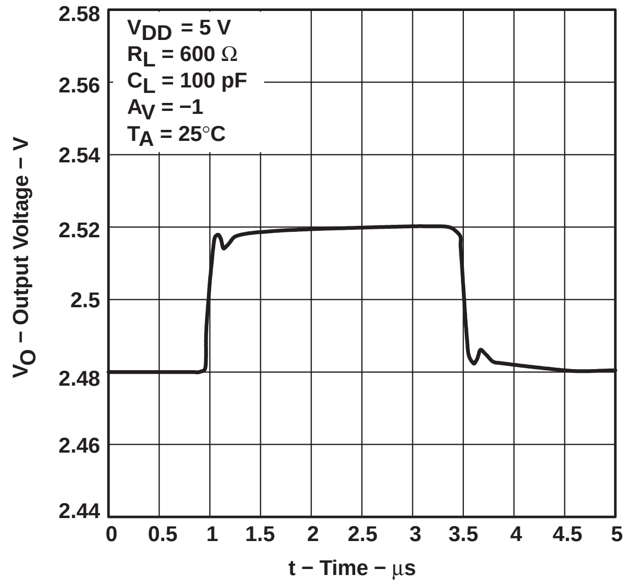


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

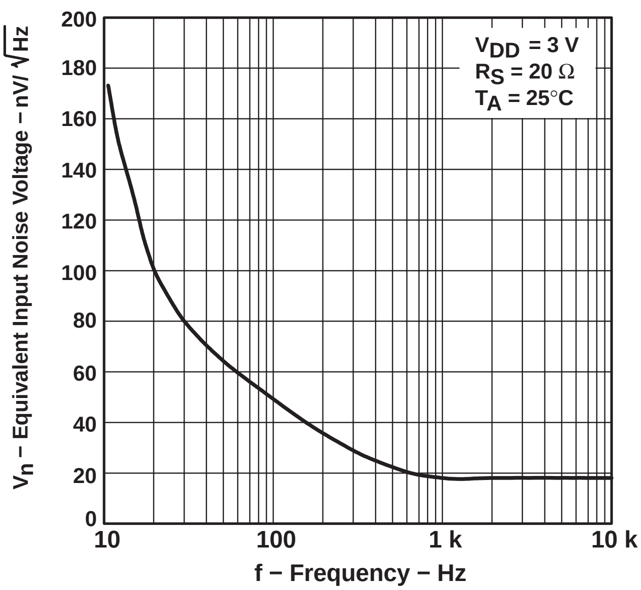


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

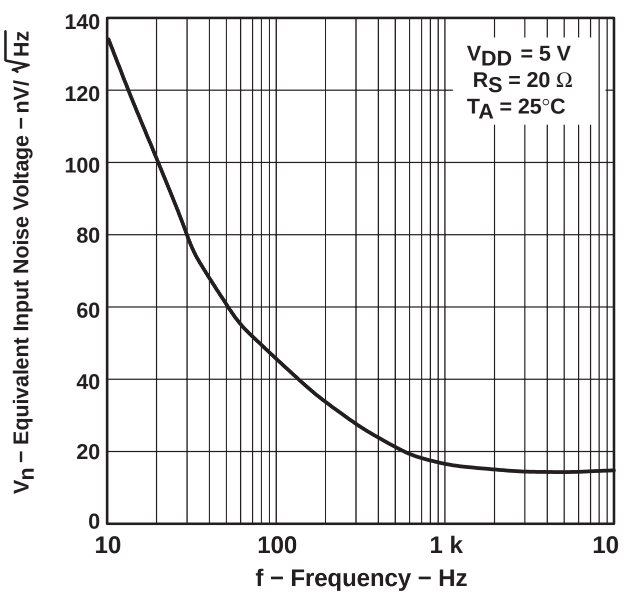


Figure 42

TYPICAL CHARACTERISTICS

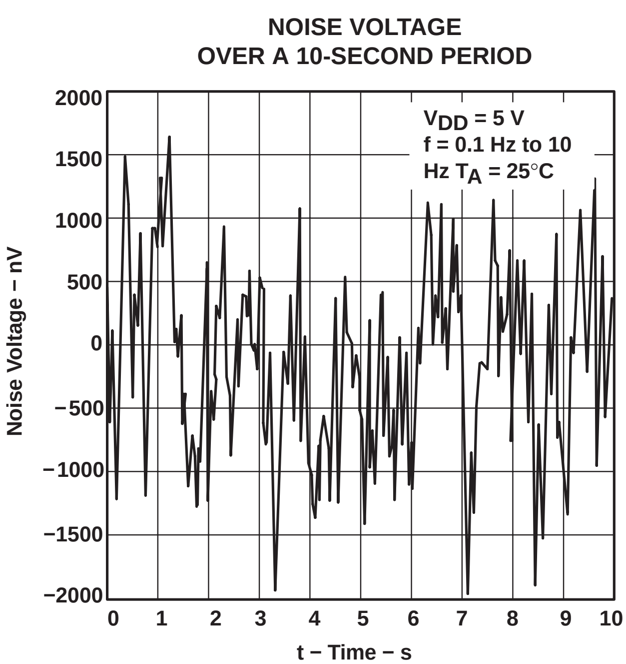


Figure 43

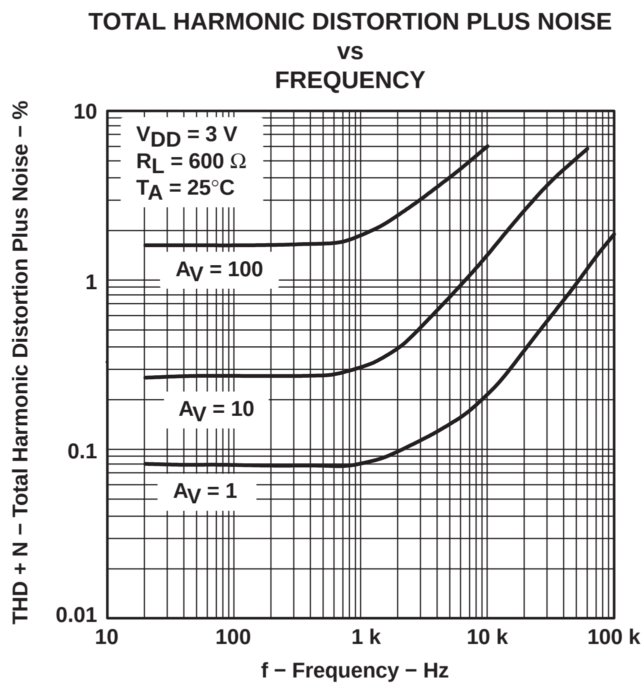


Figure 44

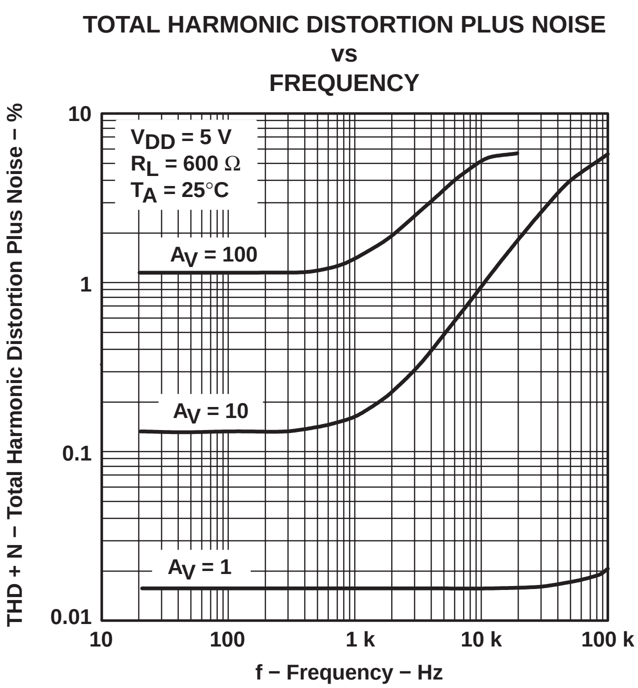


Figure 45

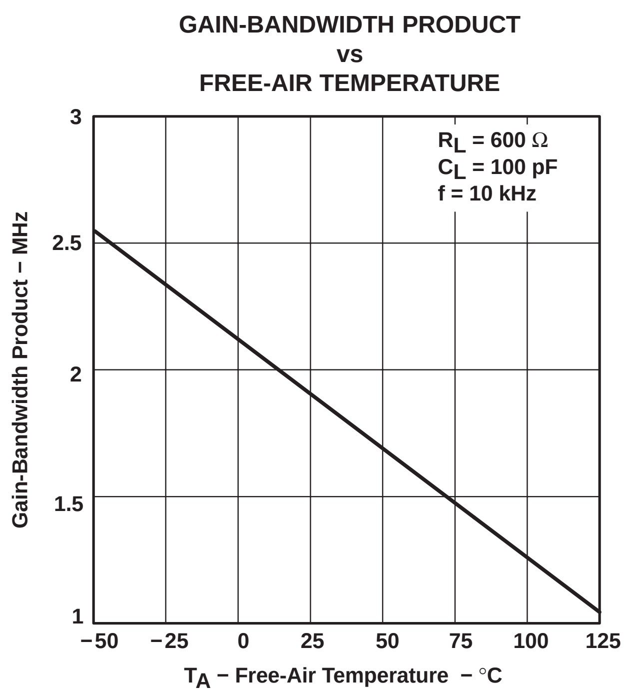


Figure 46

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

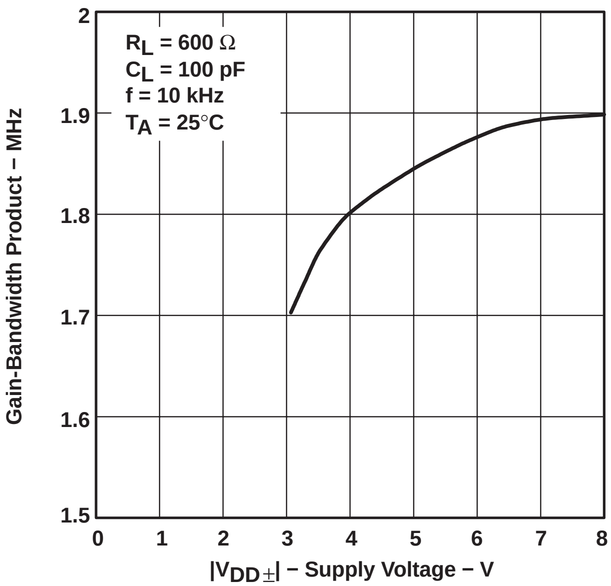


Figure 47

PHASE MARGIN
vs
LOAD CAPACITANCE

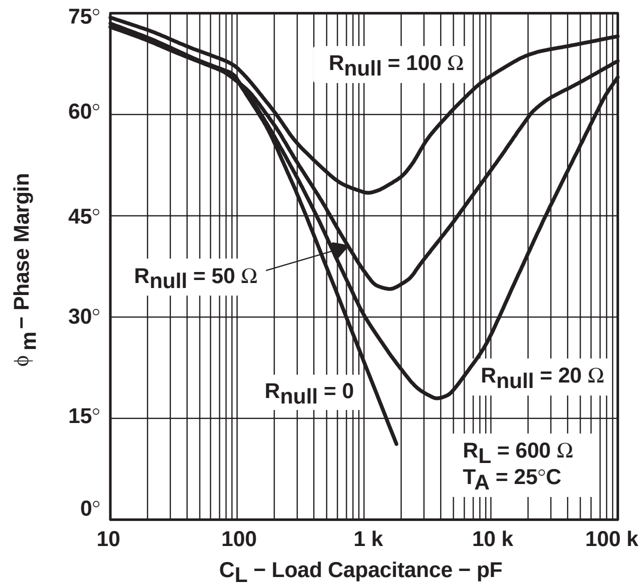


Figure 48

GAIN MARGIN
vs
LOAD CAPACITANCE

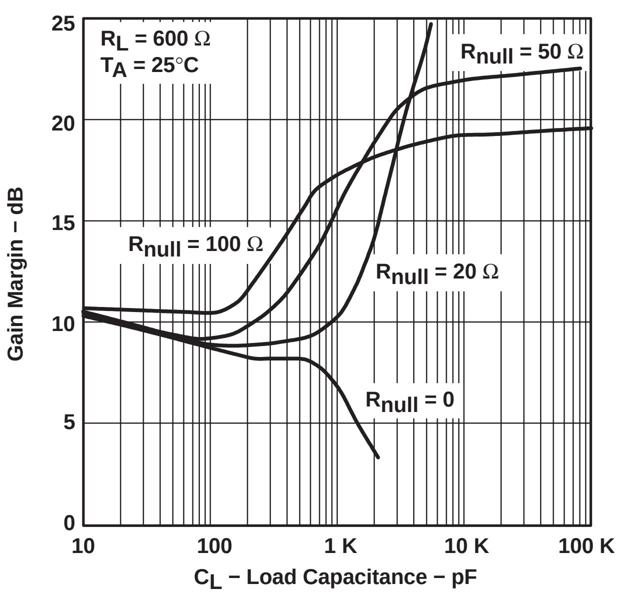


Figure 49

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

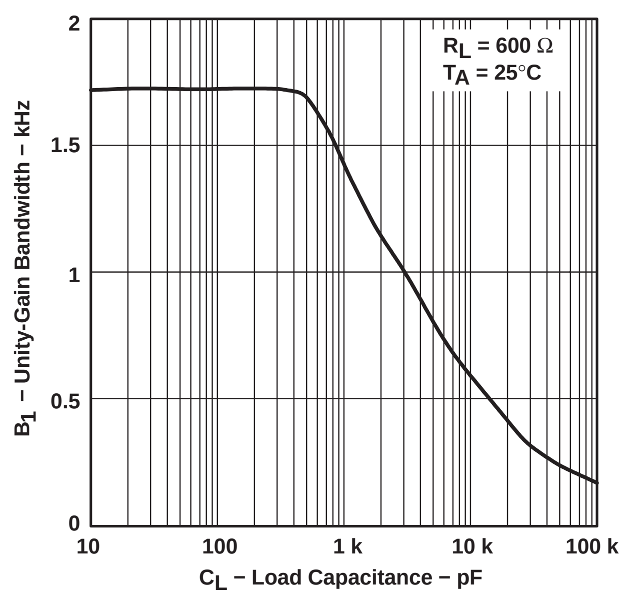


Figure 50

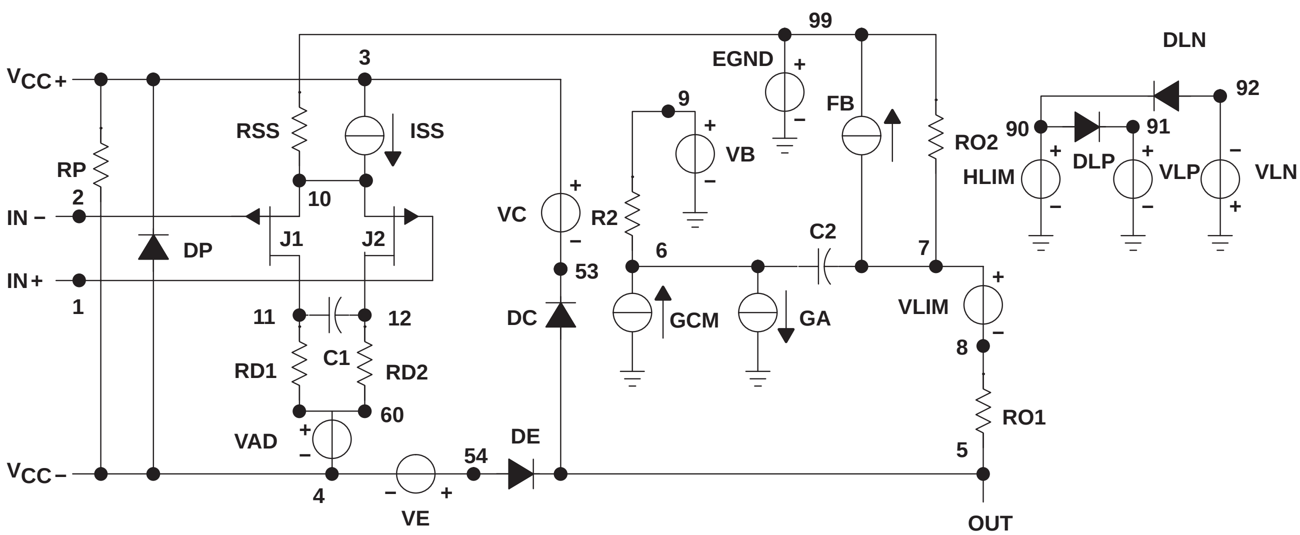
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using *PSpice*™ *Parts*™ model generation software. The Boyle macromodel (see Note 5) and subcircuit in Figure 51 were generated using the TLV244x typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV2442 1 2 3 4 5
C1     11    12    14E−12
C2     6     7     60.00E−12
DC     5     53    DX
DE     54    5     DX
DLP    90    91    DX
DLN    92    90    DX
DP     4     3     DX
EGND   99    0     POLY (2) (3,0) (4,) 0 .5 .5
FB     7     99    POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 −1E6 1E6 1E6 −1E6
GA     6     0     11    12 377.0E−6
GCM    0     6     10    99 134E−9
ISS    3     10    DC 216.0E−6
HLIM   90    0     VLIM 1K
J1     11    2     10 JX
J2     12    1     10 JX
R2     6     9     100.OE3
RD1    60    11    2.653E3
RD2    60    12    2.653E3
R01    8     5     50
R02    7     99    50
RP     3     4     4.310E3
RSS    10    99    925.9E3
VAD    60    4     −.5
VB     9     0     DC 0
VC     3     53    DC .78
VE     54    4     DC .78
VLIM   7     8     DC 0
VLP    91    0     DC 1.9
VLN    0     92    DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 51. Boyle Macromodel and Subcircuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV2442AQDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2442AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	None	CU NIPDAU	Level-1-220C-UNLIM
TLV2442QDRQ1	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
TLV2442QPWRQ1	ACTIVE	TSSOP	PW	8	2000	None	CU NIPDAU	Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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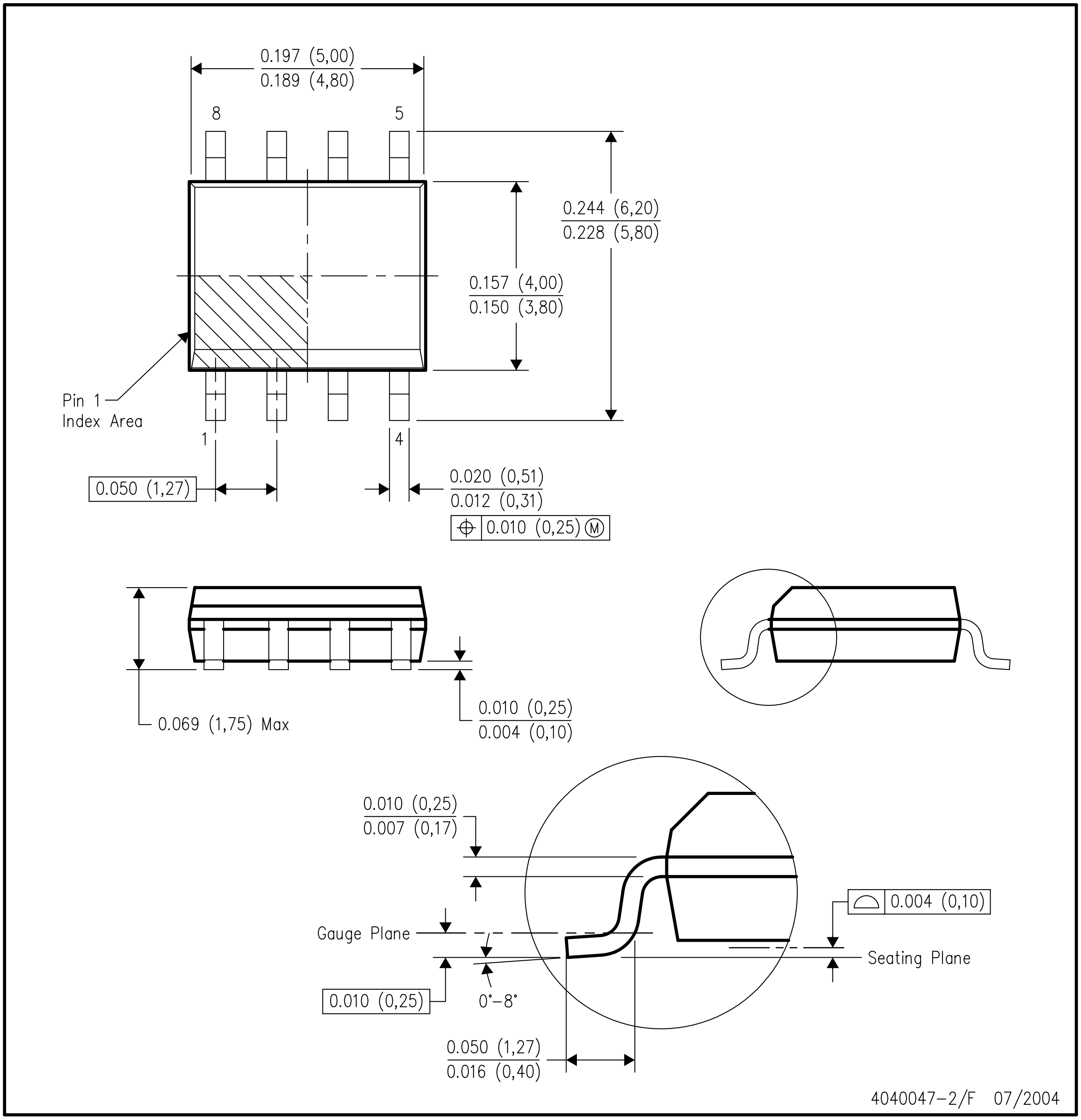
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

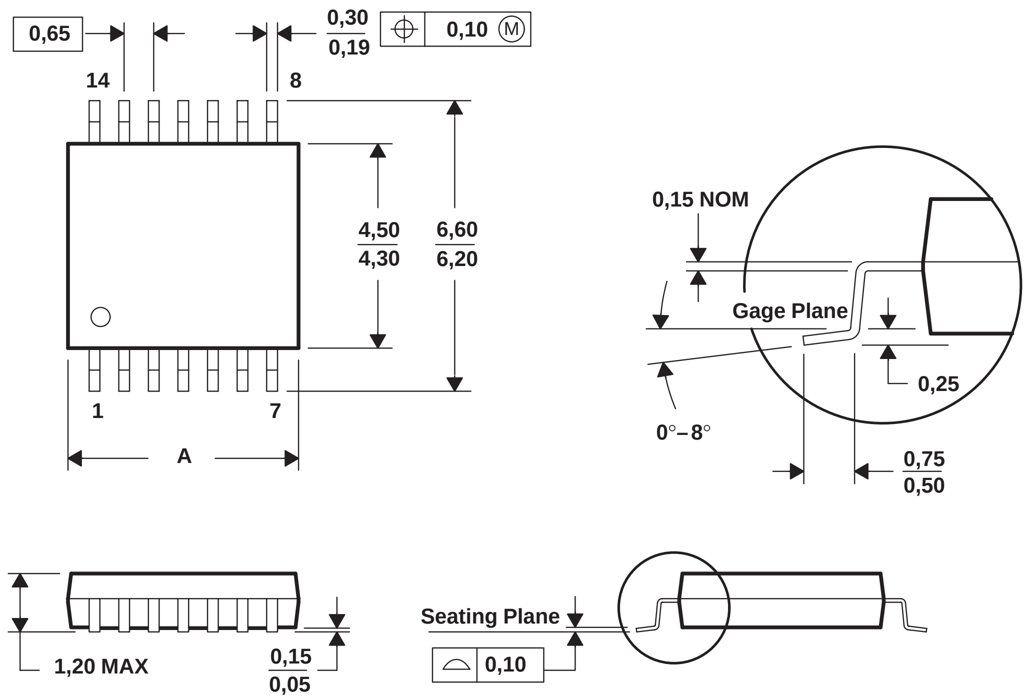
D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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Post Office Box 655303 Dallas, Texas 75265