#### TLV2721, TLV2721Y Advanced LinCMOS™ RAIL-TO-RAIL VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS SLOS197A – AUGUST1997 – REVISED MARCH 2001

- Output Swing Includes Both Supply Rails
- Low Noise . . . 19 nV/ $\sqrt{Hz}$  Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Single-Supply 3-V and 5-V Operation
- Very Low Power . . . 110 μA Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Wide Supply Voltage Range 2.7 V to 10 V
- Macromodel Included

#### description

DBV PACKAGE (TOP VIEW) OUT 1 5 V<sub>DD-</sub>/GND V<sub>DD+</sub> 2 IN+ 3 4 IN-

The TLV2721 is a single low-voltage operational amplifier available in the SOT-23 package. It offers a compromise between the ac performance and output drive of the TLV2731 and the micropower TLV2711.

It consumes only 150  $\mu$ A (max) of supply current and is ideal for battery-powered applications. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2721 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2721, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm<sup>2</sup>, the SOT-23 package only requires one third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

T.	Vie max AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM‡
TA	V <sub>IO</sub> max AT 25°C	SOT-23 (DBV)†	STMBOL	FORM+ (Y)
0°C to 70°C	3 mV	TLV2721CDBV	VAKC	TLV2721Y
-40°C to 85°C	3 mV	TLV2721IDBV	VAKI	

**AVAILABLE OPTIONS** 

<sup>†</sup> The DBV package available in tape and reel only.

<sup>‡</sup> Chip forms are tested at  $T_A = 25^{\circ}C$  only.



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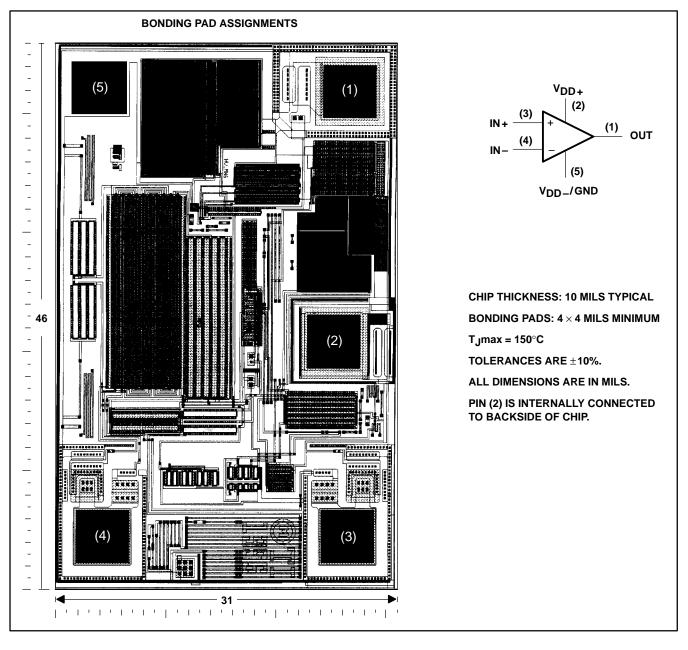


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#### **TLV2721Y** chip information

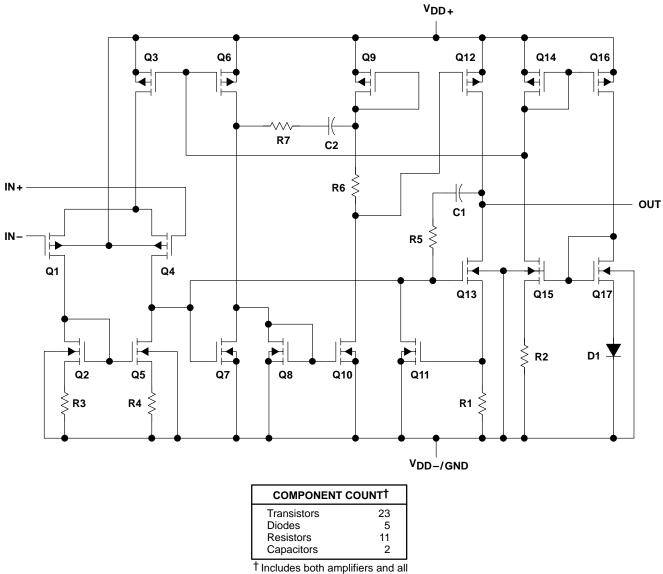
This chip, when properly assembled, displays characteristics similar to the TLV2721C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.





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#### equivalent schematic



ESD, bias, and trim circuitry



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, V <sub>DD</sub> (see Note 1)	
Differential input voltage, V <sub>ID</sub> (see Note 2)	
Input voltage range, V <sub>I</sub> (any input, see Note 1)	
Input current, I <sub>I</sub> (each input)	±5 mA
Output current, I <sub>O</sub>	±50 mA
Total current into V <sub>DD+</sub>	±50 mA
Total current out of V <sub>DD</sub>	±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : TLV2721C	0°C to 70°C
TLV2721I	–40°C to 85°C
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV packa	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to VDD-.

 Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V<sub>DD</sub> – 0.3 V.

3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

#### **DISSIPATION RATING TABLE**

PACKAGE	T <sub>A</sub> ≤ 25°C	DERATING FACTOR	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C
	POWER RATING	ABOVE T <sub>A</sub> = 25°C	POWER RATING	POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

#### recommended operating conditions

	TLV2721C		TL	UNIT	
	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V <sub>DD</sub> (see Note 1)	2.7	10	2.7	10	V
Input voltage range, VI	V <sub>DD</sub> -	V <sub>DD+</sub> -1.3	V <sub>DD</sub> -	V <sub>DD+</sub> -1.3	V
Common-mode input voltage, VIC	V <sub>DD</sub> -	V <sub>DD+</sub> -1.3	V <sub>DD</sub> -	V <sub>DD+</sub> -1.3	V
Operating free-air temperature, T <sub>A</sub>	0	70	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V<sub>DD</sub> -.



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#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 3 V (unless otherwise noted)

		TEAT AS		- +	Т	LV27210	C	1	<b>FLV2721</b>					
	PARAMETER	TEST CON	DITIONS	TA‡	MIN	TYP	MAX	MIN	TYP	MAX	UNIT			
VIO	Input offset voltage					0.5	3		0.5	3	mV			
αNO	Temperature coefficient of input offset voltage			Full range		1			1		μV/°C			
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 1.5 V,$ $V_{O} = 0,$	$V_{IC} = 0,$ R <sub>S</sub> = 50 $\Omega$	25°C		0.003			0.003		μV/m			
IIO	Input offset current			25°C		0.5	60		0.5	60	pА			
10	input onset current			Full range			150			150	P7.			
IIB	Input bias current			25°C		1	60		1	60	pА			
чв	input bias current			Full range			150			150	PΛ			
\/	Common-mode input	Do 50.0	1)/: = 1 < 5 m)/	25°C	0 to 2	-0.3 to 2.2		0 to 2	-0.3 to 2.2		v			
VICR	voltage range	R <sub>S</sub> = 50 Ω,	V O  ≤5 mV	Full range	0 to 1.7			0 to 1.7			V			
		I <sub>OH</sub> = -100 μA		25°C		2.97			2.97					
∨он	High-level output voltage			25°C		2.88			2.88		V			
-	vollage	I <sub>OH</sub> = -400 μA		Full range	2.6			2.6						
		V <sub>IC</sub> = 1.5 V, I <sub>OL</sub> = 50 μA 25°C 15			15									
VOL	Low-level output voltage			25°C		150			150		m٧			
	vollage	V <sub>IC</sub> = 1.5 V,	I <sub>OL</sub> = 500 μA	IOL = 500 μA	$OL = 300 \mu A$	IOL = 300 μA	Full range			500			500	
	Large-signal		P: - 2 k0t 25°	25°C	2	3		2	3					
AVD	differential voltage	$V_{IC} = 1.5 V,$ $V_{O} = 1 V \text{ to } 2 V$		Full range	1	1		1	1		V/m			
	amplification	VO = 1 V 10 2 V	$R_L = 1 M\Omega^{\ddagger}$	25°C		250			250					
<sup>r</sup> id	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω			
ric	Common-mode input resistance			25°C		10 <sup>12</sup>			1012		Ω			
c <sub>ic</sub>	Common-mode input capacitance	f = 10 kHz		25°C		6			6		pF			
z <sub>o</sub>	Closed-loop output impedance	f = 10 kHz,	A <sub>V</sub> = 10	25°C		90			90		Ω			
CMPP	Common-mode	$V_{IC} = 0$ to 1.7 V,		25°C	70	82		70	82		٩D			
CMRR	rejection ratio	V <sub>O</sub> = 1.5 V,	$R_S = 50 \Omega$	Full range	65			65			dB			
koup	Supply voltage	V <sub>DD</sub> = 2.7 V to 8	V,	25°C	80	95		80	95		40			
ksvr	rejection ratio (ΔV <sub>DD</sub> /ΔV <sub>IO</sub> )	$V_{IC} = V_{DD}/2$ ,	No load	Full range	80			80			dB			
1	Supply ourrest		Nolood	25°C		100	150		100	150				
DD	Supply current	V <sub>O</sub> = 1.5 V,	No load	Full range			200			200	μA			

<sup>†</sup> Full range for the TLV2721C is 0°C to 70°C. Full range for the TLV2721I is – 40°C to 85°C.

‡Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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#### operating characteristics at specified free-air temperature, $V_{DD}$ = 3 V

	DADAMETER	TEAT COND		- +	Т	LV2721	C		TLV2721										
	PARAMETER	TEST COND	ITIONS	TA <sup>†</sup>	MIN	TYP	MAX	MIN	TYP	MAX	UNIT								
	Slew rate at unity	V <sub>O</sub> = 1.1 V to 1.9 V,	$P_{1} = 2 k_{0} t$	25°C	0.1	0.25		0.1	0.25										
SR	gain	$C_{L} = 100 \text{ pF}^{\ddagger}$	RL = 2 K32+,	Full range	0.05			0.05			V/µs								
V	Equivalent input	f = 10 Hz		25°C		120			120		nV/√Hz								
Vn	noise voltage	f = 1 kHz		25°C	20			20											
M	Peak-to-peak	f = 0.1 Hz to 1 Hz		25°C		680			680										
VN(PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C	860			860			mV								
I <sub>n</sub>	Equivalent input noise current			25°C	0.6		0.6			fA/√Hz									
		$V_0 = 1 V \text{ to } 2 V,$	A <sub>V</sub> = 1	25°C		2.52%			2.52%										
	Total harmonic	f = 20 kHz, R <sub>L</sub> = 2 kΩ <sup>‡</sup>	A <sub>V</sub> = 10	25.0		7.01%			7.01%										
THD+N	distortion plus noise	$V_0 = 1 V \text{ to } 2 V,$	A <sub>V</sub> = 1	25°C		0.076%			0.076%										
		f = 20 kHz, R <sub>L</sub> = 2 kΩ§	A <sub>V</sub> = 10	25.0		0.147%			0.147%										
	Gain-bandwidth product	f = 1 kHz, C <sub>L</sub> = 100 pF <sup>‡</sup>	$R_L = 2 k\Omega^{\ddagger},$	25°C		480			480		kHz								
BOM	Maximum output-swing bandwidth	$V_{O}(PP) = 1 V,$ $R_L = 2 k\Omega^{\ddagger},$	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF‡	25°C	30		5°C 30		30		30		30		30		30		kHz
+	Settling time	$A_V = -1$ , Step = 1 V to 2 V,	To 0.1%	25°C		4.5			4.5		μs								
t <sub>S</sub>	$R_1 = 2 k_0 + 1$		25°C	6.8		6.8		μs											
<sup>¢</sup> m	Phase margin at unity gain	$R_{I} = 2 k\Omega^{\ddagger},$	$R_{l} = 2 k\Omega^{\ddagger}, \qquad C_{l} = 100 pF^{\ddagger}$			53°			53°										
	Gain margin	1 -		25°C		12			12		dB								

<sup>†</sup> Full range is –40°C to 85°C. <sup>‡</sup> Referenced to 1.5 V

§ Referenced to 0 V



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#### electrical characteristics at specified free-air temperature, V<sub>DD</sub> = 5 V (unless otherwise noted)

		TEAT AS	DITIONS	- +	Т	LV27210		1	[LV2721]		
	PARAMETER	TEST CON	DITIONS	TA‡	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIO	Input offset voltage					0.5	3		0.5	3	mV
αΛIΟ	Temperature coefficient of input offset voltage			Full range		1			1		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm 2.5 \text{ V},$ $V_{O} = 0,$	$V_{IC} = 0,$ R <sub>S</sub> = 50 $\Omega$	25°C		0.003			0.003		μV/m
10	Input offset current			25°C		0.5	60		0.5	60	pА
.10	input onoor ourront			Full range			150			150	P/1
IВ	Input bias current			25°C		1	60		1	60	pА
	•			Full range			150			150	
\/	Common-mode input	Da 50.0	1)// a l < E ma)/	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		v
VICR	voltage range	R <sub>S</sub> = 50 Ω,	V <sub>IO</sub>   ≤5 mV	Full range	0 to 3.5			0 to 3.5			v
	High-level output	I <sub>OH</sub> = -500 μA		0500	4.75	4.88		4.75	4.88		v
Vон	voltage	I <sub>OH</sub> = -1 mA		25°C	4.6	4.76		4.6	4.76		v
		V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 50 μA	25°C		12			12		
VOL	Low-level output voltage	V <sub>IC</sub> = 2.5 V,	c = 2.5 V, I <sub>OL</sub> = 500 μA	25°C		120			120		mV
	vollago	$v_{\rm IC} = 2.5 v_{\rm c}$	IOL = 300 μA	Full range			500			500	
	Large-signal		<b>B</b> alot	25°C	3	5		3	5		
AVD	differential voltage	$V_{IC} = 2.5 V,$ $V_{O} = 1 V \text{ to } 4 V$	$R_L = 2 k\Omega^{\ddagger}$	Full range	1			1			V/mV
	amplification	0	$R_L = 1 M\Omega^{\ddagger}$	25°C		800			800		
<sup>r</sup> id	Differential input resistance			25°C		10 <sup>12</sup>			10 <sup>12</sup>		Ω
r <sub>ic</sub>	Common-mode input resistance			25°C		1012			1012		Ω
c <sub>ic</sub>	Common-mode input capacitance	f = 10 kHz		25°C		6			6		pF
z <sub>o</sub>	Closed-loop output impedance	f = 10 kHz,	A <sub>V</sub> = 10	25°C		70			70		Ω
	Common-mode	$V_{IC} = 0$ to 2.7 V,	V <sub>O</sub> = 1.5 V,	25°C	70	85		70	85		٦D
CMRR	rejection ratio	R <sub>S</sub> = 50 Ω	<u> </u>	Full range	65			65			dB
ksvr	Supply voltage rejection ratio	$V_{DD} = 4.4 \text{ V to 8}$		25°C	80	95		80	95		dB
	$(\Delta V_{DD} / \Delta V_{IO})$	$V_{IC} = V_{DD}/2$ ,	Nie le e el	Full range	80			80			
100	Supply current		No load	25°C		110	150		110	150	
DD	Supply current	V <sub>O</sub> = 2.5 V,	NU IUau	Full range			200			200	μA

<sup>†</sup> Full range for the TLV2721C is 0°C to 70°C. Full range for the TLV2721I is – 40°C to 85°C.

‡Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T<sub>A</sub> = 150°C extrapolated to  $T_A = 25^{\circ}C$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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#### operating characteristics at specified free-air temperature, $V_{DD}$ = 5 V

				- +	Т	LV2721	C		TLV2721		
	PARAMETER	TEST CONDITIONS		TA <sup>†</sup>	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
	Slew rate at unity	V <sub>O</sub> = 1.5 V to 3.5 V,	$R_{I} = 2 k\Omega^{\ddagger},$	25°C	0.1	0.25		0.1	0.25		
SR	gain	$C_L = 100 \text{ pF}^{\ddagger}$	RL = 2 K32+,	Full range	0.05			0.05			V/µs
V	Equivalent input	f = 10 Hz		25°C		90			90		nV/√Hz
Vn	noise voltage	f = 1 kHz		25°C		19			19		nv/vHz
Peak-to-peak		f = 0.1 Hz to 1 Hz		25°C		800			800		
VN(PP)	equivalent input noise voltage	f = 0.1 Hz to 10 Hz		25°C		960			960		mV
In	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
		$V_{O} = 1.5 V \text{ to } 3.5 V,$	A <sub>V</sub> = 1	0500		2.45%			2.45%		
THD+N	Total harmonic		A <sub>V</sub> = 10	25°C		5.54%			5.54%		
THD+N	distortion plus noise	$V_{O} = 1.5 V \text{ to } 3.5 V,$	A <sub>V</sub> = 1	25°C		0.142%			0.142%		
		f = 20 kHz, R <sub>L</sub> = 2 kΩ§	A <sub>V</sub> = 10			0.257%			0.257%		
	Gain-bandwidth product	f = 1  kHz, C <sub>L</sub> = 100 pF <sup>‡</sup>	$R_L = 2 k\Omega^{\ddagger},$	25°C		510			510		kHz
B <sub>OM</sub>	Maximum output- swing bandwidth	$V_{O(PP)} = 1 V,$ R <sub>L</sub> = 2 k $\Omega^{\ddagger}$ ,	A <sub>V</sub> = 1, C <sub>L</sub> = 100 pF‡	25°C		40			40		kHz
t <sub>s</sub>	Settling time	A <sub>V</sub> = -1, Step = 1.5 V to 3.5 V,	To 0.1%	25°C		6.8			6.8		μs
۰S		R <sub>L</sub> = 2 kΩ <sup>‡</sup> , C <sub>L</sub> = 100 pF <sup>‡</sup>	To 0.01%	25°C		9.2			9.2		μο
<sup>¢</sup> m	Phase margin at unity gain	R <sub>L</sub> = 2 kΩ <sup>‡</sup> ,	C <sub>L</sub> = 100 pF‡	25°C		53°			53°		
	Gain margin	]		25°C		12			12		dB

<sup>†</sup> Full range is –40°C to 85°C. <sup>‡</sup> Referenced to 2.5 V

§ Referenced to 0 V



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## electrical characteristics at V\_DD = 3 V, T\_A = 25 $^\circ\text{C}$ (unless otherwise noted)

		теет о			TI	V2721Y	,		
	PARAMETER	IESI C	ONDITIONS		MIN	TYP	MAX	UNIT	
VIO	Input offset voltage					620		μV	
lio	Input offset current	$V_{DD} \pm = \pm 1.5 \text{ V},$ R <sub>S</sub> = 50 $\Omega$	V <sub>IC</sub> = 0,	V <sub>O</sub> = 0,		0.5	60	pА	
I <sub>IB</sub>	Input bias current	113 = 30 32				1	60	pА	
VICR	Common-mode input voltage range	V <sub>IO</sub>   ≤5 mV,	R <sub>S</sub> = 50 Ω			-0.3 to 2.2		V	
Vон	High-level output voltage	I <sub>OH</sub> = -100 μA				2.97		V	
Val		V <sub>IC</sub> = 1.5 V,	l <sub>OL</sub> = 50 μ/		15		mV		
VOL	Low-level output voltage	Low-level output voltage $V_{IC} = 1.5 \text{ V}, \qquad I_{OL} = 500 \mu\text{A}$		μA		150			
A	Large-signal differential		$R_L = 2 k\Omega^{\dagger}$	†		3			
AVD	voltage amplification	$V_{O} = 1 V \text{ to } 2 V$	R <sub>L</sub> = 1 MΩ	†	250			V/mV	
<sup>r</sup> id	Differential input resistance					1012		Ω	
r <sub>ic</sub>	Common-mode input resistance					1012		Ω	
c <sub>ic</sub>	Common-mode input capacitance	f = 10 kHz				6		pF	
z <sub>o</sub>	Closed-loop output impedance	f = 10 kHz,	A <sub>V</sub> = 10			90		Ω	
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V,	V <sub>O</sub> = 0,	R <sub>S</sub> = 50 Ω		82		dB	
ksvr	Supply voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 2.7 \text{ V to 8 V},$	V <sub>IC</sub> = 0,	No load		95		dB	
IDD	Supply current	V <sub>O</sub> = 0,	No load			100		μA	

<sup>†</sup>Referenced to 1.5 V

## electrical characteristics at V\_DD = 5 V, T\_A = 25 $^\circ\text{C}$ (unless otherwise noted)

		TEST			TI	_V2721Y	·		
	PARAMETER	IESI C	ONDITIONS		MIN	TYP	MAX	UNIT	
VIO	Input offset voltage					610		μV	
١O	Input offset current	$V_{DD} \pm = \pm 1.5 V,$ Rs = 50 $\Omega$	$V_{IC} = 0,$	V <sub>O</sub> = 0,		0.5	60	pА	
I <sub>IB</sub>	Input bias current	115 = 30 32				1	60	pА	
VICR	Common-mode input voltage range	V <sub>IO</sub>   ≤5 mV,	R <sub>S</sub> = 50 Ω			-0.3 to 4.2		V	
VOH	High-level output voltage	I <sub>OH</sub> = -500 μA				4.88		V	
Max	Low-level output voltage	V <sub>IC</sub> = 2.5 V,	loL = 50 μ.	A		12		mV	
VOL	Low-level output voltage	V <sub>IC</sub> = 2.5 V,	I <sub>OL</sub> = 500	μA		120		IIIV	
A	Large-signal differential		$R_L = 2 k\Omega^{\dagger}$	t		5		\//ma\/	
AVD	voltage amplification	$V_{O} = 1 V \text{ to } 4 V$	R <sub>L</sub> = 1 MΩ	1	800			V/mV	
<sup>r</sup> id	Differential input resistance					1012		Ω	
ric	Common-mode input resistance					1012		Ω	
cic	Common-mode input capacitance	f = 10 kHz				6		pF	
z <sub>o</sub>	Closed-loop output impedance	f = 10 kHz,	A <sub>V</sub> = 10			70		Ω	
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = 0 to 1.7 V,	V <sub>O</sub> = 0,	R <sub>S</sub> = 50 Ω		85		dB	
<b>k</b> SVR	Supply voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	V <sub>DD</sub> = 2.7 V to 8 V,	$V_{IC} = 0,$	No load		95		dB	
IDD	Supply current	V <sub>O</sub> = 0,	No load			110		μA	
- <i>i</i>									

<sup>†</sup>Referenced to 2.5 V



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#### **TYPICAL CHARACTERISTICS**

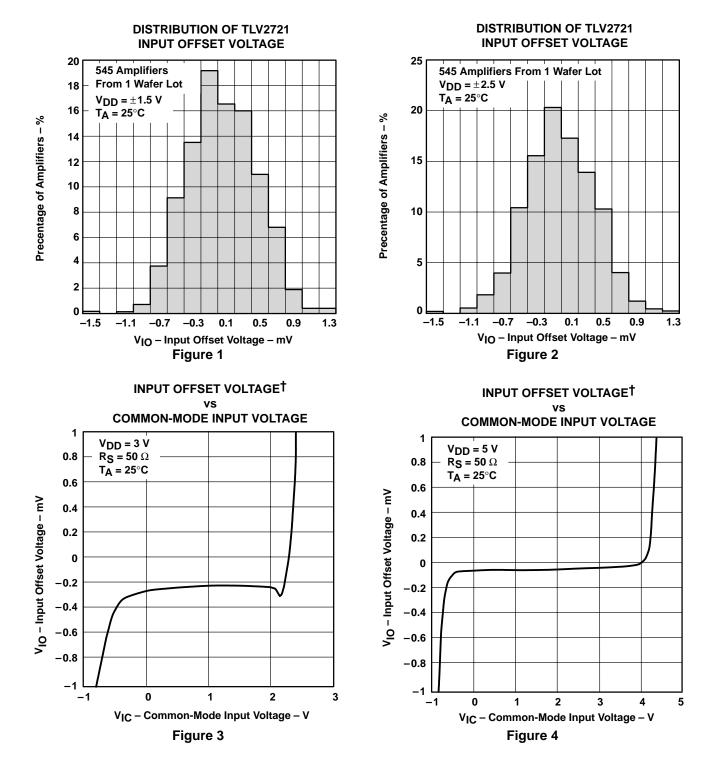
#### **Table of Graphs**

			FIGURE
VIO	Input offset voltage	Distribution vs Common-mode input voltage	1, 2 3, 4
αVIO	Input offset voltage temperature coefficient	Distribution	5, 6
IIB/IIO	Input bias and input offset currents	vs Free-air temperature	7
VI	Input voltage	vs Supply voltage vs Free-air temperature	8 9
Vон	High-level output voltage	vs High-level output current	10, 13
VOL	Low-level output voltage	vs Low-level output current	11, 12, 14
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	15
IOS	Short-circuit output current	vs Supply voltage vs Free-air temperature	16 17
VO	Output voltage	vs Differential input voltage	18, 19
AVD	Differential voltage amplification	vs Load resistance	20
AVD	Large signal differential voltage amplification	vs Frequency vs Free-air temperature	21, 22 23, 24
z <sub>o</sub>	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	27 28
ksvr	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	29, 30 31
IDD	Supply current	vs Supply voltage	32
SR	Slew rate	vs Load capacitance vs Free-air temperature	33 34
Vo	Inverting large-signal pulse response		35, 36
Vo	Voltage-follower large-signal pulse response		37, 38
Vo	Inverting small-signal pulse response		39, 40
Vo	Voltage-follower small-signal pulse response		41, 42
Vn	Equivalent input noise voltage	vs Frequency	43, 44
	Input noise voltage (referred to input)	Over a 10-second period	45
THD + N	Total harmonic distortion plus noise	vs Frequency	46
	Gain-bandwidth product	vs Free-air temperature vs Supply voltage	47 48
<sup>¢</sup> m	Phase margin	vs Frequency vs Load capacitance	21, 22 51, 52
	Gain margin	vs Load capacitance	49, 50
B <sub>1</sub>	Unity-gain bandwidth	vs Load capacitance	53, 54



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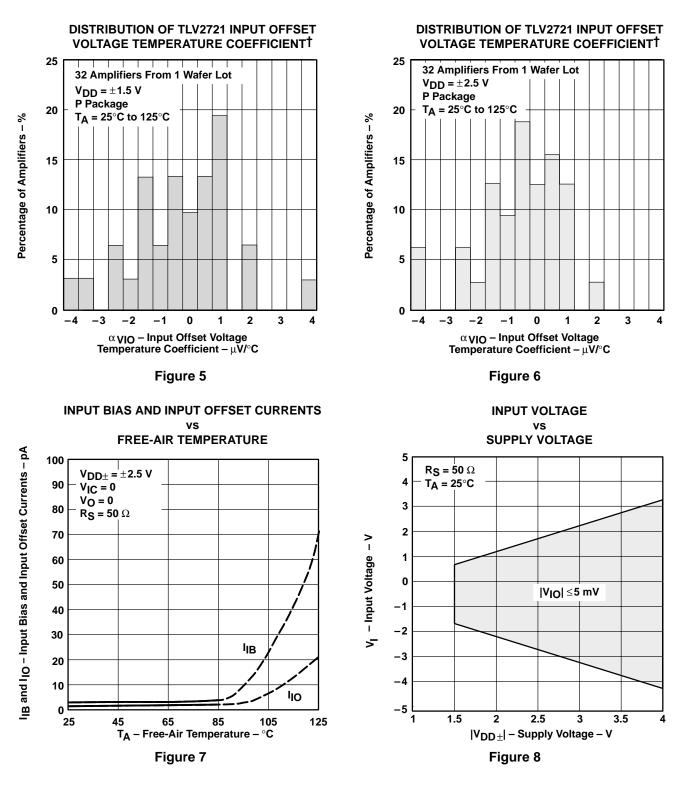
#### **TYPICAL CHARACTERISTICS**





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**TYPICAL CHARACTERISTICS** 

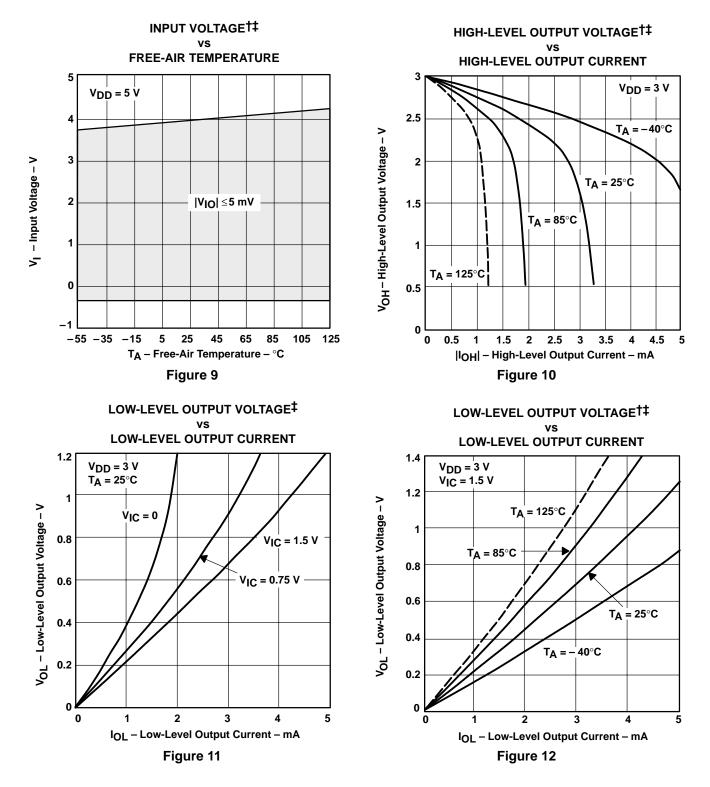


<sup>†</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



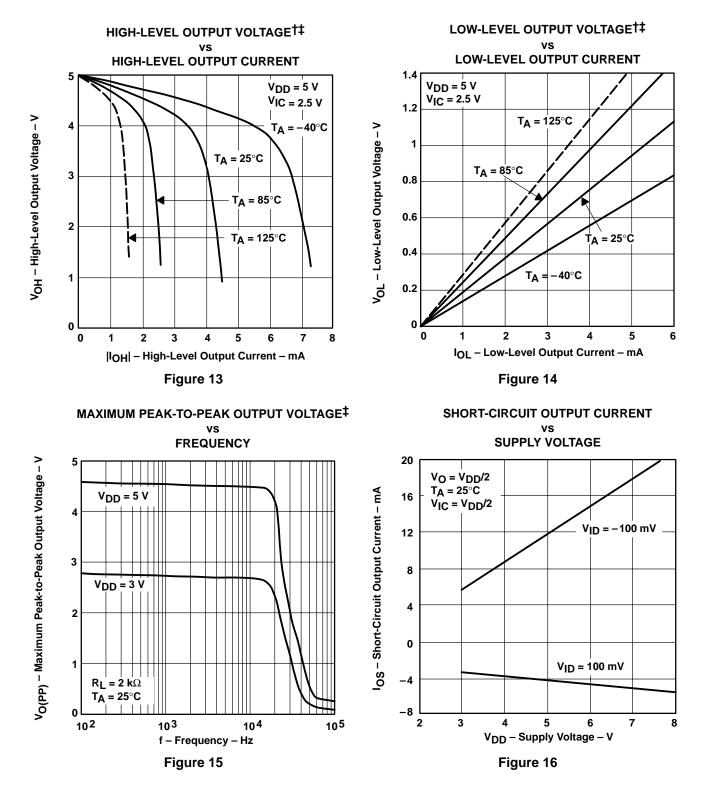
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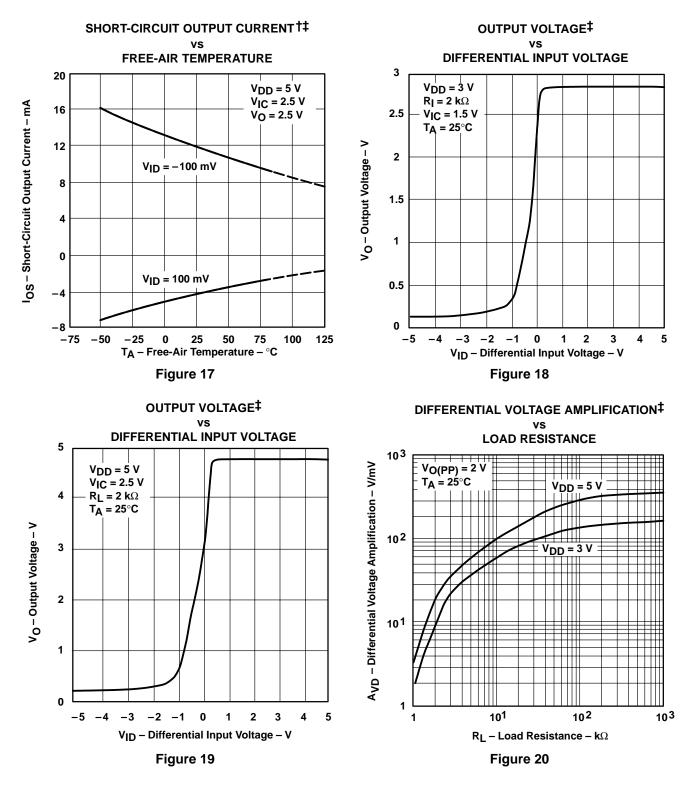


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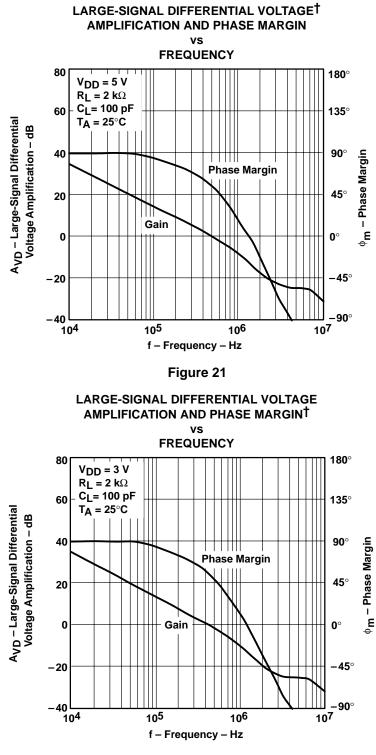
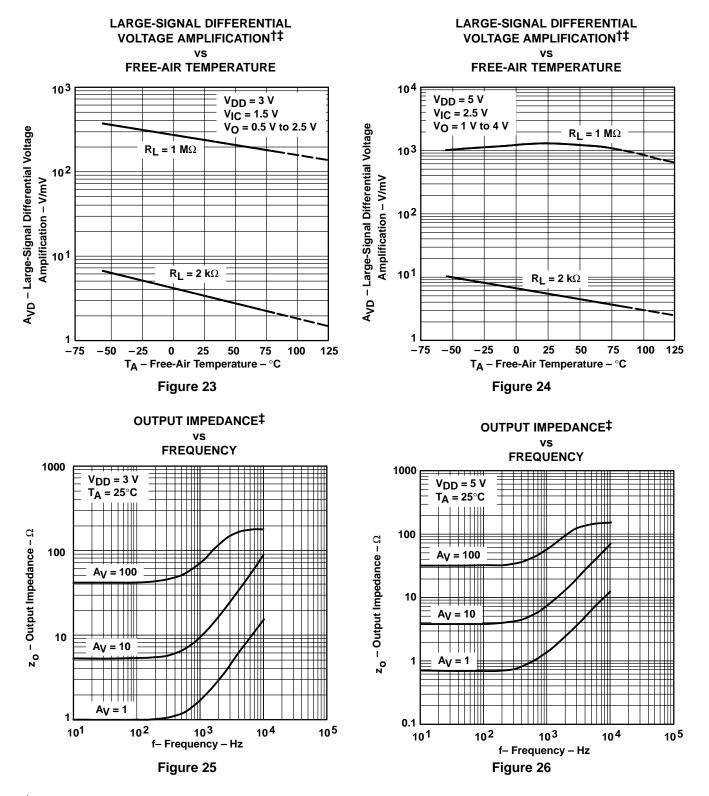


Figure 22



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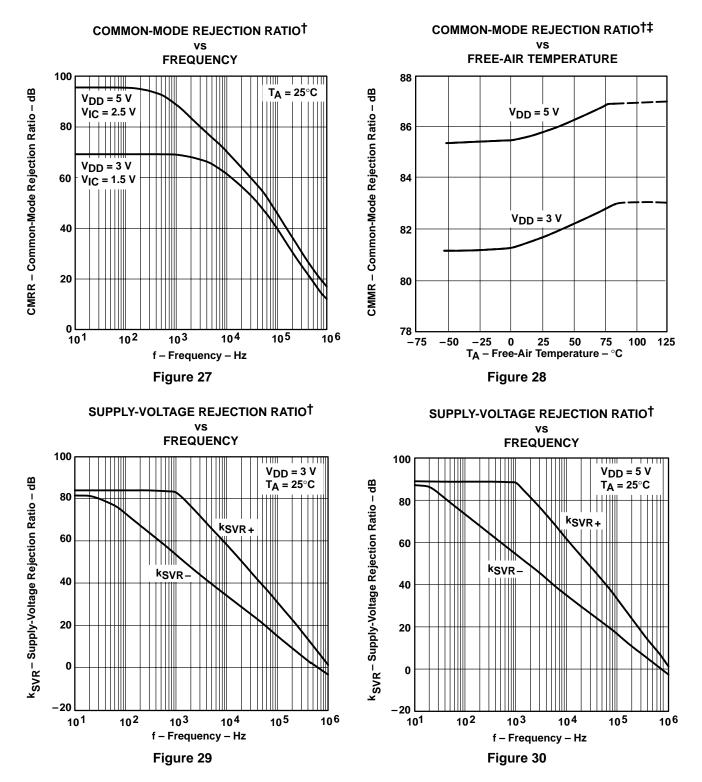
**TYPICAL CHARACTERISTICS** 





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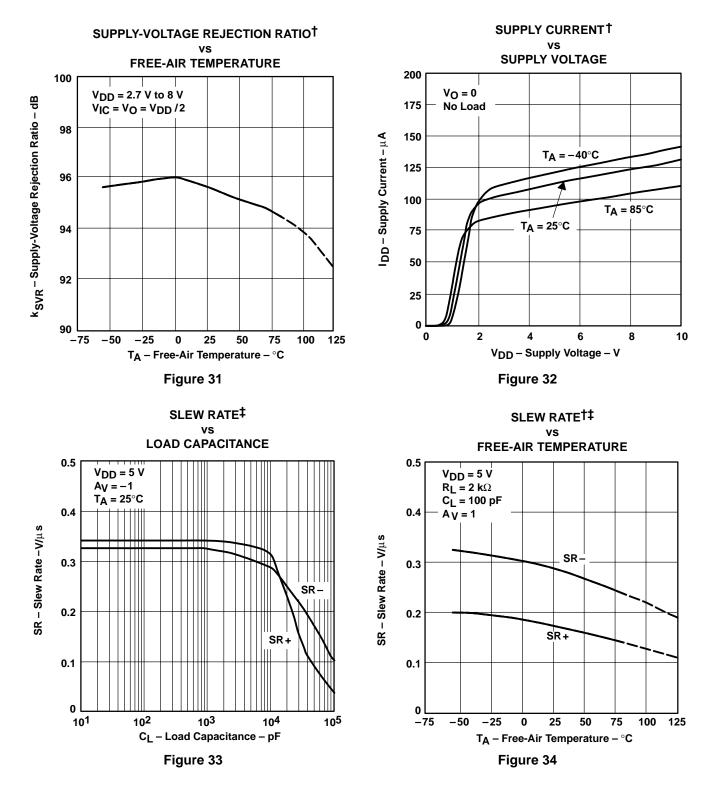
**TYPICAL CHARACTERISTICS** 



<sup>†</sup> For all curves where  $V_{DD}$  = 5 V, all loads are referenced to 2.5 V. For all curves where  $V_{DD}$  = 3 V, all loads are referenced to 1.5 V. <sup>‡</sup> Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



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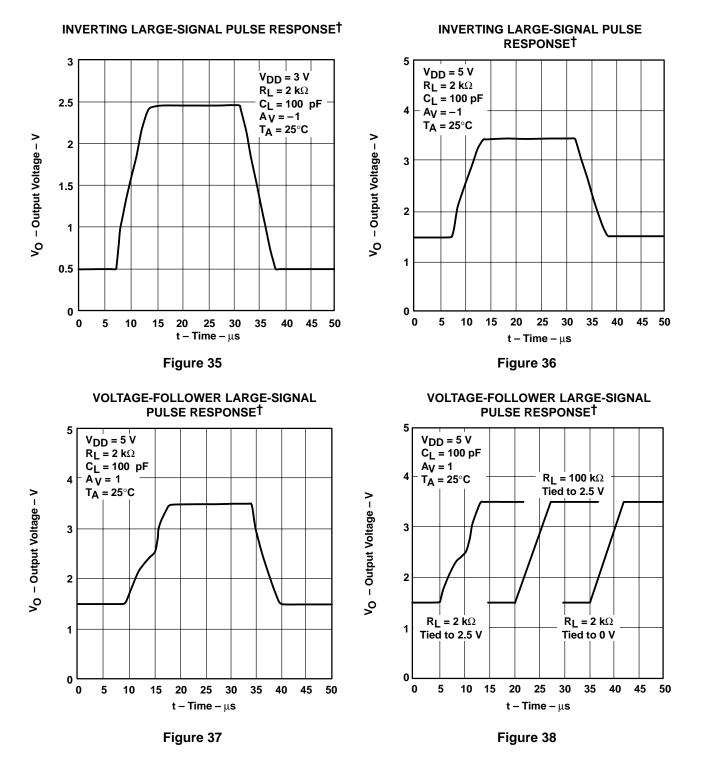


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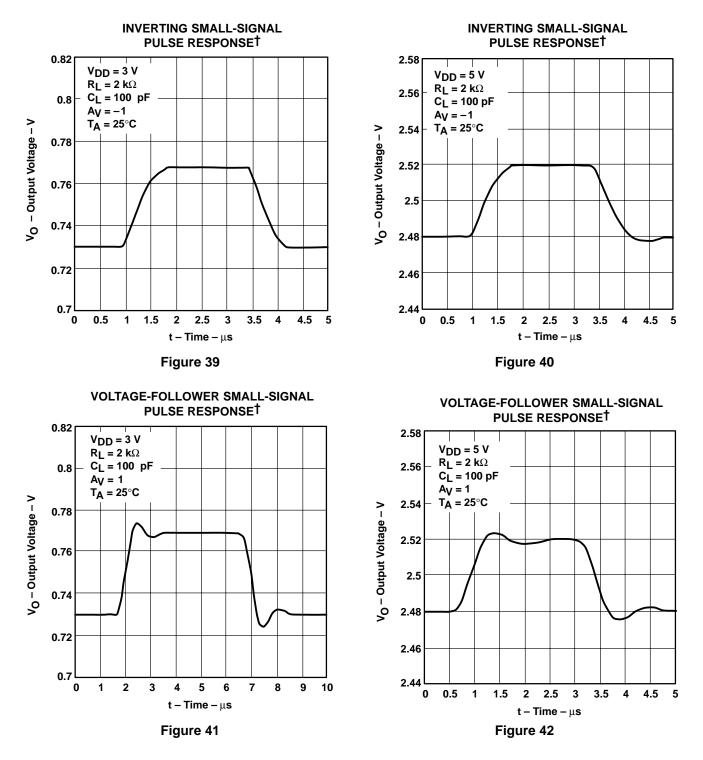
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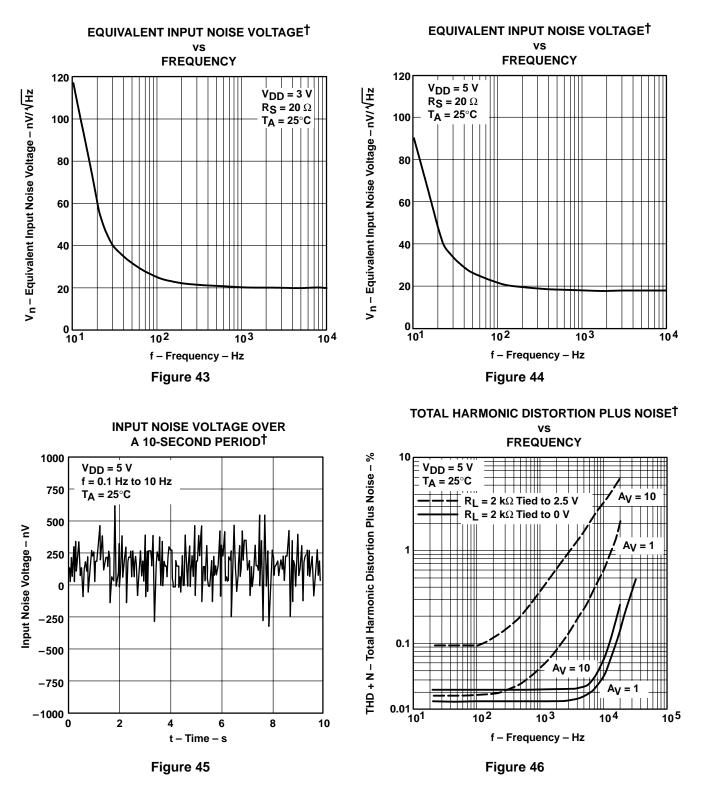
#### **TYPICAL CHARACTERISTICS**





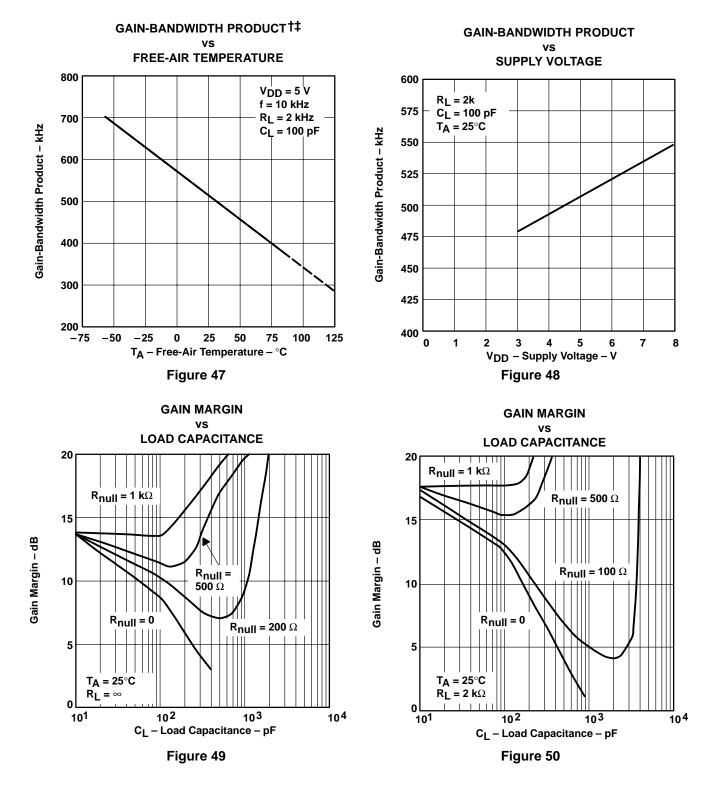
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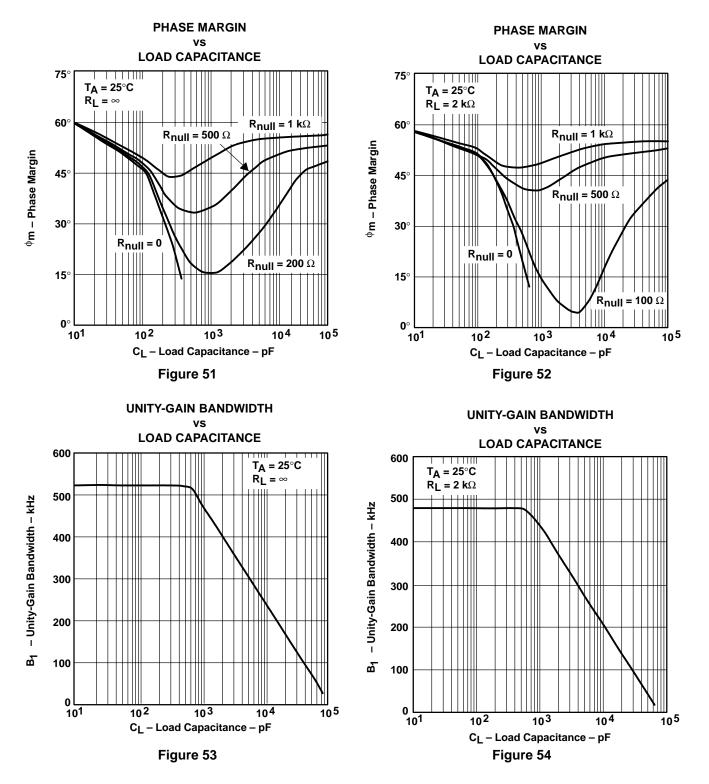


#### **TYPICAL CHARACTERISTICS**



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#### TYPICAL CHARACTERISTICS





#### APPLICATION INFORMATION

#### driving large capacitive loads

The TLV2721 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 49 through Figure 54 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins ( $R_{null} = 0$ ).

A small series resistor (R<sub>null</sub>) at the output of the device (Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 49 through Figure 52 show the effects of adding series resistances of 100  $\Omega$ , 200  $\Omega$ , 500  $\Omega$ , and 1 k $\Omega$ . The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta \phi_{m1} = \tan^{-1} \left( 2 \times \pi \times \text{UGBW} \times \text{R}_{null} \times \text{C}_{L} \right)$$
(1)

Where :

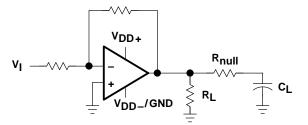
 $\Delta \phi_{m1}$  = Improvement in phase margin

UGBW = Unity-gain bandwidth frequency

R<sub>null</sub> = Output series resistance

 $C_1$  = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (Figure 53 and Figure 54). To use equation 1, UGBW must be approximated from Figure 54 and Figure 55.





The TLV2721 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500  $\mu$ A and source 1 mA at V<sub>DD</sub> = 5 V at a maximum quiescent I<sub>DD</sub> of 200  $\mu$ A. This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as  $2 k\Omega$ , the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 37. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 38 illustrates two 2-kΩ load conditions. The first load condition shows the distortion seen for a 2-kΩ load tied to 2.5 V. The third load condition in Figure 38 shows no distortion for a 2-kΩ load tied to 0 V.
- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 38 illustrates the difference seen on the output for a  $2-k\Omega$  load and a  $100-k\Omega$  load with both tied to 2.5 V.
- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.



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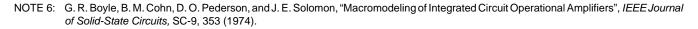
#### APPLICATION INFORMATION

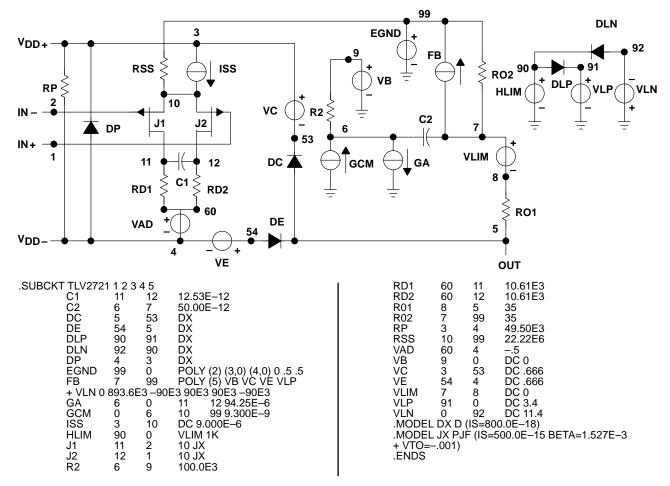
#### macromodel information

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel (see Note 6) and subcircuit in Figure 56 are generated using the TLV2721 typical electrical and operating characteristics at  $T_A = 25^{\circ}C$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit







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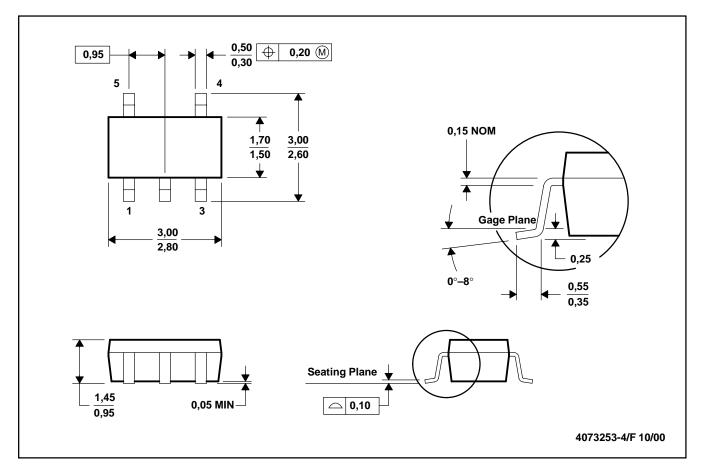


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#### **MECHANICAL INFORMATION**

#### PLASTIC SMALL-OUTLINE

#### DBV (R-PDSO-G5)



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-178



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