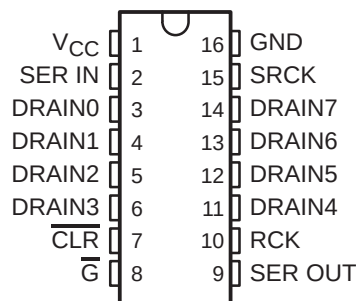


TPIC6C595 POWER LOGIC 8-BIT SHIFT REGISTER

SLIS061B – JULY 1998 – REVISED MAY 2004

- Low $r_{DS(on)}$. . . 7 Ω Typ
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS Transistor Outputs of 100-mA Continuous Current
- 250-mA Current Limit Capability
- ESD Protection . . . 2500 V
- Output Clamp Voltage . . . 33 V
- Devices Are Cascadable
- Low Power Consumption

D OR N PACKAGE
(TOP VIEW)

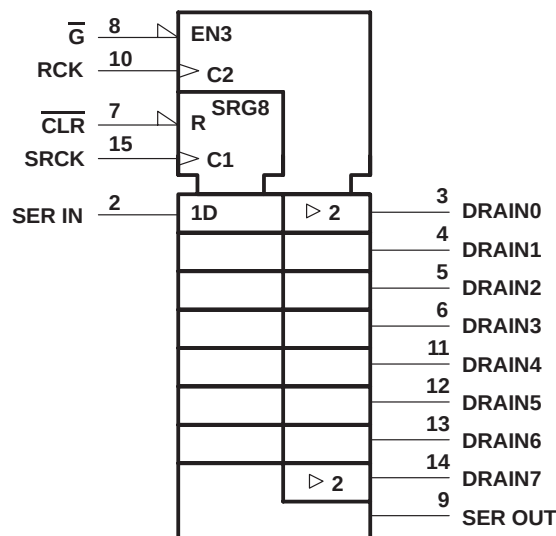


description

The TPIC6C595 is a monolithic, medium-voltage, low-current power 8-bit shift register designed for use in systems that require relatively moderate load power such as LEDs. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other low-current or medium-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift register clock (SRCK) and the register clock (RCK), respectively. The device transfers data out the serial output (SER OUT) port on the rising edge of SRCK. The storage register transfers data to the output buffer when shift register clear ($\overline{CLR}$) is high. When $\overline{CLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability. The SER OUT allows for cascading of the data from the shift register to additional devices.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.



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INSTRUMENTS**

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TPIC6C595

POWER LOGIC 8-BIT SHIFT REGISTER

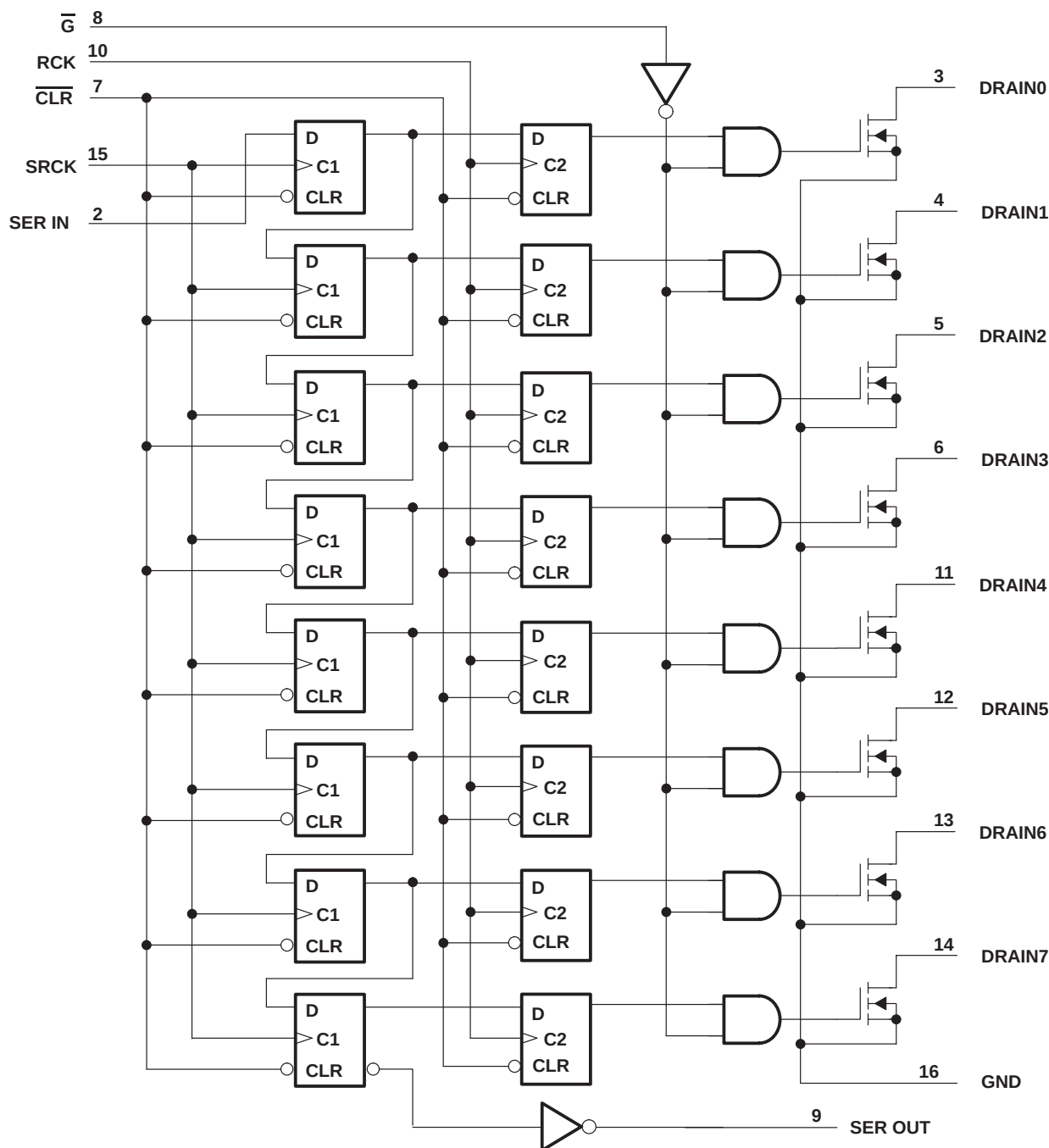
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description (continued)

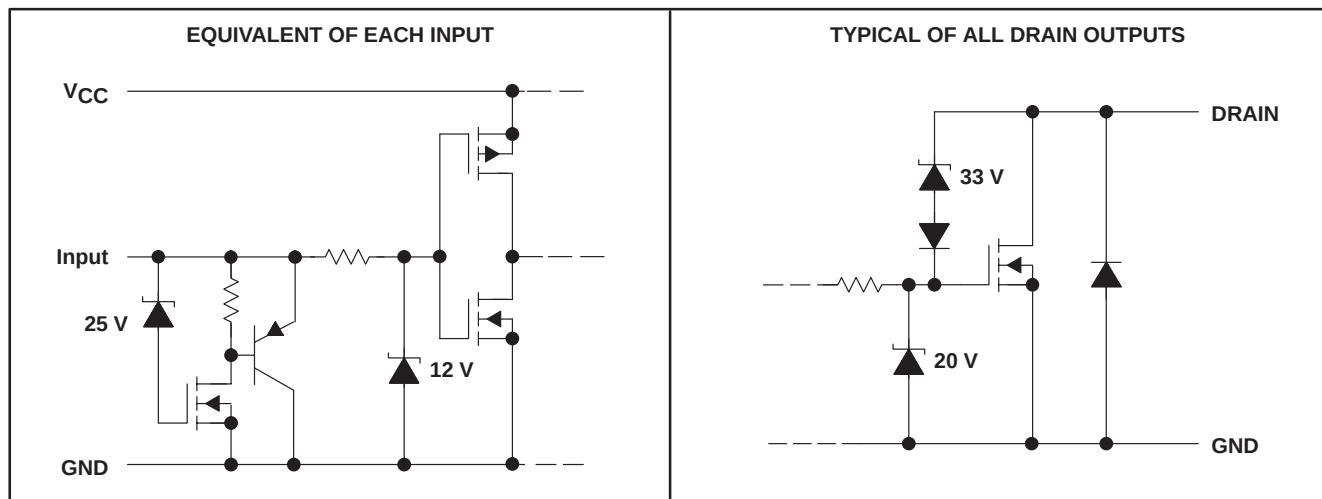
Outputs are low-side, open-drain DMOS transistors with output ratings of 33 V and 100 mA continuous sink-current capability. Each output provides a 250-mA maximum current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 2500 V of ESD protection when tested using the human-body model and the 200-V machine model.

The TPIC6C595 is characterized for operation over the operating case temperature range of -40°C to 125°C .

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)[†]

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	-0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	33 V
Continuous source-to-drain diode anode current	250 mA
Pulsed source-to-drain diode anode current (see Note 3)	500 mA
Pulsed drain current, each output, all outputs on, I_D , $T_C = 25^\circ\text{C}$ (see Note 3)	250 mA
Continuous drain current, each output, all outputs on, I_D , $T_C = 25^\circ\text{C}$	100 mA
Peak drain current single output, I_{DM} , $T_C = 25^\circ\text{C}$ (see Note 3)	250 mA
Single-pulse avalanche energy, E_{AS} (see Figure 4)	30 mJ
Avalanche current, I_{AS} (see Note 4)	200 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	-40°C to 150°C
Operating case temperature range, T_C	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to GND.
 2. Each power DMOS source is internally connected to GND.
 3. Pulse duration $\leq 100 \mu\text{s}$ and duty cycle $\leq 2\%$.
 4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, $L = 1.5 \text{ H}$, $I_{AS} = 200 \text{ mA}$ (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
D	1087 mW	8.7 mW/°C	217 mW
N	1470 mW	11.7 mW/°C	294 mW

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recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, $T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$, all outputs on (see Notes 3 and 5 and Figure 11)		250	mA
Setup time, SER IN high before SRCK $\uparrow$, t_{SU} (see Figure 2)	20		ns
Hold time, SER IN high after SRCK $\uparrow$, t_H (see Figure 2)	20		ns
Pulse duration, t_W (see Figure 2)	40		ns
Operating case temperature, T_C	-40	125	$^\circ\text{C}$

electrical characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 1\text{ mA}$	33	37		V
V_{SD} Source-to-drain diode forward voltage	$I_F = 100\text{ mA}$		0.85	1.2	V
V_{OH} High-level output voltage, SER OUT	$I_{OH} = -20\text{ }\mu\text{A}$, $V_{CC} = 4.5\text{ V}$	4.4	4.49		V
	$I_{OH} = -4\text{ mA}$, $V_{CC} = 4.5\text{ V}$	4	4.2		
V_{OL} Low-level output voltage, SER OUT	$I_{OL} = 20\text{ }\mu\text{A}$, $V_{CC} = 4.5\text{ V}$		0.005	0.1	V
	$I_{OL} = 4\text{ mA}$, $V_{CC} = 4.5\text{ V}$		0.3	0.5	
I_{IH} High-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$			1	μA
I_{IL} Low-level input current	$V_{CC} = 5.5\text{ V}$, $V_I = 0$			-1	μA
I_{CC} Logic supply current	$V_{CC} = 5.5\text{ V}$	All outputs off		20	200
		All outputs on		150	
$I_{CC}(\text{FRQ})$ Logic supply current at frequency	$f_{SRCK} = 5\text{ MHz}$, $C_L = 30\text{ pF}$, All outputs off, See Figures 2 and 6		1.2	5	mA
I_N Nominal current	$V_{DS(\text{on})} = 0.5\text{ V}$, $T_C = 85^\circ\text{C}$, $I_N = I_D$, See Notes 5, 6, and 7		90		mA
I_{DSX} Off-state drain current	$V_{DS} = 30\text{ V}$, $V_{CC} = 5.5\text{ V}$		0.1	0.2	μA
	$V_{DS} = 30\text{ V}$, $T_C = 125^\circ\text{C}$, $V_{CC} = 5.5\text{ V}$		0.15	0.3	
$r_{DS(\text{on})}$ Static drain-source on-state resistance	$I_D = 50\text{ mA}$, $V_{CC} = 4.5\text{ V}$	See Notes 5 and 6 and Figures 7 and 8	6.5	9	Ω
	$I_D = 50\text{ mA}$, $T_C = 125^\circ\text{C}$, $V_{CC} = 4.5\text{ V}$		9.9	12	
	$I_D = 100\text{ mA}$, $V_{CC} = 4.5\text{ V}$		6.8	10	

- NOTES: 3. Pulse duration $\leq 100\text{ }\mu\text{s}$ and duty cycle $\leq 2\%$.
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ\text{C}$.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$

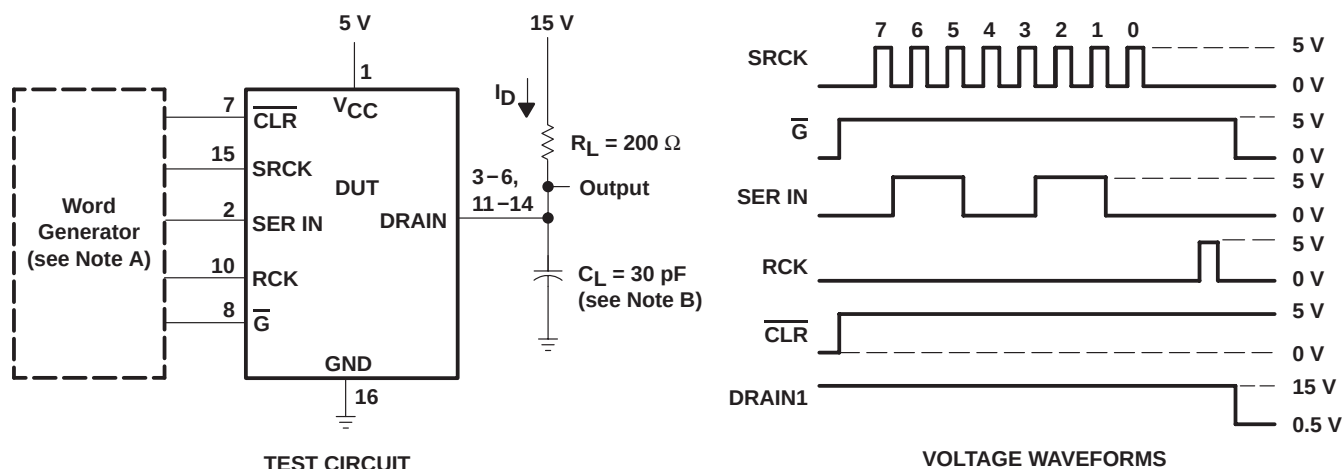
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	$C_L = 30\text{ pF}$, $I_D = 75\text{ mA}$, See Figures 1, 2, and 9		80		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			50		ns
t_{pd}	Propagation delay time, SRCK to SEROUT			20		ns
t_r	Rise time, drain output			100		ns
t_f	Fall time, drain output			80		ns
t_a	Reverse-recovery-current rise time	$I_F = 100\text{ mA}$, $di/dt = 10\text{ A}/\mu\text{s}$, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			120		

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	D package		115	$^\circ\text{C}/\text{W}$
		N package		85	

PARAMETER MEASUREMENT INFORMATION



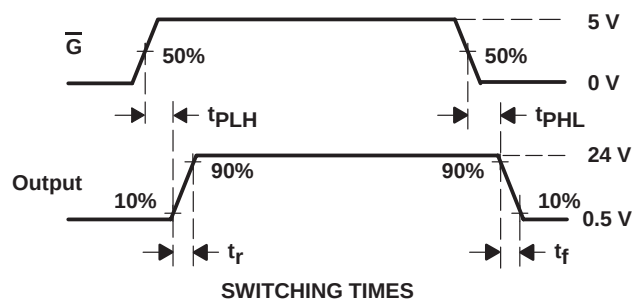
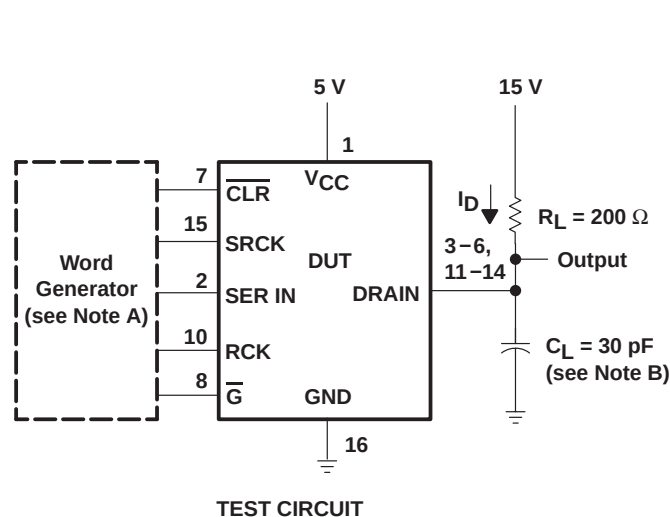
NOTES: A. The word generator has the following characteristics: $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$, $t_w = 300\text{ ns}$, pulsed repetition rate (PRR) = 5 kHz , $Z_O = 50\text{ }\Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

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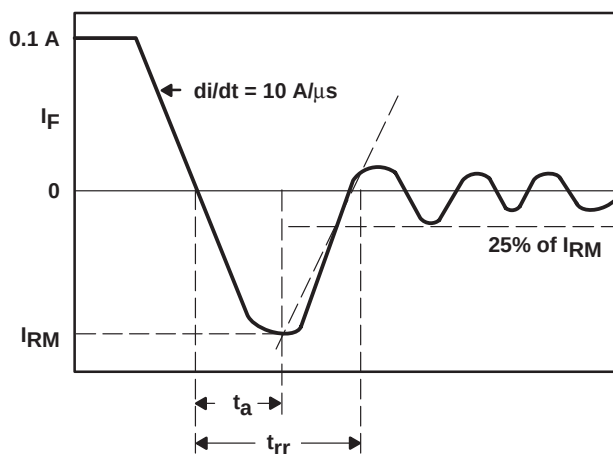
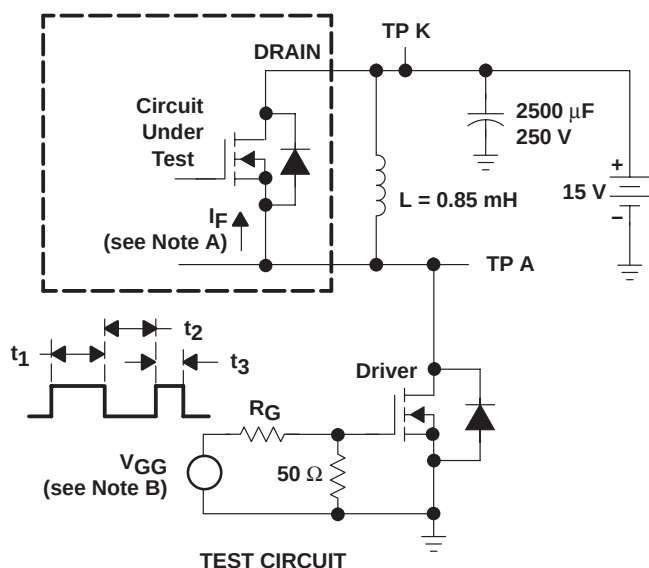
PARAMETER MEASUREMENT INFORMATION



INPUT SETUP AND HOLD WAVEFORMS

- NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50$ Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

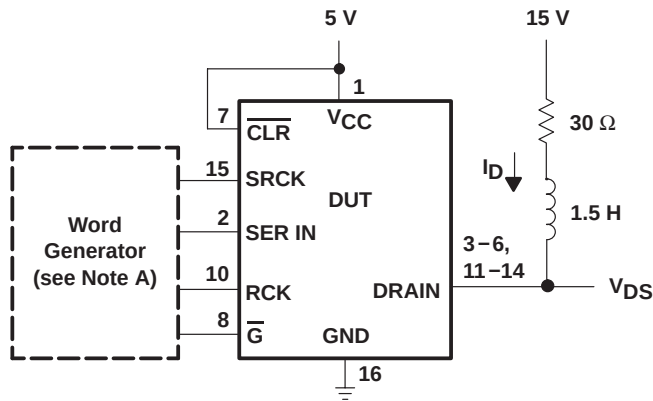


CURRENT WAVEFORM

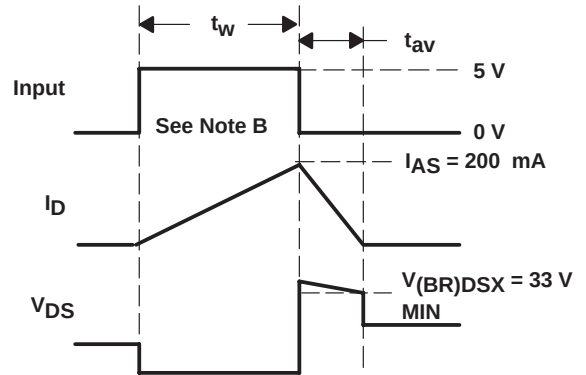
- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for $di/dt = 10$ A/μs. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10$ μs, $t_2 = 7$ μs, and $t_3 = 3$ μs.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT

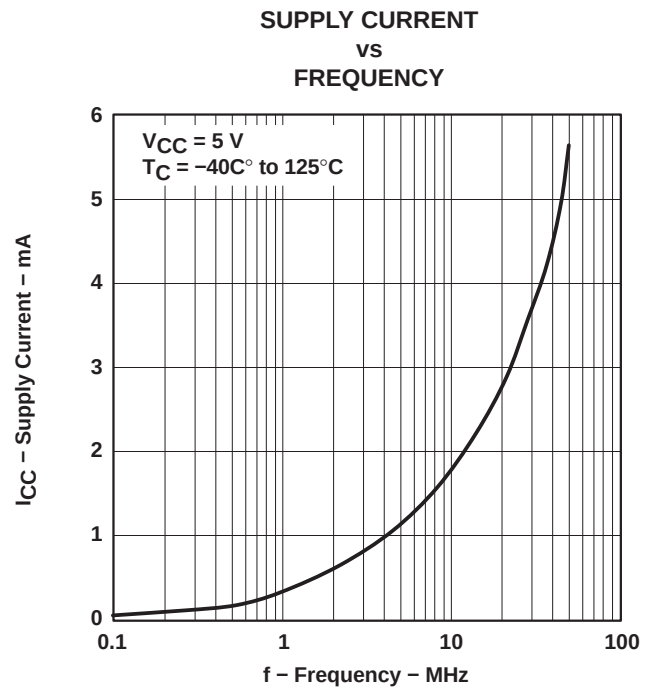
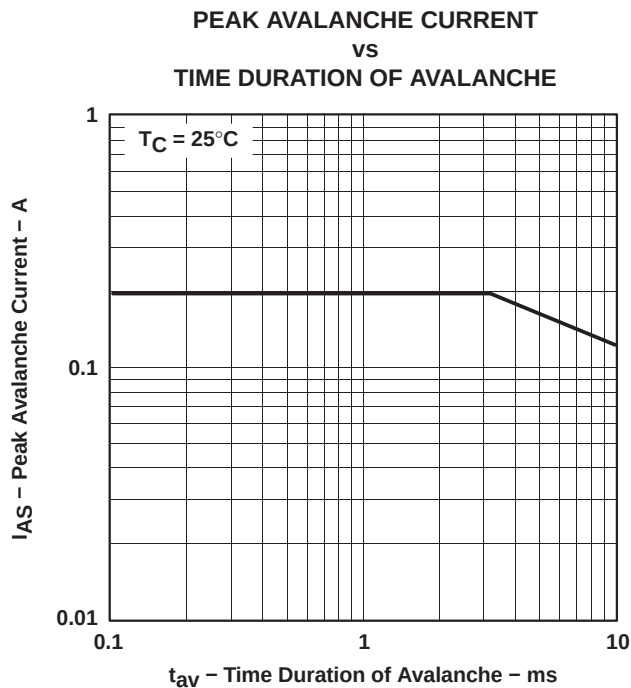


VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 200$ mA.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS



TPIC6C595

POWER LOGIC 8-BIT SHIFT REGISTER

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TYPICAL CHARACTERISTICS

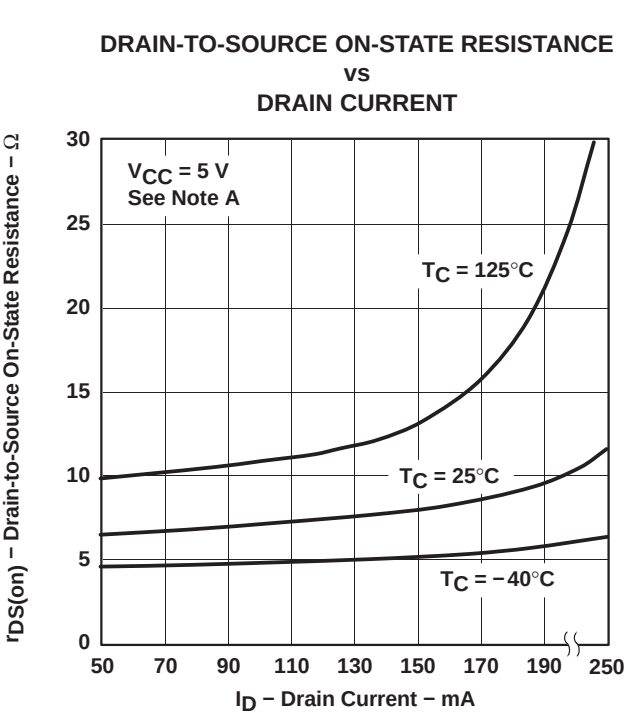


Figure 7

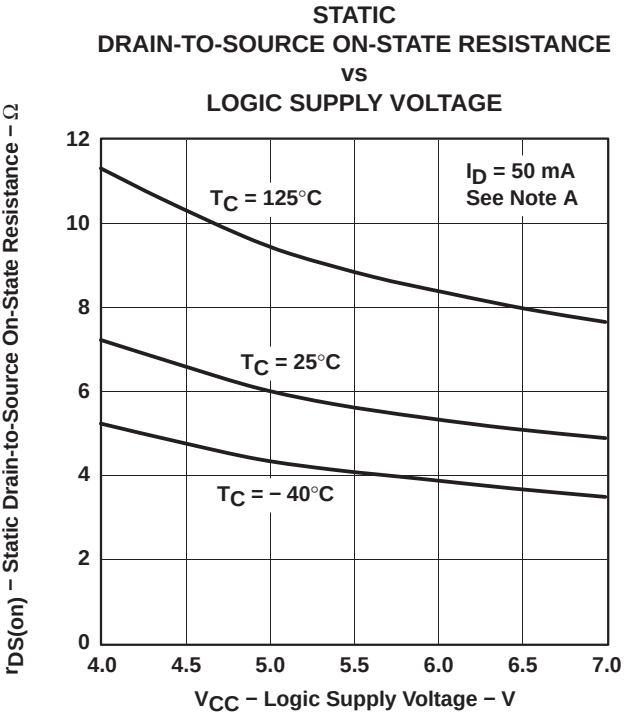


Figure 8

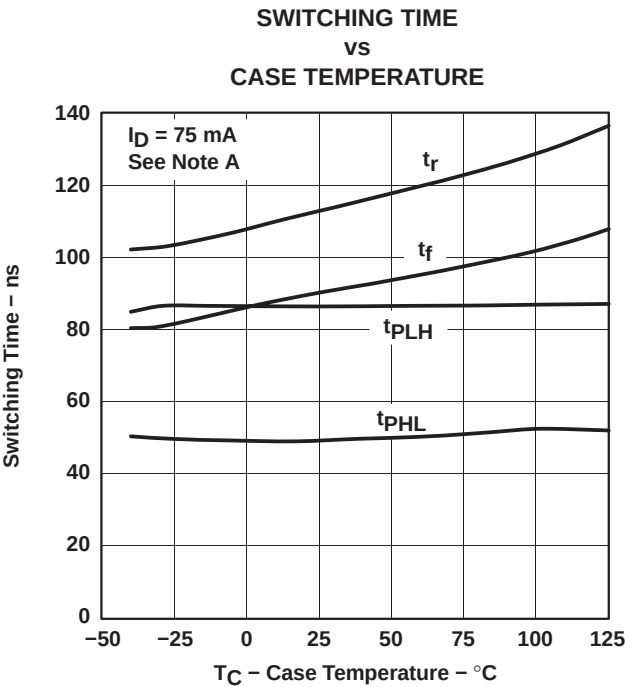


Figure 9

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

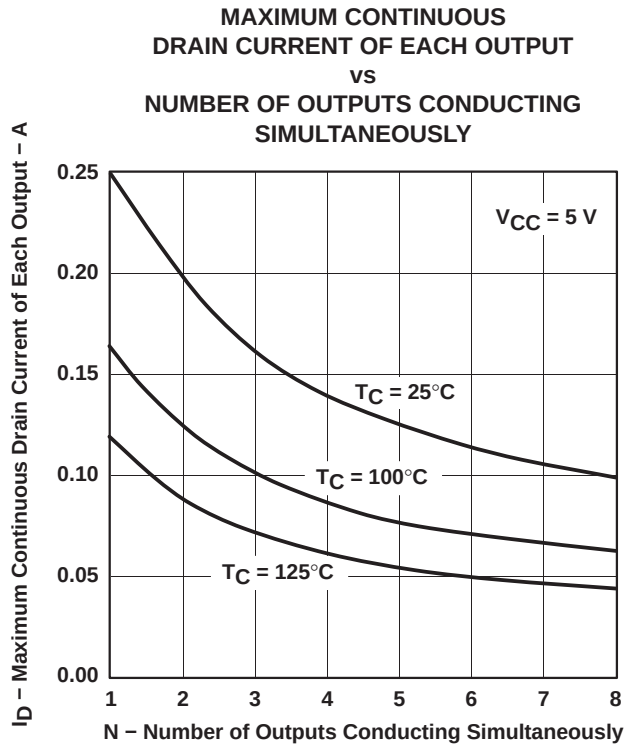


Figure 10

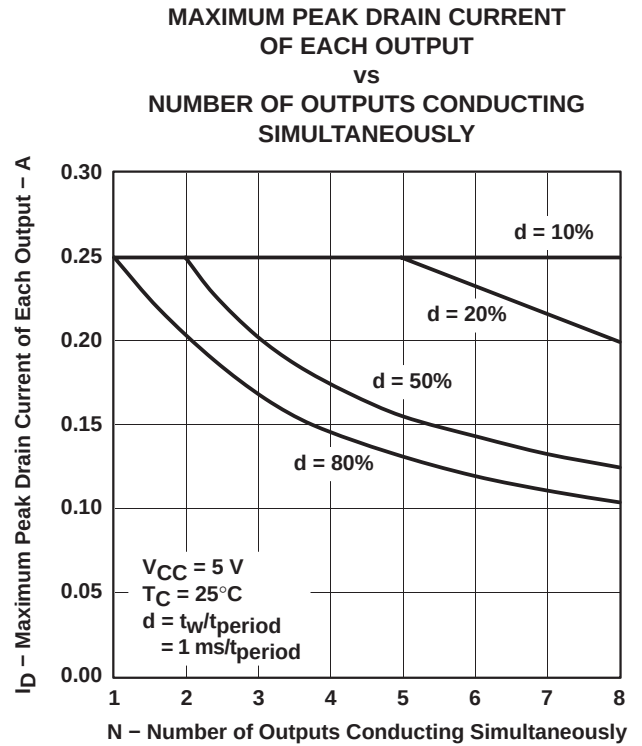


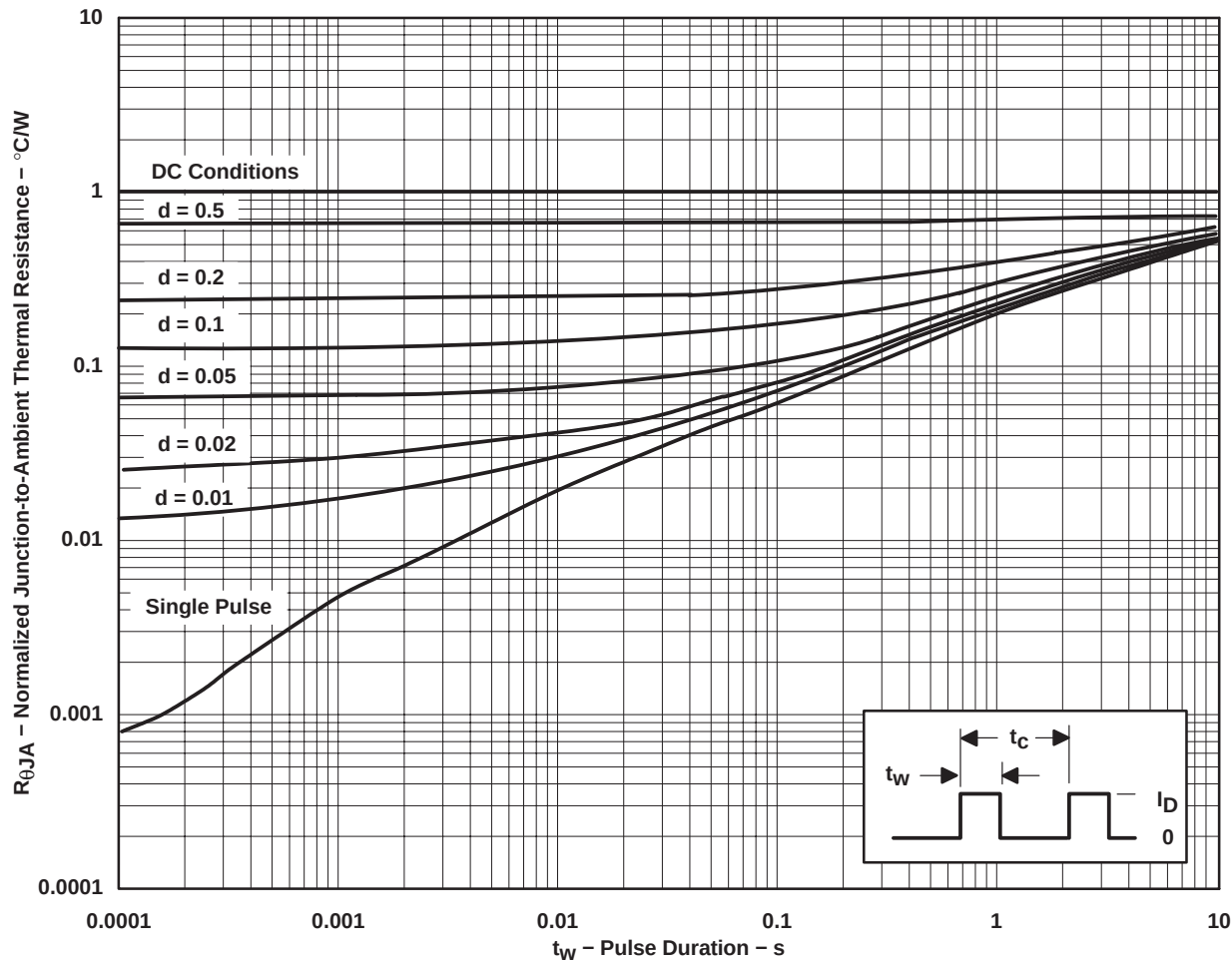
Figure 11

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THERMAL INFORMATION

D PACKAGE[†]
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
VS
PULSE DURATION



[†] Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t) R_{\theta JA}$
 t_W = pulse duration
 t_C = cycle time
 d = duty cycle = t_W/t_C

Figure 12

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