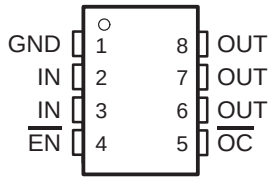
- **95-mΩ Maximum (5-V Input) High-Side MOSFET Switch**
- **Short-Circuit Protection and Thermal Protection**
- **Logic Overcurrent Output**
- **4-V to 7-V Operating Range**
- **Enable Input Compatible With 3-V and 5-V Logic**
- **Controlled Rise and Fall Times Limit Current Surges and Minimize EMI**
- **Undervoltage Lockout Ensures That Switch is Off at Start-Up**
- **10-μA Maximum Standby Current**
- **Available in Space-Saving 8-Pin SOIC and 8-Pin PDIP**
- **0°C to 125°C Operating Junction Temperature Range**
- **12-kV Output, 6-kV Input Electrostatic-Discharge Protection**

D OR P PACKAGE
(TOP VIEW)



description

The TPS2014 and TPS2015 power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. The high-side switch is a 95-mΩ n-channel MOSFET. The switch is controlled by a logic enable that is compatible with 3-V and 5-V logic. Gate drive is provided by an internal charge pump designed to control the power switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 4 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS20xx limits the output current to a safe level by switching into a constant-current mode, and the overcurrent logic output is set to low. Continuous heavy overloads and short circuits will increase the power dissipation in the switch and cause the junction temperature to rise. A thermal protection circuit is implemented, which shuts the switch off to prevent damage when the junction temperature exceeds its thermal limit. An undervoltage lockout is provided to ensure the switch is in the off state at start-up.

The TPS2014 and TPS2015 differ only in short-circuit current limits. The TPS2014 is designed to limit at 1.2 A load and the TPS2015 limits at 2 A (see the available options table). The TPS20xx is available in 8-pin small-outline integrated circuit (SOIC) and 8-pin PDIP packages, and operates over a junction temperature range of 0°C to 125°C.

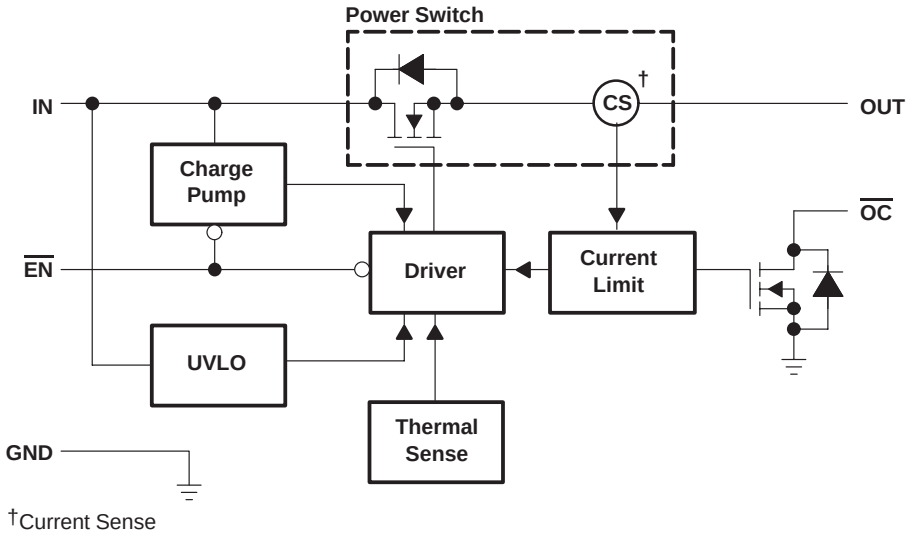
AVAILABLE OPTIONS

T_A	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
			SOIC (D)†	PDIP (P)	
0°C TO 85°C	0.6 A	1.2 A	TPS2014D	TPS2014P	TPS2014Y
	1 A	2 A	TPS2015D	TPS2015P	TPS2015Y

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2014DR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

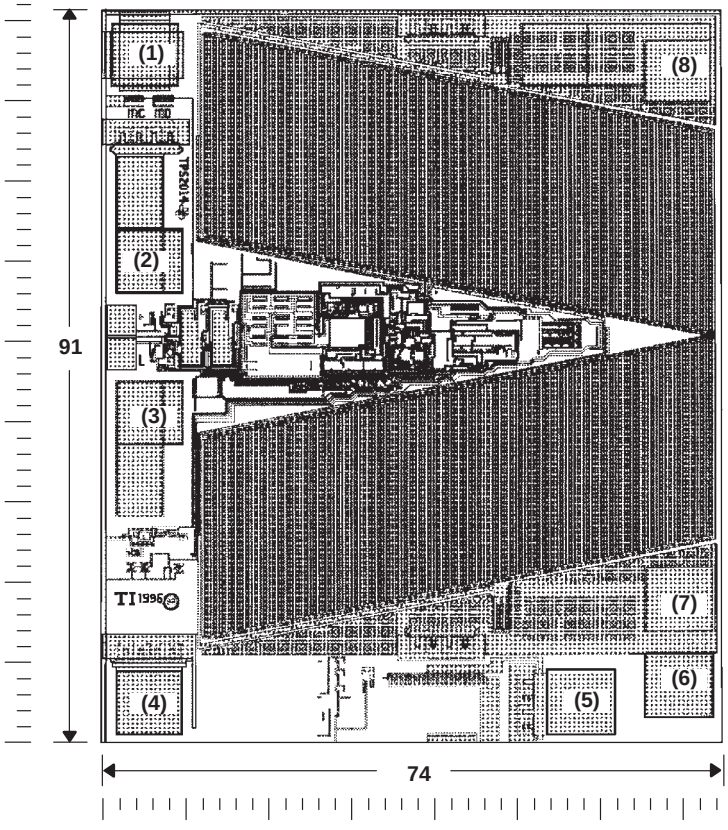
functional block diagram

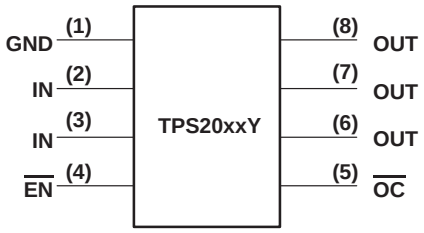


TPS20xxY chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS20xx. Ultrasonic bonding may be used on the doped aluminium bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAl

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{EN}$	4	I	Enable input. Logic low at $\overline{EN}$ turns the power switch on.
GND	1	I	Ground
$\overline{IN}$	2, 3	I	Input voltage
$\overline{OC}$	5	O	$\overline{OC}$ is asserted active low during a fault condition.
OUT	6–8	O	Power switch output

detailed description

power switch

The power switch is an n-channel MOSFET with a maximum on-state resistance of 95 mΩ ($V_{I(IN)}$ = 5 V), configured as a high-side switch.

charge pump

An internal 100-kHz charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 4 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range instead of the microsecond or nanosecond range for a standard FET.

enable ($\overline{EN}$)

A logic high on $\overline{EN}$ turns off the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA. A logic zero input restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{OC}$)

$\overline{OC}$ is an open-drain logic output that is asserted (active low) when an overload or short circuit is encountered. The output remains asserted until the overload or short-circuit condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET provides a much more efficient way to measure current than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its linear region, which switches the output into a constant current mode and simply holds the current constant while varying the voltage on the load.

thermal sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately to 180°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

An internal voltage sense monitors the input voltage. When the input voltage is below 3.2 V nominal, a control signal turns off the power switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, V_I (see Note1) . . . . . –0.3 V to 7 V
Output voltage range, V_O (see Note1) . . . . . –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, V_I at $\overline{EN}$ . . . . . –0.3 V to 7 V
Continuous output current, I_O . . . . . internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . 0°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
P	1175 mW	9.4 mW/°C	752 mW	235 mW
D	725 mW	5.8 mW/°C	464 mW	145 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I		4	5.5	V
Input voltage, V_I at $\overline{EN}$		0	5.5	V
Continuous output current, I_O	TPS2014	0	0.6	A
	TPS2015	0	1	
Operating virtual junction temperature, T_J		0	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
r_{on}	On-state resistance	V_I = 5.5 V,	T_J = 25°C			75	95	mΩ
		V_I = 5 V,	T_J = 25°C			80	95	
		V_I = 4.5V,	T_J = 25°C			90	110	
		V_I = 4 V,	T_J = 25°C			96	110	
I_{lkg}	Leakage current, output	$\overline{EN}$ = V_I,	T_J = 25°C			0.001	1	µA
		$\overline{EN}$ = V_I,	0°C ≤ T_J ≤ 125°C				10	
t_r	Rise time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		4		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.8		
t_f	Fall time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		3.9		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage	4 V ≤ V_I ≤ 5.5 V	2		V
V_{IL}	Low-level input voltage	4 V ≤ V_I ≤ 5.5 V		0.8	V
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = V_I	–0.5	0.5	μA
t_{PLH}	Propagation (delay) time, low to high output	C_L = 1 μF		20	ms
t_{PHL}	Propagation (delay) time, high to low output	C_L = 1 μF		40	ms

current limit

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V	TPS2014	0.66	1.2	1.8	A
			TPS2015	1.1	2	3	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDL}	Supply current, low-level output	$\overline{EN}$ = V_I	T_J = 25°C		0.015	10	μA
			0°C ≤ T_J ≤ 125°C			10	μA
I_{DDH}	Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73	100	μA
			0°C ≤ T_J ≤ 125°C			100	μA

undervoltage lockout

PARAMETER		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	2	3.2	4	V

$\overline{OC}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS}	Short-circuit output current	0°C ≤ T_J ≤ 125°C			5	mA
V_{OL}	Low-level output voltage	0°C ≤ T_J ≤ 125°C			0.3	mA

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†			TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
r_{on}	On-state resistance	V_I = 5.5 V,	T_J = 25°C			75		mΩ
		V_I = 5 V,	T_J = 25°C			80		
		V_I = 4.5V,	T_J = 25°C			90		
		V_I = 4 V,	T_J = 25°C			96		
I_{lkg}	Leakage current, output	$\overline{EN}$ = V_I,	T_J = 25°C			0.001		µA
		$\overline{EN}$ = V_I,	0°C ≤ T_J ≤ 125°C			10		
t_r	Rise time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		4		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.8		
t_f	Fall time, output	V_I = 5.5 V,	T_J = 25°C	C_L = 1 µF		3.9		ms
		V_I = 4 V,	T_J = 25°C	C_L = 1 µF		3.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input ($\overline{EN}$)

PARAMETER		TEST CONDITIONS	TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
V_{IH}	High-level input voltage	4 V ≤ V_I ≤ 5.5 V		2		V
V_{IL}	Low-level input voltage	4 V ≤ V_I ≤ 5.5 V		0.8		V
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = V_I		0.5		µA
t_{PLH}	Propagation (delay) time, low to high output	C_L = 1 µF		20		ms
t_{PHL}	Propagation (delay) time, high to low output	C_L = 1 µF		40		

current limit

PARAMETER		TEST CONDITIONS†		TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
I_{OS}	Short-circuit output current	T_J = 25°C, V_I = 5.5 V	TPS2014		1.2		A
			TPS2015		2		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

supply current

PARAMETER		TEST CONDITIONS		TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
I_{DDL}	Supply current, low-level output	$\overline{EN}$ = V_I	T_J = 25°C		0.015		µA
			0°C ≤ T_J ≤ 125°C		10		
I_{DDH}	Supply current, high-level output	$\overline{EN}$ = 0 V	T_J = 25°C		73		µA
			0°C ≤ T_J ≤ 125°C		100		

undervoltage lockout

PARAMETER		TPS2014Y, TPS2015Y MIN	TPS2014Y, TPS2015Y TYP	TPS2014Y, TPS2015Y MAX	UNIT
V_{IL}	Low-level input voltage		3.2		V

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted) (continued)

$\overline{OC}$

PARAMETER		TEST CONDITIONS	TPS2014Y, TPS2015Y			UNIT
			MIN	TYP	MAX	
I_{OS}	Short-circuit output current	0°C ≤ T_J ≤ 125°C		5		mA
V_{OL}	Low-level output voltage	0°C ≤ T_J ≤ 125°C		0.3		

PARAMETER MEASUREMENT INFORMATION

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TPS2015 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V	8

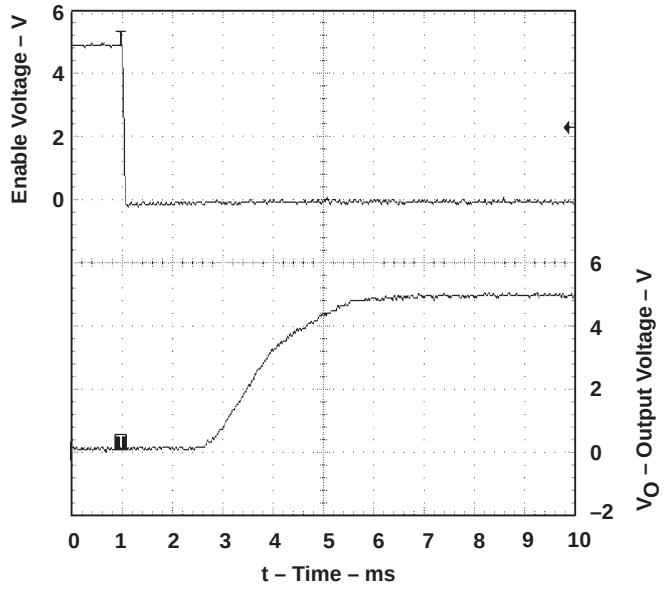

Figure 1. Propagation Delay and Rise Time With 1-μF Load, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

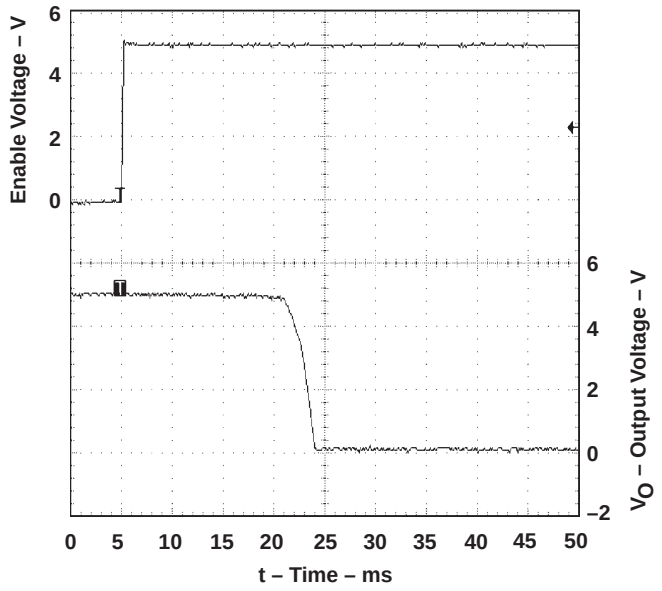

Figure 2. Propagation Delay and Fall Time With 1-μF Load, $V_{I(IN)}$ = 5 V

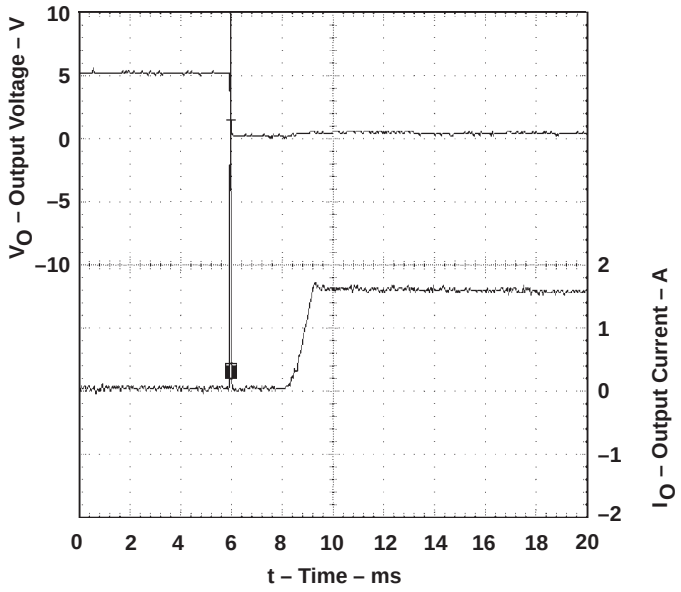

Figure 3. TPS2014 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

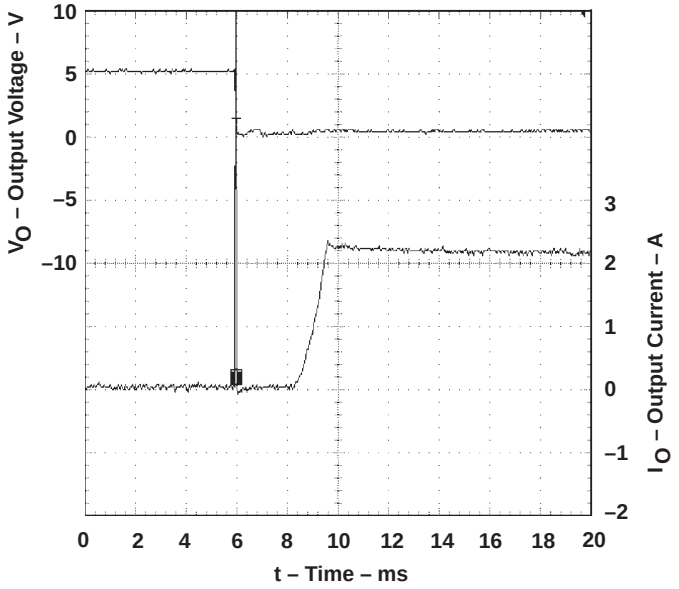

Figure 4. TPS2015 Short-Circuit Current. Short is Applied to Enabled Device, $V_{I(IN)}$ = 5 V

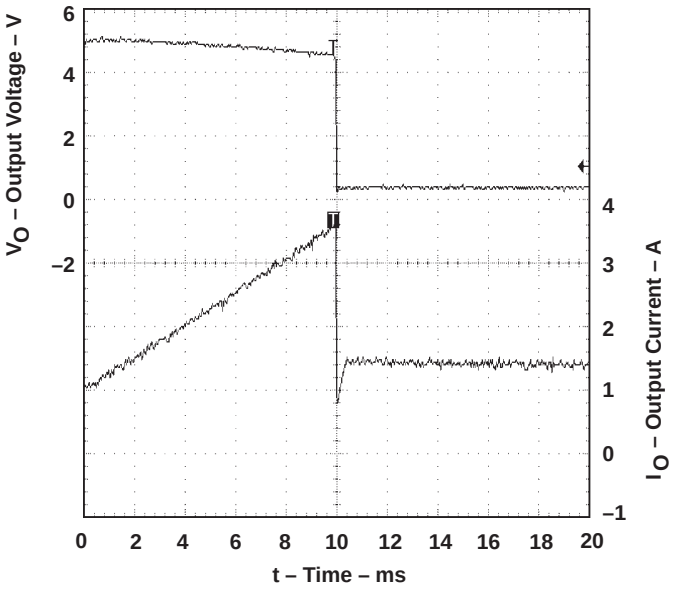

Figure 5. TPS2014 Threshold Current, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

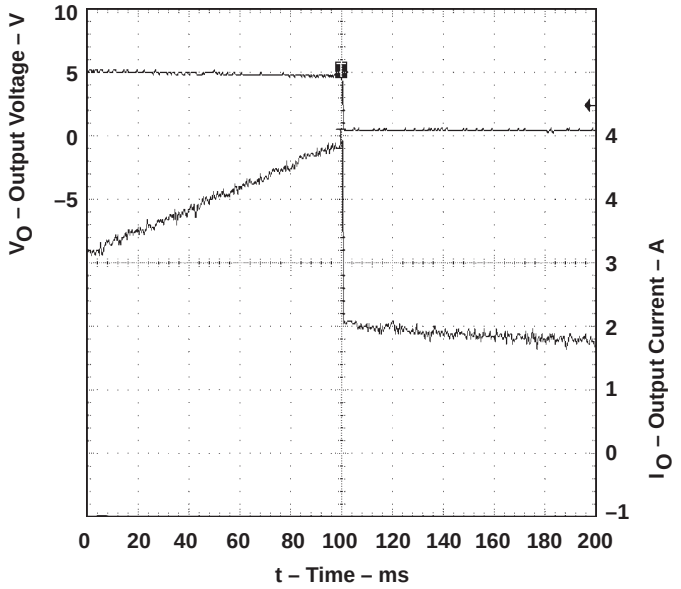

Figure 6. TPS2015 Threshold Current, $V_{I(IN)}$ = 5 V

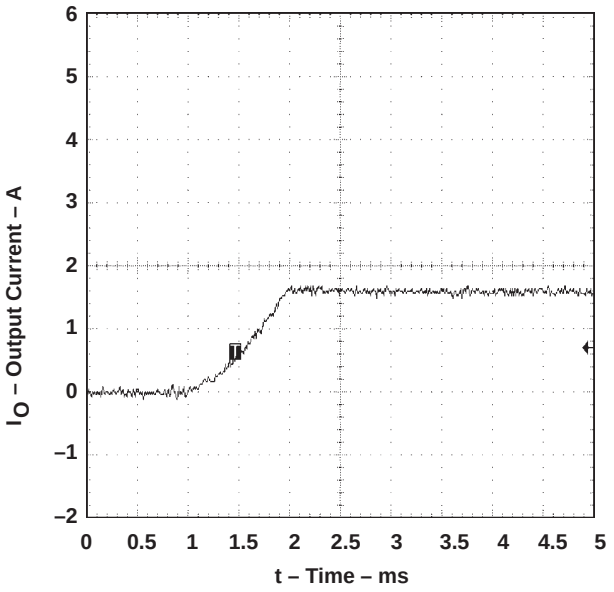

Figure 7. TPS2014 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V

PARAMETER MEASUREMENT INFORMATION

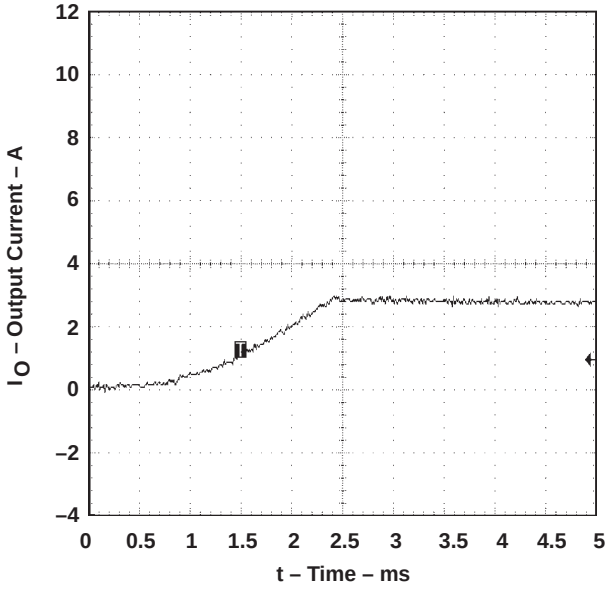

Figure 8. TPS2015 (Enabled) into Short Circuit, $V_{I(IN)}$ = 5 V

TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

TURN-ON DELAY TIME vs INPUT VOLTAGE

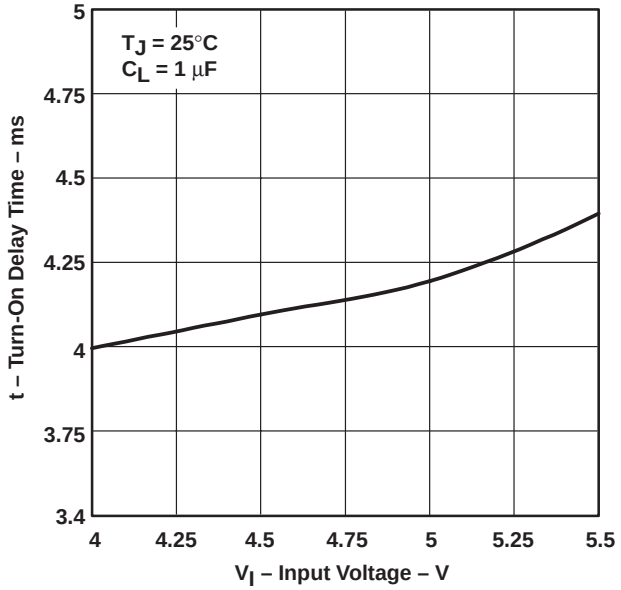


Figure 9

TURN-OFF DELAY TIME vs INPUT VOLTAGE

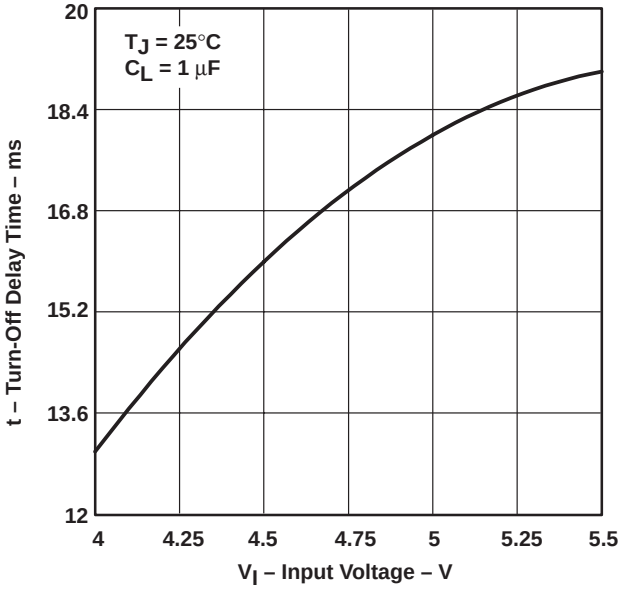


Figure 10

RISE TIME vs OUTPUT CURRENT

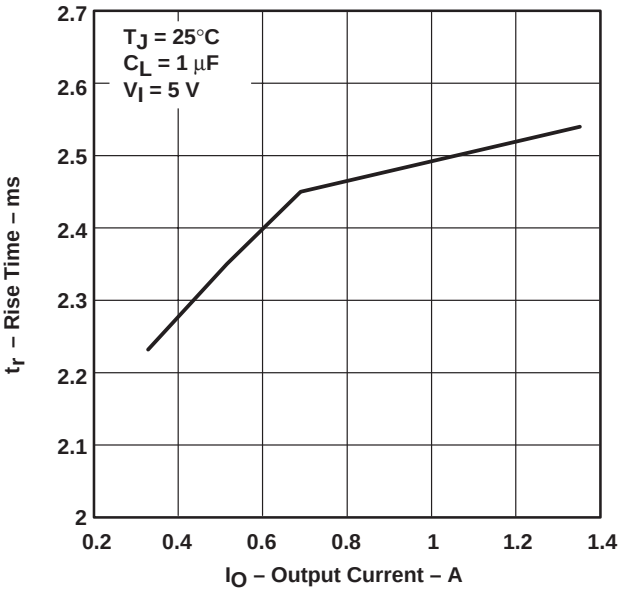


Figure 11

FALL TIME vs OUTPUT CURRENT

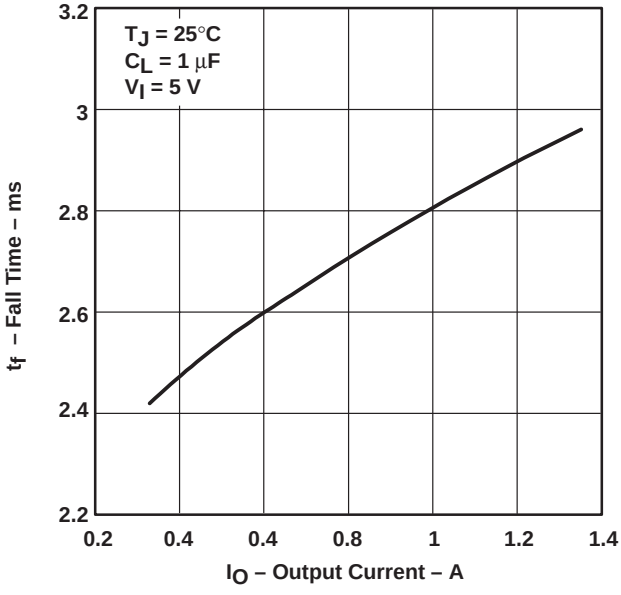


Figure 12

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

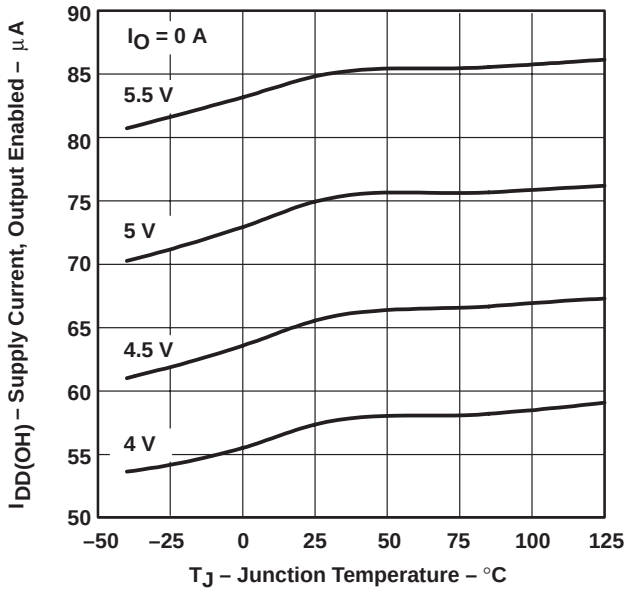


Figure 13

SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

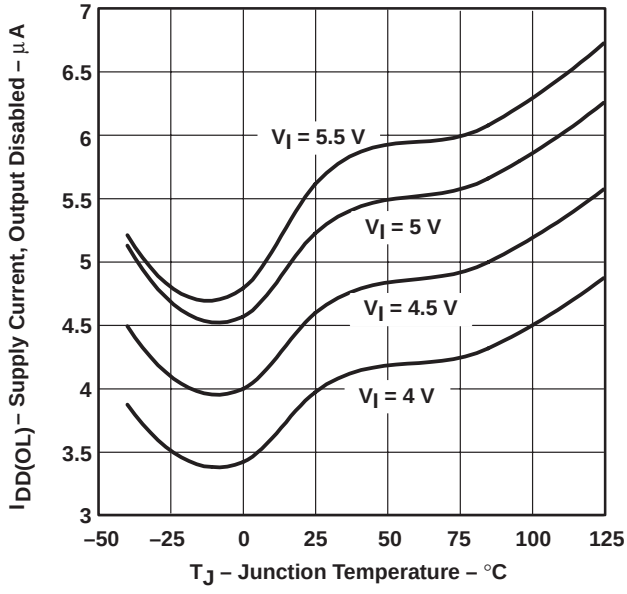


Figure 14

SUPPLY CURRENT, OUTPUT ENABLED vs INPUT VOLTAGE

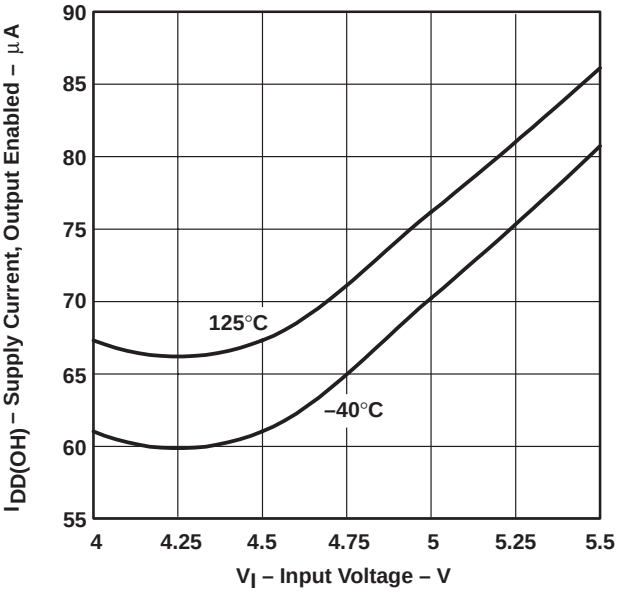


Figure 15

SUPPLY CURRENT, OUTPUT DISABLED vs INPUT VOLTAGE

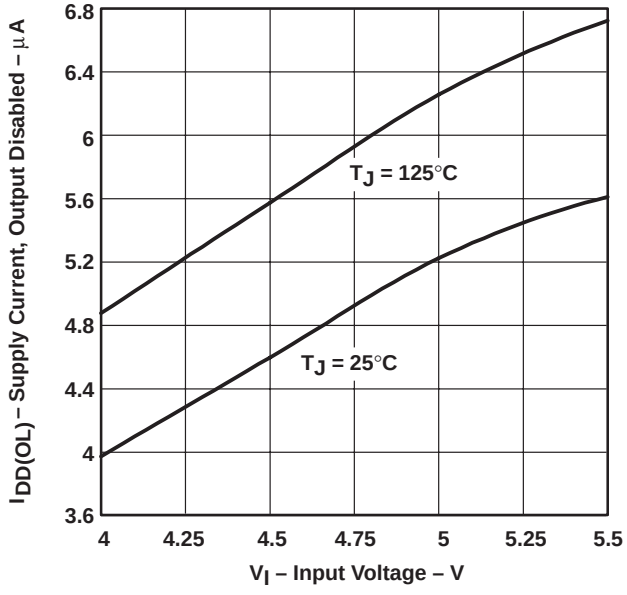


Figure 16

TYPICAL CHARACTERISTICS

ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

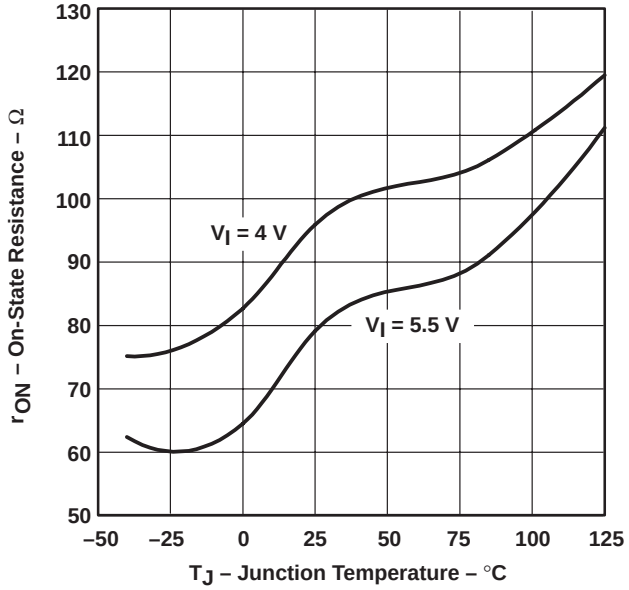


Figure 17

ON-STATE RESISTANCE vs INPUT VOLTAGE

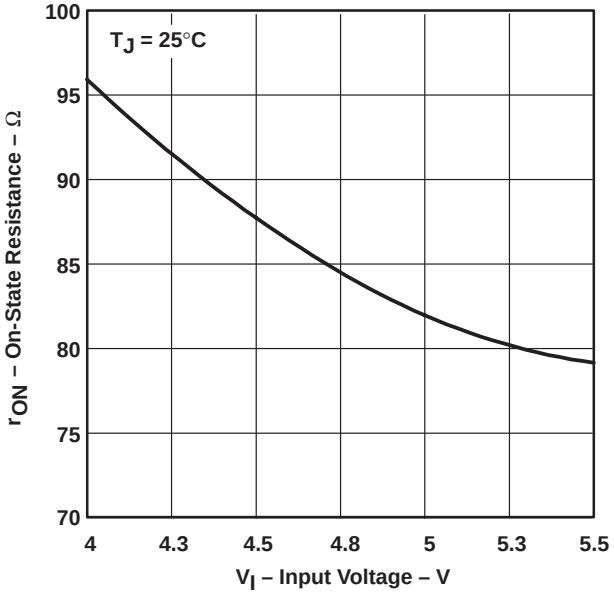


Figure 18

INPUT VOLTAGE TO OUTPUT VOLTAGE vs INPUT VOLTAGE

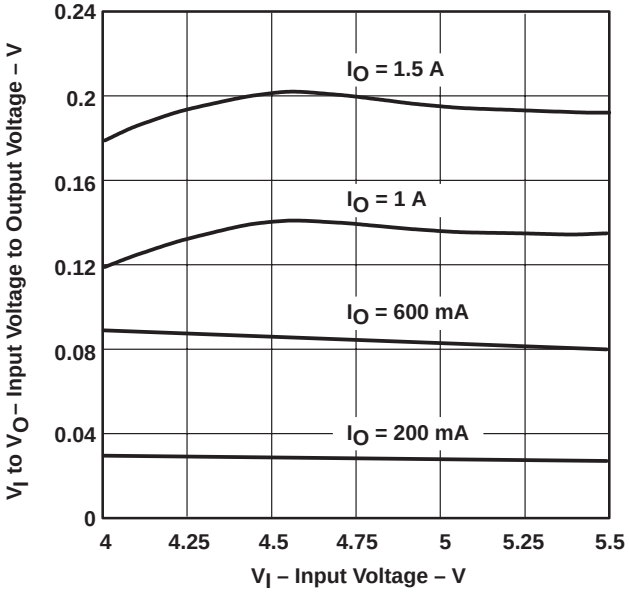


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT vs INPUT VOLTAGE

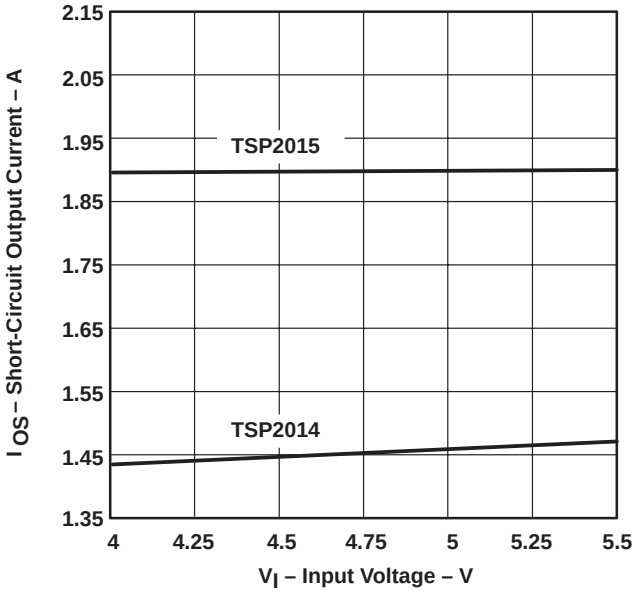


Figure 20

TYPICAL CHARACTERISTICS

**THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE**

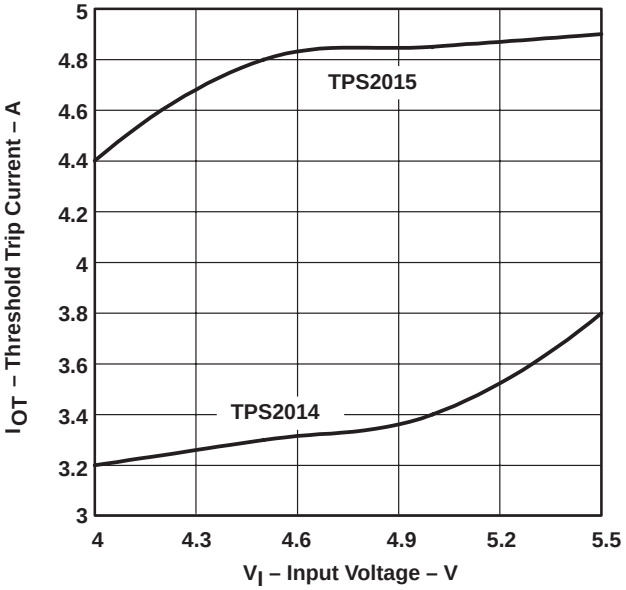


Figure 21

**SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE**

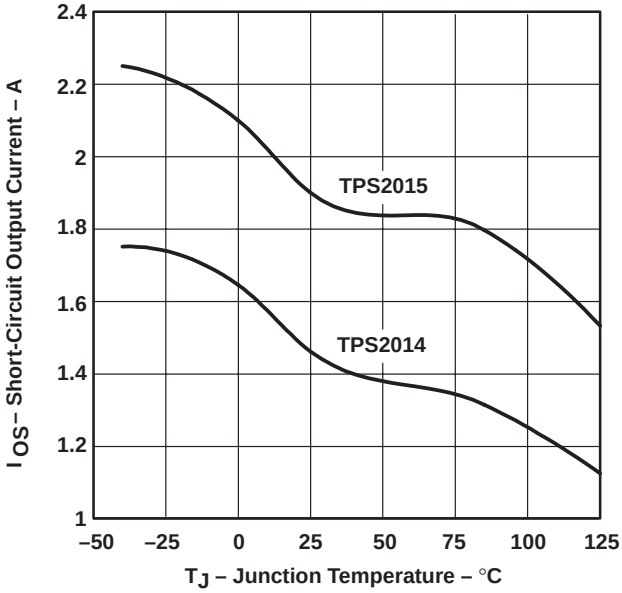


Figure 22

**UVLO TRIP VOLTAGE
vs
JUNCTION TEMPERATURE**

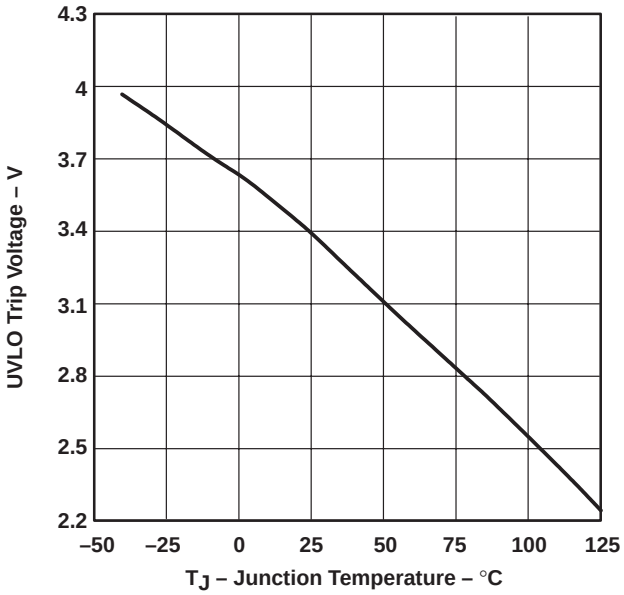


Figure 23

APPLICATION INFORMATION

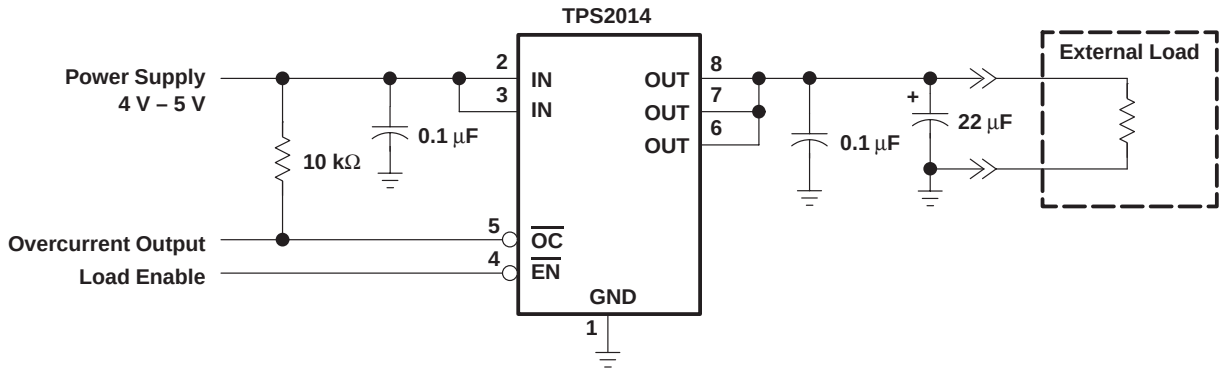


Figure 24. Typical Application

power supply considerations

The TPS20xx has multiple inputs and outputs that must be connected in parallel to minimize voltage drop and prevent unnecessary power dissipation.

A 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. A high-value electrolytic capacitor is also desirable when the output load is heavy or has large paralleled capacitors. Bypassing the output with a 0.1-μF ceramic capacitor improves the immunity of the device to electrostatic discharge (ESD).

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike sense resistors and polyfuses, sense FETs do not increase series resistance to the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Shutdown only occurs when the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figures 7 and 8). The TPS20xx senses the short and immediately switches into a constant-current output.

Under the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents flow for a short time before the current-limit circuit can react (see Figures 3 and 4). After the current-limit circuit has tripped, the device limits normally.

Under the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached (see Figures 5 and 6). The TPS20xx is capable of delivering current up to the current-limit threshold without damage. When the threshold has been reached, the device switches into its constant-current mode.

APPLICATION INFORMATION

power dissipation and junction temperature

The low on-resistance of the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistance of these packages is high compared to that of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find r_{on} at the input voltage and at the operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read r_{on} from Figure 17. Next calculate the power dissipation using:

$$P_D = r_{on} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient temperature

$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W, P = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection is provided to prevent damage to the IC when heavy-overload or a short-circuit fault is present for an extended period of time. The fault forces the TPS20xx into constant current mode, which causes the voltage across the high-side switch to increase. Under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to dangerously high levels. The protection circuit senses the junction temperature of the switch and shuts it off. The switch remains off until the junction temperature has dropped approximately 20°C. The switch continues to cycle in this manner until the load fault or the input power is removed.

undervoltage lockout

An undervoltage lockout is provided to ensure that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 3.2 V, the power switch quickly turns off. This facilitates the design of hot-insertion systems that may not have the ability to turn off the power switch before input power is removed. Upon reapplication of the input voltage (if enabled), the power switch turns on with a controlled rise time to reduce inrush current, EMI, and voltage overshoots.

For proper operation of the UVLO, the TPS20xx requires the voltage decay from 3 V to 2 V to take at least 200 μs. Capacitance is added to the input or output of the TPS20xx to increase this decay rate. Capacitance is generally added to the output to lower inrush current due to input capacitance.

Universal Serial Bus (USB) applications

The USB specification provides for five different classes of devices based on their power sourcing and sinking requirements. These classes of devices are: bus-powered hub, self-powered hub, lower power bus-powered function, high power bus-powered function, and self-powered functions. The TPS20xx can provide power distribution solutions for many of these devices.

APPLICATION INFORMATION

bus-powered and self-power hubs

Hubs provide data and power for downstream functions through output ports. Self-power hubs have internal power supplies that furnish power to downstream functions. Each port is required to supply 500 mA continuous to a downstream function. Each port must have overcurrent protection to meet the requlatory safety limit that no single port can deliver more than 5 A. The self-power hub must also have a method to detect and report an overcurrent condition to the USB host. The TPS20xx provides the required current-limiting function and has an overcurrent logic output to inform the hub controller of the fault condition. The on-state resistance of the TPS20xx is low enough to meet all USB voltage regulation requirements. The switch also provides the capability to remove power from a faulted port.

Bus-powered hubs distribute power and data from an input port to downstream ports. Each output port is required to supply 100 mA continuous. A bus-powered hub is not required to provide overcurrent protection because it is provided by the upstream port. In order to power up in a low power state, the self-powered hub must be able to switch power to its output ports. The TPS20xx can also provide this function.

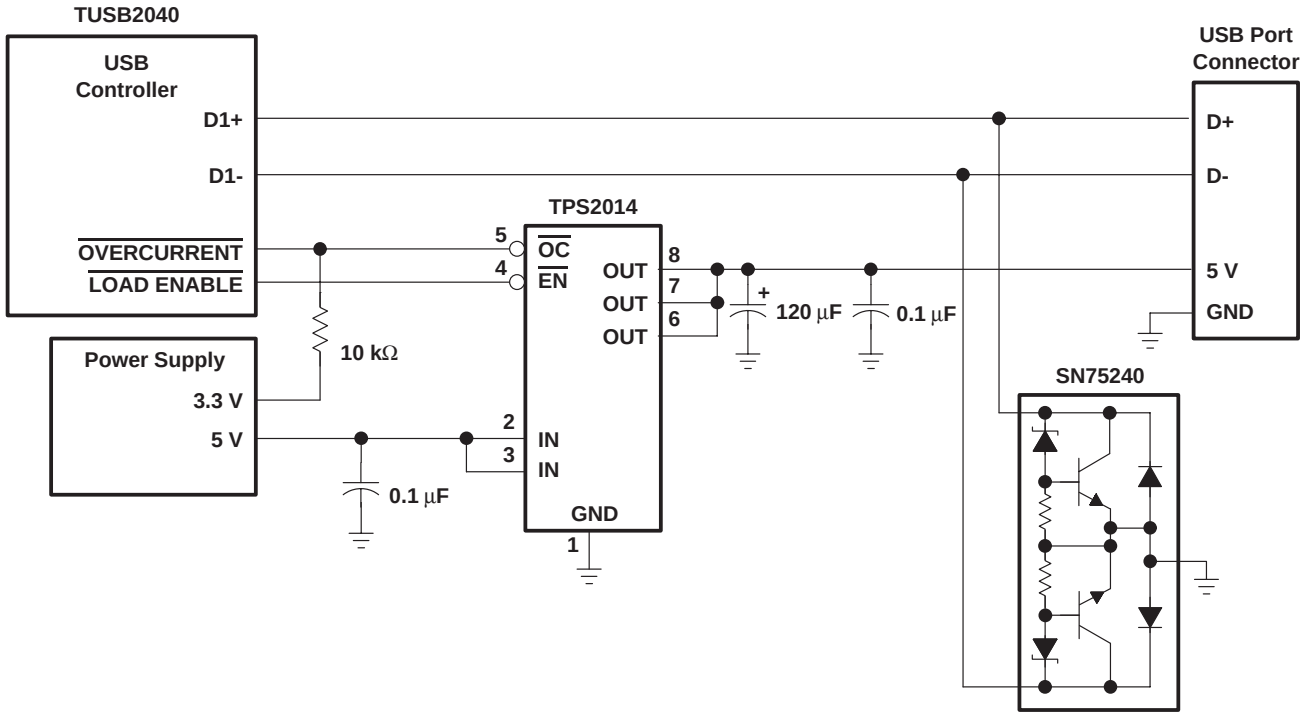


Figure 25. Typical USB Self-Powered Hub Application

low power bus-powered functions and high power bus-powered functions

Low-power and high-power bus-powered functions are powered by their input ports. If the load of the function is more than the parallel combination of 44 Ω and 10 μF, it must implement inrush current limiting. The TPS20xx provides this function with its controlled rise time during turn on.

APPLICATION INFORMATION

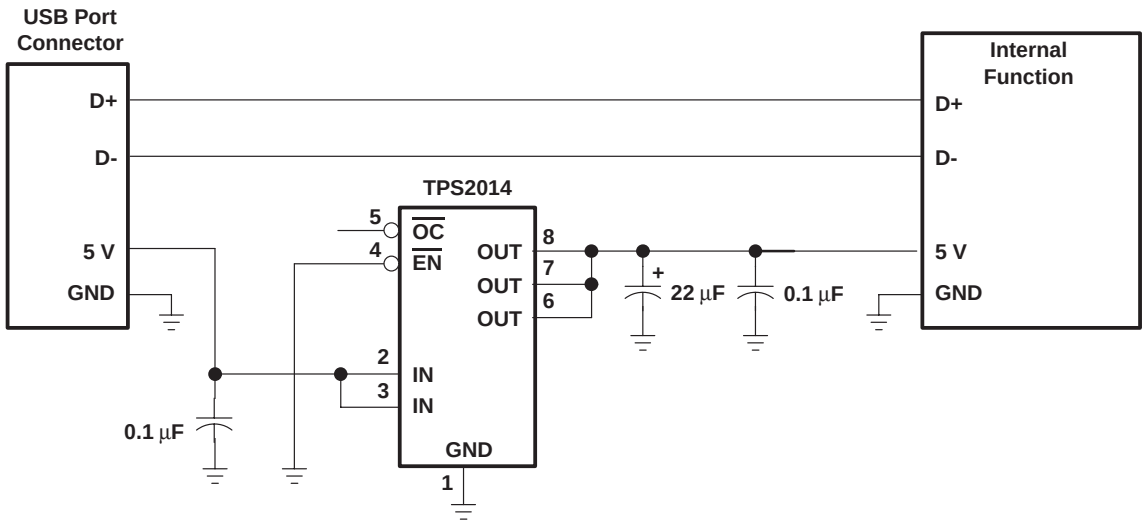


Figure 26. Typical USB Bus-Powered Function Application

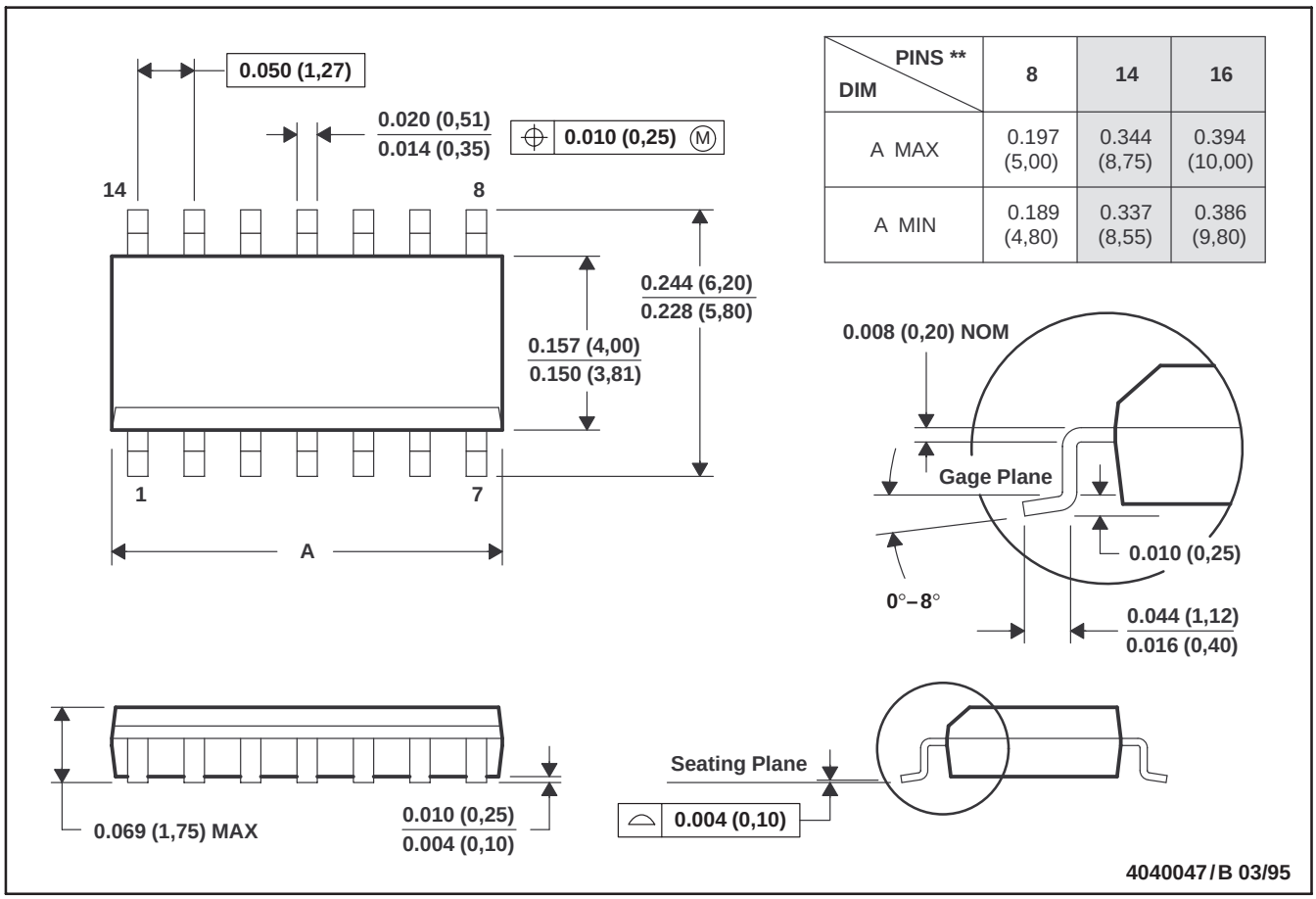
ESD protection

All TPS20xx terminals incorporate ESD-protection circuitry designed to withstand a 6-kV human-body-model discharge as defined in MIL-STD-883C. Additionally, the output is protected from discharges up to 12 kV.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

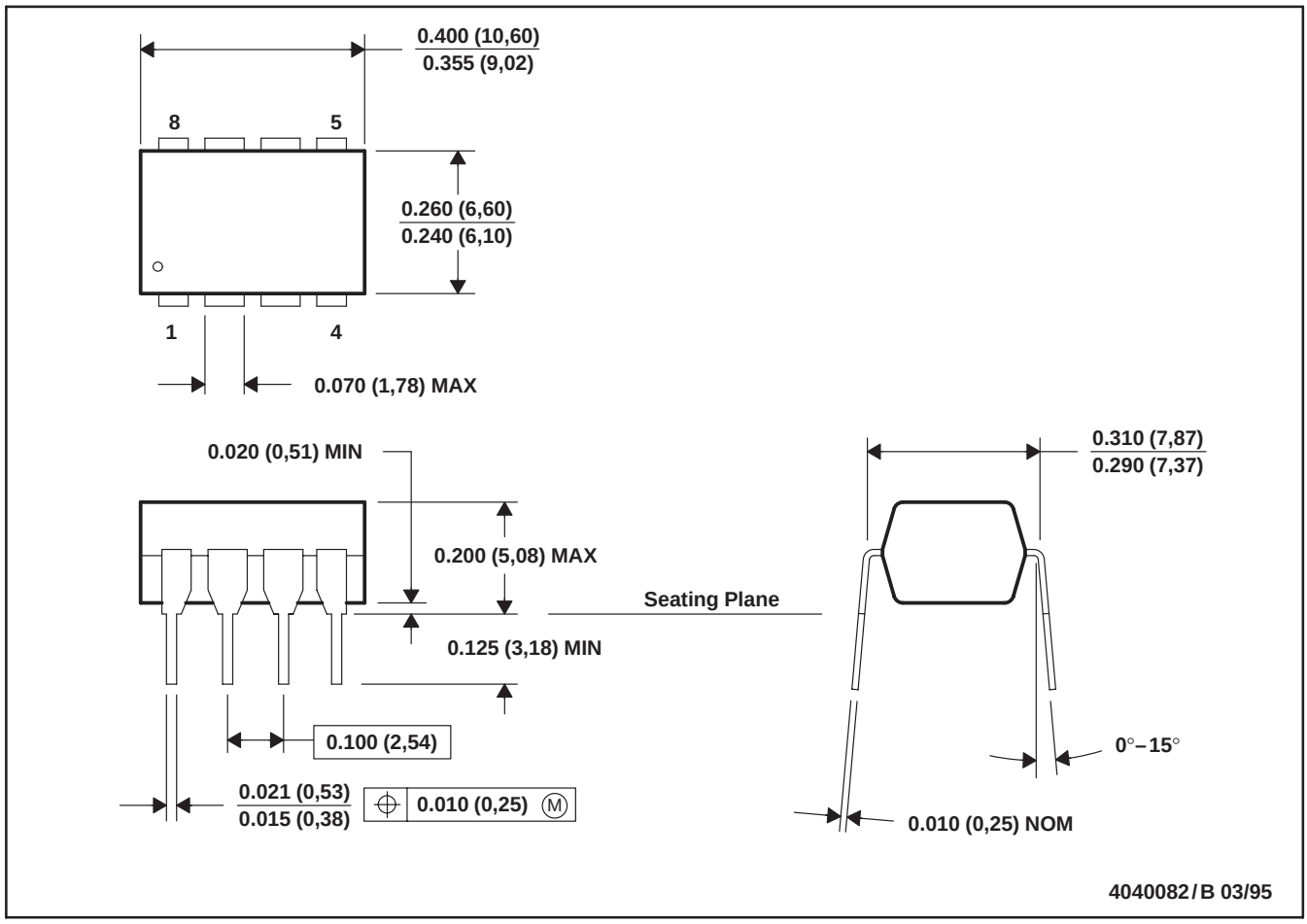


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

MECHANICAL DATA

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

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