features

- Power-On Reset Generator with Fixed Delay Time of 200 ms, no External Capacitor Needed
- Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, and 5 V
- Pin-For-Pin Compatible with the MAX705 through MAX708 Series
- Integrated Watchdog Timer (TPS3705 only)
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Maximum Supply Current of 50 μA
- MSOP-8 and SO-8 Packages
- Temperature Range . . . –40°C to 85°C

typical applications

- Designs Using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

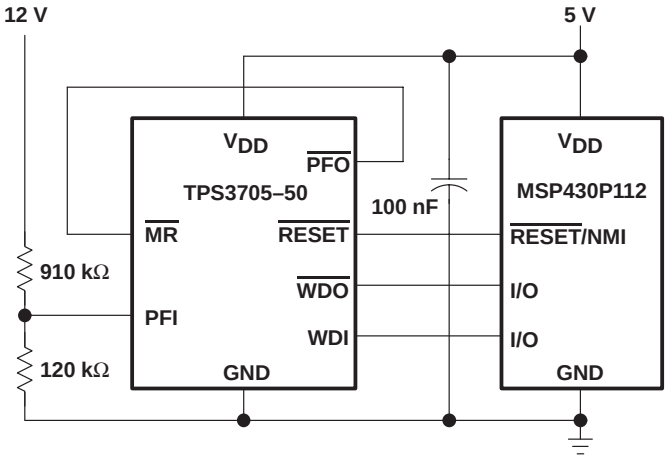
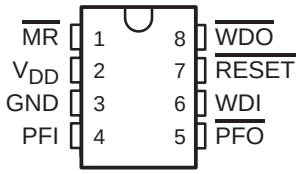
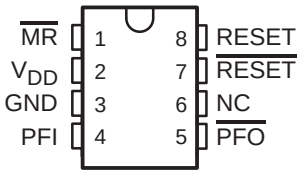


Figure 1. Typical MSP430 Application

TPS3705 . . . D PACKAGE
(TOP VIEW)

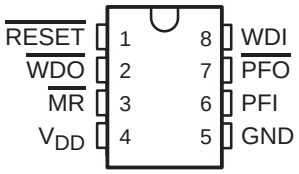


TPS3707 . . . D PACKAGE
(TOP VIEW)

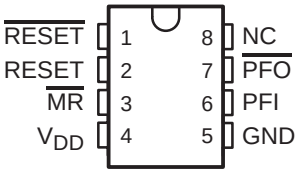


NC – No internal connection

TPS3705 . . . DGN PACKAGE
(TOP VIEW)



TPS3707 . . . DGN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS3705, TPS3707 family of microprocessor supply-voltage supervisors provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT+}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\,typ}$ = 200 ms, starts after V_{DD} has risen above the threshold voltage V_{IT+}. When the supply voltage drops below the threshold voltage V_{IT-}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage V_{IT-} set by an internal voltage divider.

The TPS3705-xx and TPS3707-xx devices incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active.

The TPS370x-xx families integrate a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3705-xx devices have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$ = 1.6 s, $\overline{\text{WDO}}$ becomes active. This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3707-xx devices do not have the Watchdog function, but include a high-level output RESET.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in either 8-pin MSOP or standard SOIC packages. The TPS3705, TPS3707 devices are characterized for operation over a temperature range of –40°C to 85°C.

AVAILABLE OPTIONS

T_A	THRESHOLD VOLTAGE	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
		SMALL OUTLINE (D)	POWER–PAD™ μ-SMALL OUTLINE (DGN)		
–40°C to 85°C	2.63 V	TPS3705–30D	TPS3705–30DGN	TIAAT	TPS3705-30Y
	2.93 V	TPS3705–33D	TPS3705–33DGN	TIAAU	TPS3705–33Y
	4.55 V	TPS3705–50D	TPS3705–50DGN	TIAAV	TPS3705–50Y
	2.25 V	TPS3707–25D	TPS3707–25DGN	TIAAW	TPS3707–25Y
	2.63 V	TPS3707–30D	TPS3707–30DGN	TIAAX	TPS3707–30Y
	2.93 V	TPS3707–33D	TPS3707–33DGN	TIAAY	TPS3707–33Y
	4.55 V	TPS3707–50D	TPS3707–50DGN	TIAAZ	TPS3707–50Y

Function Tables

TRUTH TABLE, TPS3705

$\overline{MR}$	$V_{DD}>V_{IT}$	$\overline{RESET}$	TYPICAL DELAY
H→L	1	H→L	30 ns
L→H	1	L→H	200 ms
H	1→0	H→L	3 µs
H	0→1	L→H	200 ms

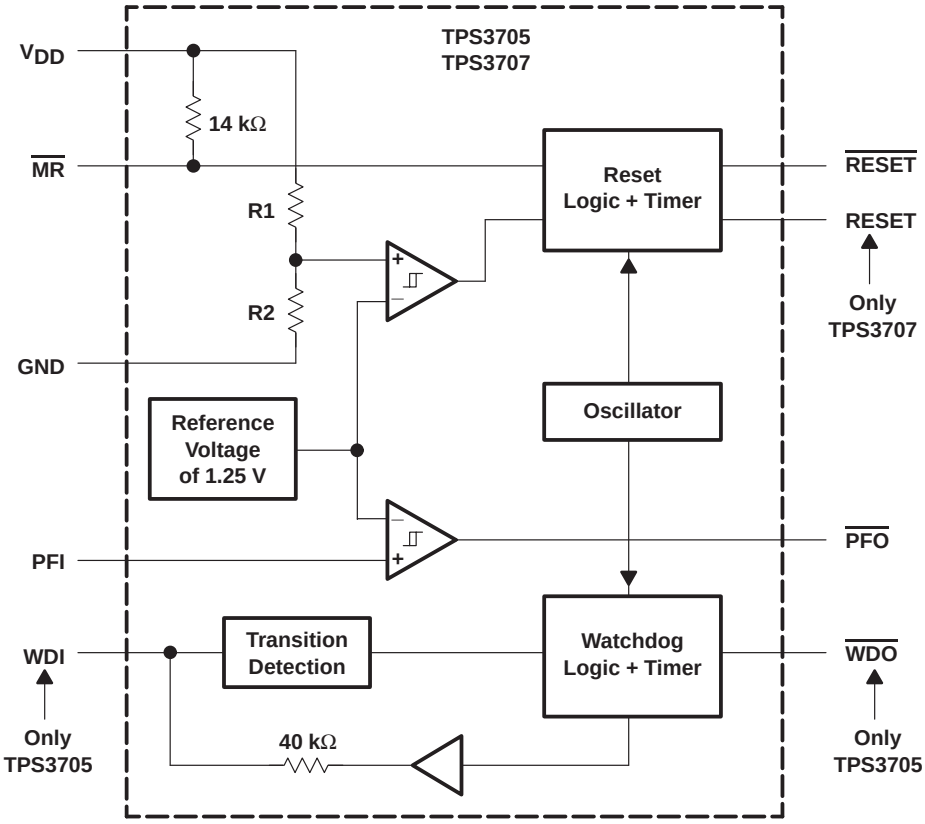
TRUTH TABLE, TPS3707

$\overline{MR}$	$V_{DD}>V_{IT}$	$\overline{RESET}$	RESET	TYPICAL DELAY
H→L	1	H→L	L→H	30 ns
L→H	1	L→H	H→L	200 ms
H	1→0	H→L	L→H	3 µs
H	0→1	L→H	H→L	200 ms

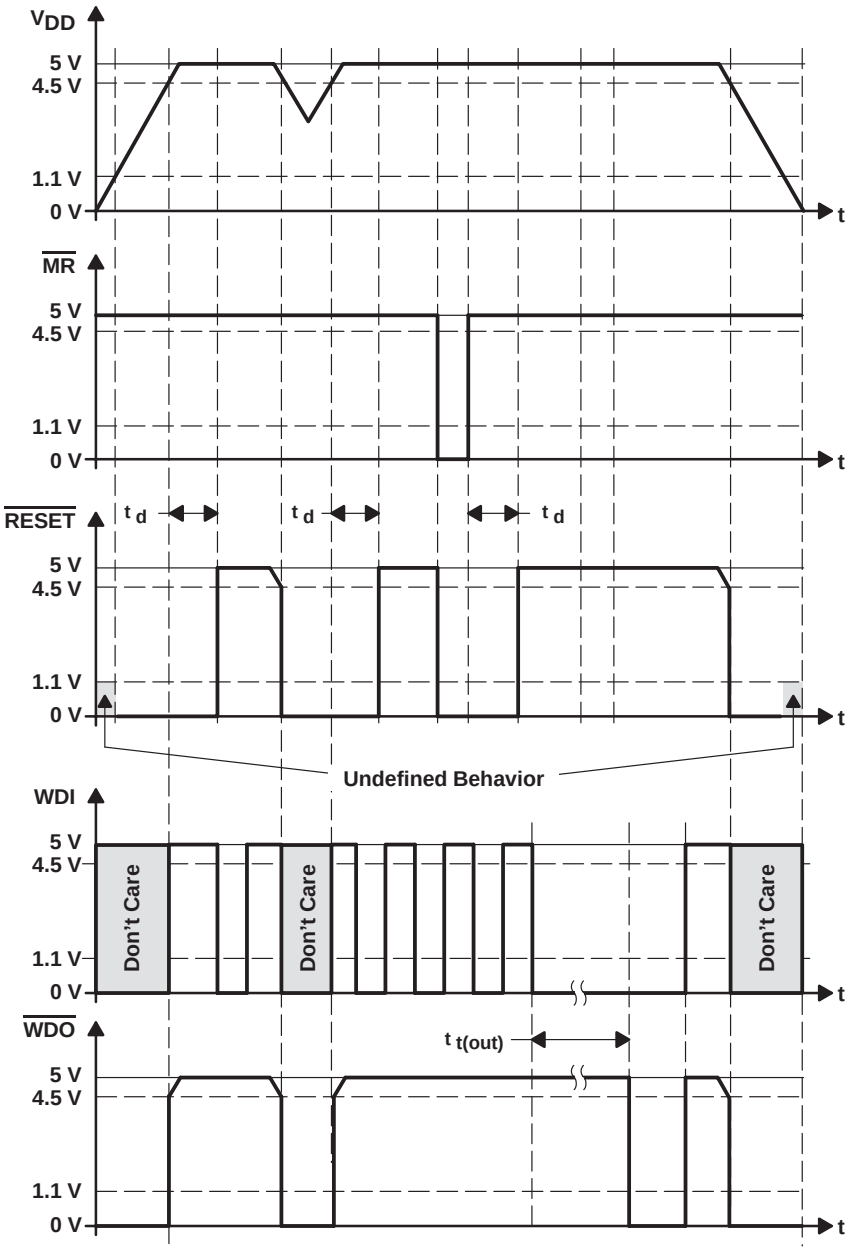
TRUTH TABLE, TPS370x

$PFI>V_{IT}$	$\overline{PFO}$	TYPICAL DELAY
0→1	L→H	0.5 µs
1→0	H→L	0.5 µs

functional block diagram



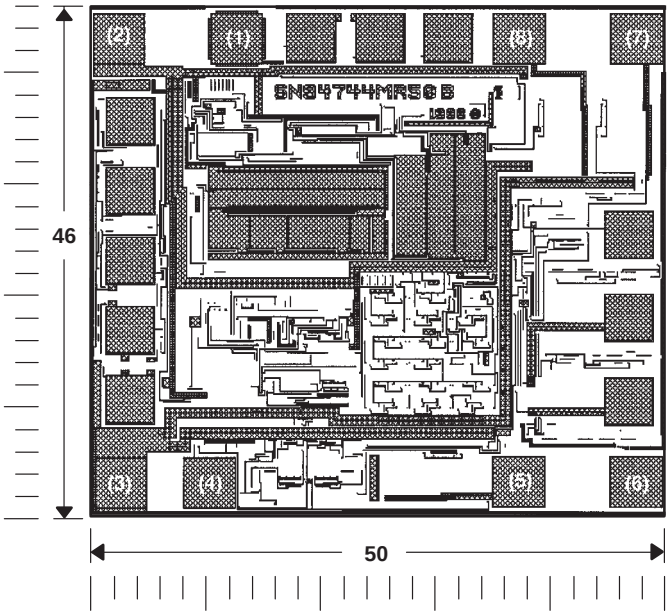
timing diagrams

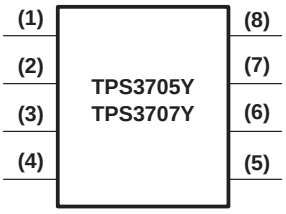


TPS370xY chip information

These chips, when properly assembled, display characteristics similar to those of the TPS370x. Thermal compression or ultrasonic bonding may be caused on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

Terminal Functions

TERMINAL NAME		NO.	I/O	DESCRIPTION
$\overline{MR}$		1	I	Manual reset
VDD		2		Supply voltage
GND		3		Ground
PFI		4	I	Power-fail comparator input
$\overline{PFO}$		5	O	Power-fail comparator output
WDI	TPS3705	6	I	Watchdog timer input
NC	TPS3707			No internal connection
$\overline{RESET}$		7	O	Active-low reset output
$\overline{WDO}$	TPS3705	8	O	Watchdog timer output
RESET	TPS3707		O	Active-high reset output

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) . . . . . 7 V
All other pins (see Note 1) . . . . . –0.3 V to 7 V
Maximum low output current, I_{OL} . . . . . 5 mA
Maximum high output current, I_{OH} . . . . . –5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . ±20 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than t = 1000h continuously.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W
D	725 mW	5.8 mW/°C	464 mW	377 mW

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage, V_I	0	V_{DD}+0.3	V
High-level input voltage, V_{IH}	0.7×V_{DD}		V
Low-level input voltage, V_{IL}		0.3×V_{DD}	V
Input transition rise and fall rate at $\overline{MR}$ or WDI, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		TPS370x-xx	V_{DD} = 1.1 V, I_{OH} = –4 µA	0.8			V
			TPS3707-25	$V_{DD} = V_{IT+} + 0.2$ V, I_{OH} = –500 µA	$0.7\times V_{DD}$			
			TPS370x-30					
			TPS370x-33					
			TPS370x-50	$V_{DD} = V_{IT+} + 0.2$ V, I_{OH} = –800 µA	V_{DD} –1.5 V			
			TPS370x-xx	V_{DD} = 6 V, I_{OH} = –800 µA				
V_{OL}	Low-level output voltage		TPS3707-25	$V_{DD} = V_{IT+}$+0.2 V, I_{OL} = 1 mA			0.3	V
			TPS370x-30					
			TPS370x-33					
			TPS370x-50	$V_{DD} = V_{IT+}$+0.2 V, I_{OL} = 2.5 mA			0.4	V
			TPS370x-xx	V_{DD} = 6 V, I_{OL} = 3 mA				
	Power-up reset voltage (see Note 2)			$V_{DD} \geq$ 1.1 V, I_{OL} = 50 µA			0.3	V
$V_{IT–}$	Negative-going input threshold voltage (see Note 3)		TPS3707-25	T_A = 0°C to 85°C	2.20	2.25	2.30	V
			TPS370x-30		2.57	2.63	2.68	
			TPS370x-33		2.87	2.93	2.98	
			TPS370x-50		4.45	4.55	4.63	
			TPS3707-25	T_A = –40°C to 85°C	2.20	2.25	2.32	V
			TPS370x-30		2.57	2.63	2.70	
			TPS370x-33		2.87	2.93	3.0	
			TPS370x-50		4.45	4.55	4.65	
		PFI	TPS370x-xx	$V_{DD} \geq$ 2 V, T_A = –40°C to 85°C	1.20	1.25	1.30	V
V_{hys}	Hysteresis	V_{DD}	TPS3707-25			40		mV
			TPS370x-30			50		
			TPS370x-33			50		
			TPS370x-50			70		
		PFI	TPS370x-xx			10		
$I_{IH(AV)}$	Average high-level input current	WDI		WDI = V_{DD} = 6 V, Time average (dc = 88%)		100	150	µA
$I_{IL(AV)}$	Average low-level input current			WDI = 0 V, V_{DD} = 6 V, Time average (dc = 12%)		–15	–20	µA
I_{IH}	High-level input current	WDI		WDI = V_{DD} = 6 V		120	170	µA
		$\overline{MR}$		$\overline{MR}$ = $0.7\times V_{DD}$, V_{DD} = 6 V		–130	–180	
I_{IL}	Low-level input current	WDI		WDI = 0 V, V_{DD} = 6 V		–120	–170	µA
		$\overline{MR}$		$\overline{MR}$ = 0 V, V_{DD} = 6 V		–430	–600	
I_I	Input current	PFI		V_{DD} = 6 V, 0 V ≤ $V_I \leq V_{DD}$	–1	0	1	µA
I_{DD}	Supply current		TPS3707-xx	V_{DD} = 2 V to 6 V, $\overline{MR}$ = V_{DD}, $\overline{MR}$, WDI and outputs unconnected		20	50	µA
			TPS3705-xx	V_{DD} = 2 V to 6 V, $\overline{MR}$= V_{DD}, $\overline{MR}$, WDI and outputs unconnected		30	50	µA
C_i	Input capacitance			V_I = 0 V to V_{DD}		5		pF

NOTES: 2. The lowest supply voltage at which $\overline{RESET}$ becomes active. $t_{r,VDD} \geq 15$ µs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	$V_{DD} = V_{IT+} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V	6			µs
		at $\overline{MR}$	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns
		at WDI	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100			ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time out		$V_{DD} \geq V_{IT+} + 0.2$ V, See timing diagram	1.1	1.6	2.3	s
t_d	Delay time		$V_{DD} > V_{IT+} + 0.2$ V, See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{MR}$ to $\overline{RESET}$ delay	$V_{DD} \geq V_{IT+} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$ $V_{IH} = 0.7 \times V_{DD}$		50	250	ns
t_{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{MR}$ to RESET delay (TPS3707–xx only)			50	250	
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay			3	5	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to RESET delay (TPS3707-xx only)			3	5	
t_{PHL}	Propagation (delay) time, high-to-low-level output	PFI to $\overline{PFO}$ delay	V_{DD} = 2 V to 6 V		0.5	1	µs
t_{PLH}	Propagation (delay) time, low-to-high-level output				0.5	1	

TYPICAL CHARACTERISTICS

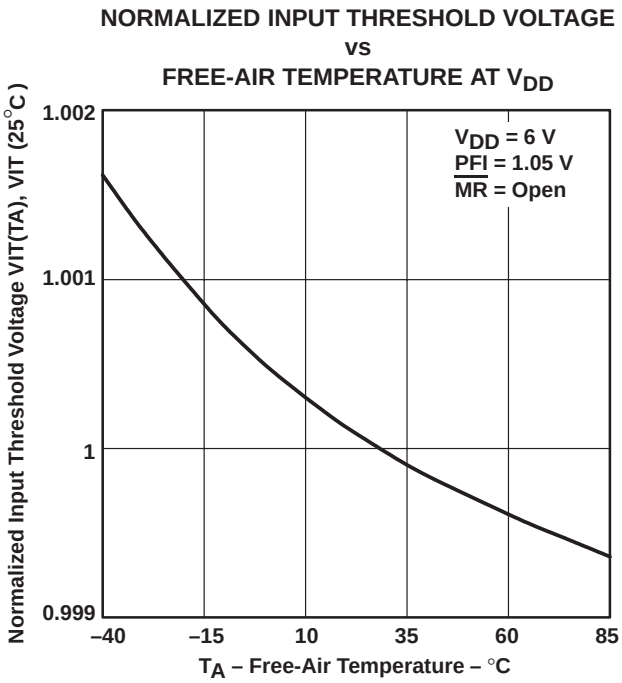


Figure 2

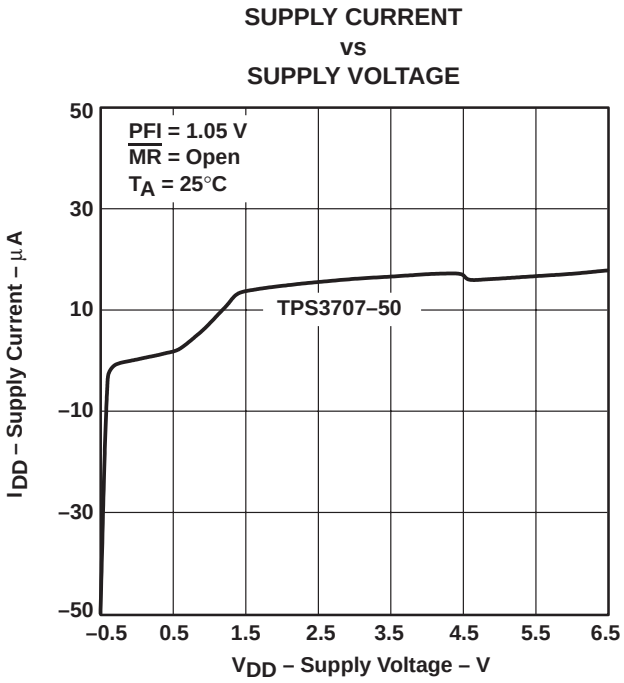


Figure 3

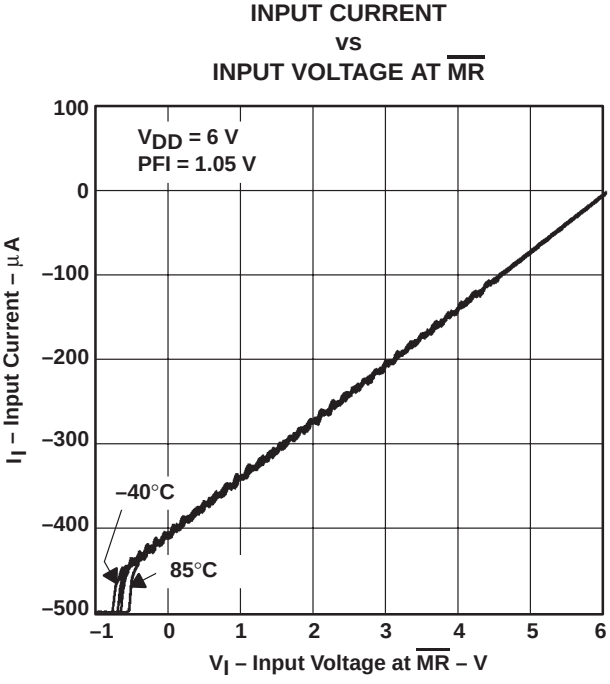


Figure 4

TYPICAL CHARACTERISTICS

MINIMUM PULSE DURATION AT V_{DD} vs V_{DD} THRESHOLD OVERDRIVE

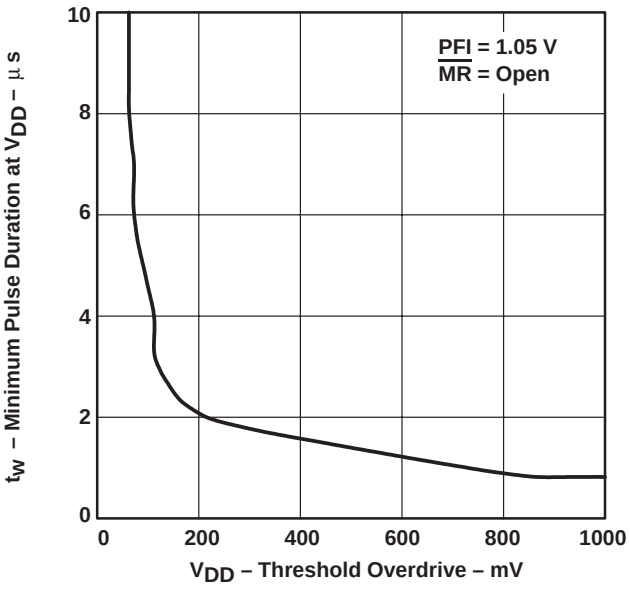


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

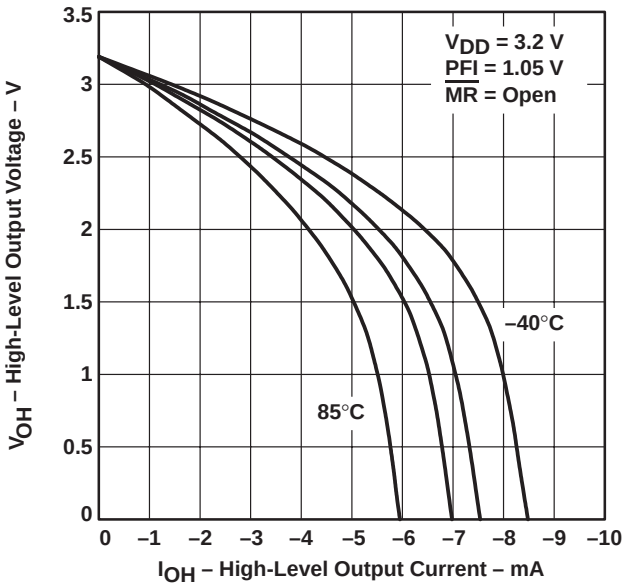


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

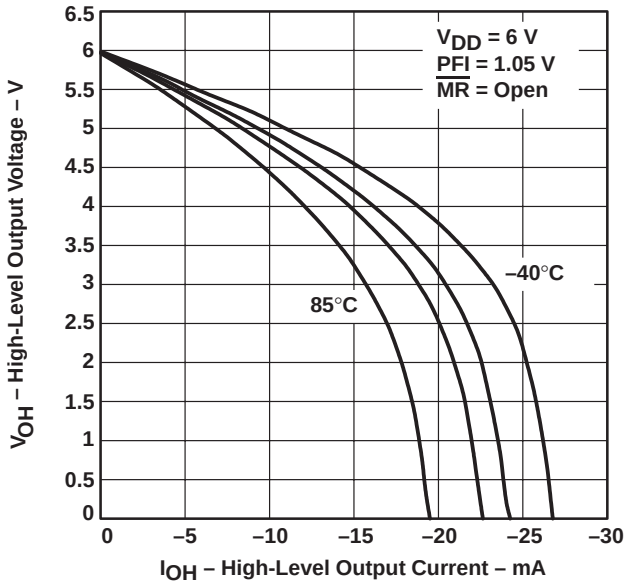


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

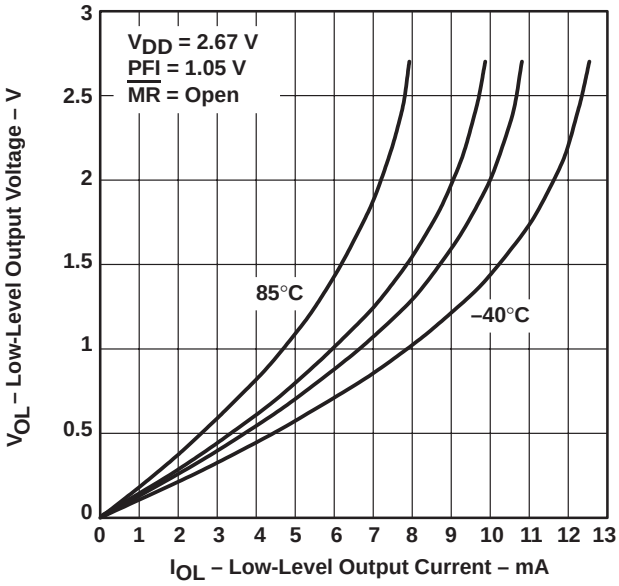
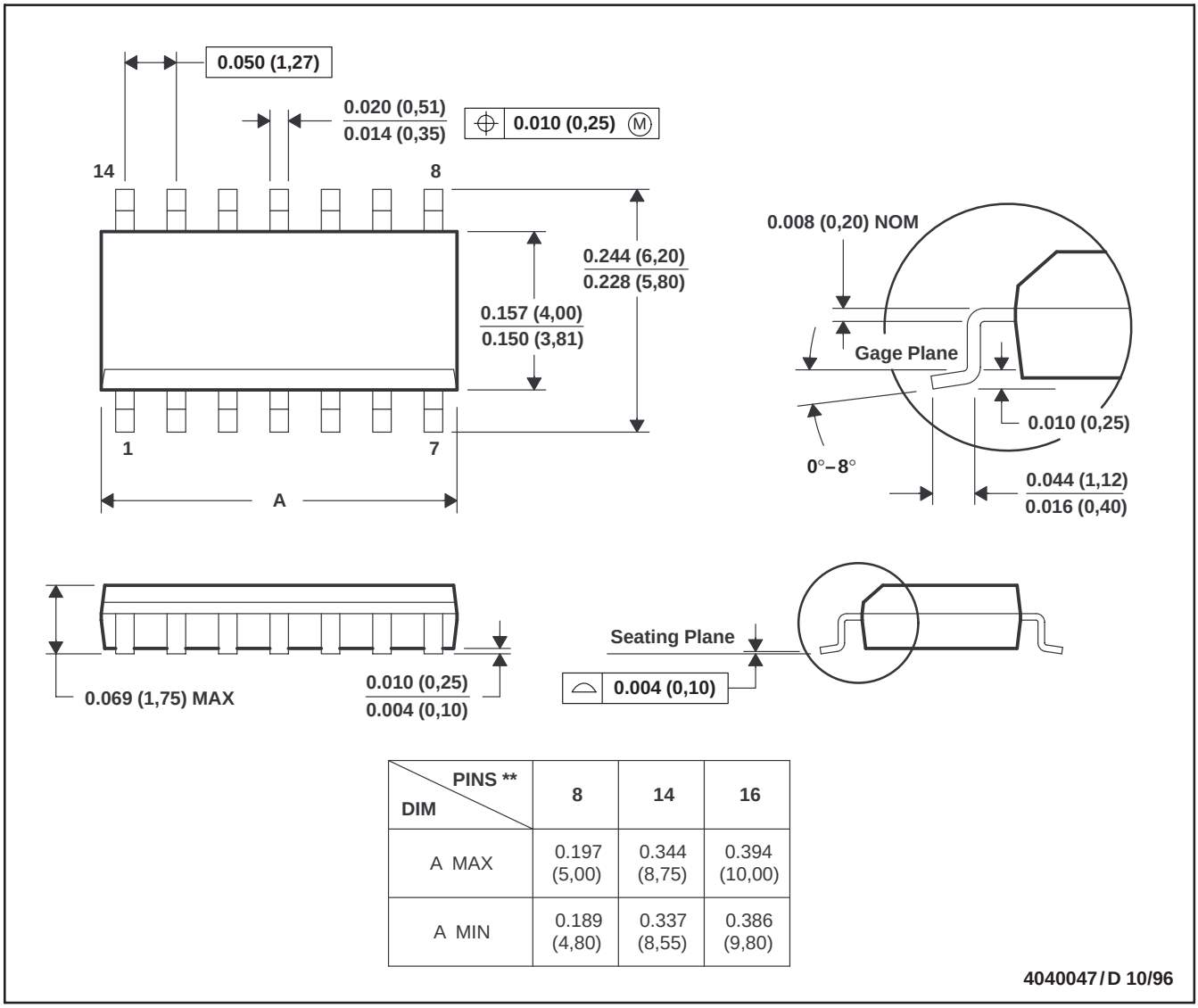


Figure 8

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



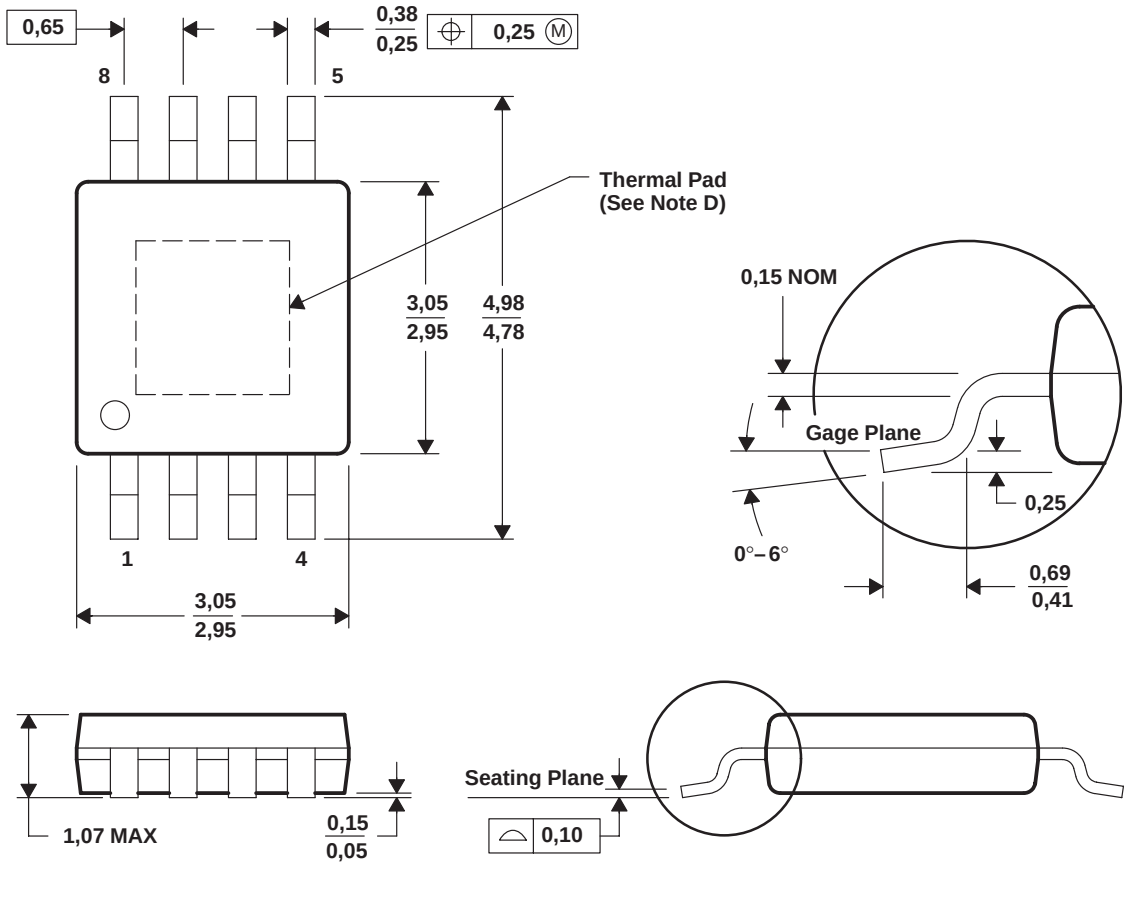
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL DATA

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments Incorporated.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.