Capacitance-Free NMOS 400-mA Low-Dropout Regulator

Check for Samples: TPS736xx-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **Stable with No Output Capacitor—Any Value or Type of Capacitor**
- **Input Voltage Range of 1.7 to 5.5 V**
- **Ultra-Low Dropout Voltage: 75 mV typ**
- **Excellent Load-Transient Response—With or Without Optional Output Capacitor**
- **New NMOS Topology Delivers Low Reverse-Leakage Current**
- **Low Noise: 30 μV_{RMS} typ (10 Hz to 100 kHz)**
- **0.5% Initial Accuracy**
- **1% Overall Accuracy Over Line, Load, and Temperature**
- **Less Than 1 µA max I_Q in Shutdown Mode**
- **Thermal Shutdown and Specified Min and Max Current Limit Protection**
- **Available in Multiple Output Voltage Versions**
  - **Fixed Outputs of 1.2 to 5 V**
  - **Custom Outputs Available**

APPLICATIONS

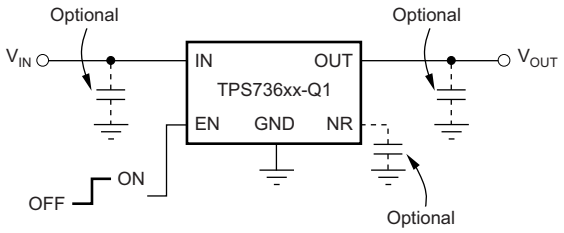
- **Post-Regulation for Switching Supplies**
- **Noise-Sensitive Circuitry such as VCOs**

DESCRIPTION

The TPS736xx-Q1 family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. The topology also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

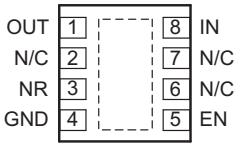
The TPS736xx-Q1 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1 µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

For all other packages, please contact TI Sales.

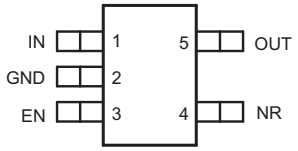


Typical Application Circuit for Fixed-Voltage Versions

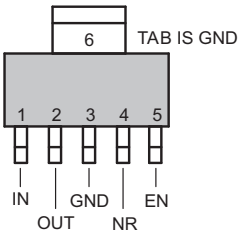
DRB PACKAGE
3mmx 3mm SON
(TOP VIEW)



DBV PACKAGE
SOT23
(TOP VIEW)



DCQ PACKAGE
SOT223
(TOP VIEW)



PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

PARAMETER		TPS736xx-Q1		UNIT
		MIN	MAX	
V_{IN} range		–0.3	6	V
V_{EN} range		–0.3	6	V
V_{OUT} range		–0.3	5.5	V
V_{NR} range		–0.3	6	V
Peak output current		Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation		See *Thermal Information* Table		
Ambient temperature range, T_A		–40	125	°C
Junction temperature range, T_J		–55	150	°C
Storage temperature range		–65	150	°C
Electrostatic discharge	Human body model (HBM)		2	kV
	Charged device model (CDM)		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS736xx-Q1(3)			UNITS
		DRB	DCQ	DBV	
		8 PINS	6 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(4)	47.8	70.4	180	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(5)	83	70	64	
θ_{JB}	Junction-to-board thermal resistance(6)	N/A	N/A	35	
ψ_{JT}	Junction-to-top characterization parameter(7)	2.1	6.8	N/A	
ψ_{JB}	Junction-to-board characterization parameter(8)	17.8	30.1	N/A	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(9)	12.1	6.3	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
  ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
  iii. DBV: There is no exposed pad with the DBV package.
  (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* section of this data sheet.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_A = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)(2)			1.7		5.5	V
V_{REF}	Internal reference		T_A = +25°C	1.198	1.2	1.21	V
V_{OUT}	Accuracy(1)(3)	Nominal	T_A = +25°C	–0.5		+0.5	%
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 400 mA	–1	±0.5	+1	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation		$V_{O(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1 mA ≤ I_{OUT} ≤ 400 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 400 mA		0.0005		
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 400 mA		75	200	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	400	650	800	mA
			3.6 V ≤ V_{IN} ≤ 4.2 V, 0°C ≤ T_A ≤ +70°C	500		800	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current(4) (–I_{IN})		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 400 mA		800	1000	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5, –40°C ≤ T_J ≤ +100°C		0.02	1	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 400 mA		58		dB
			f = 10 kHz, I_{OUT} = 400 mA		37		
V_N	Output noise voltage BW = 10 Hz – 100 kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs
V_{EN}(HI)	EN pin high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	EN pin low (shutdown)			0		0.5	V
I_{EN}(HI)	EN pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+160		°C
			Reset, temperature decreasing		+140		
T_A	Ambient operating temperature			–40		+125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6 V, the output will lock to V_{IN} and may result in a damaging overvoltage level on the output. To avoid this situation, disable the device before powering down the V_{IN}.
(3) Tolerance of external resistors not included in this specification.
(4) Fixed-voltage versions only; refer to APPLICATION INFORMATION section for more information.

PRODUCT PREVIEW

FUNCTIONAL BLOCK DIAGRAMS

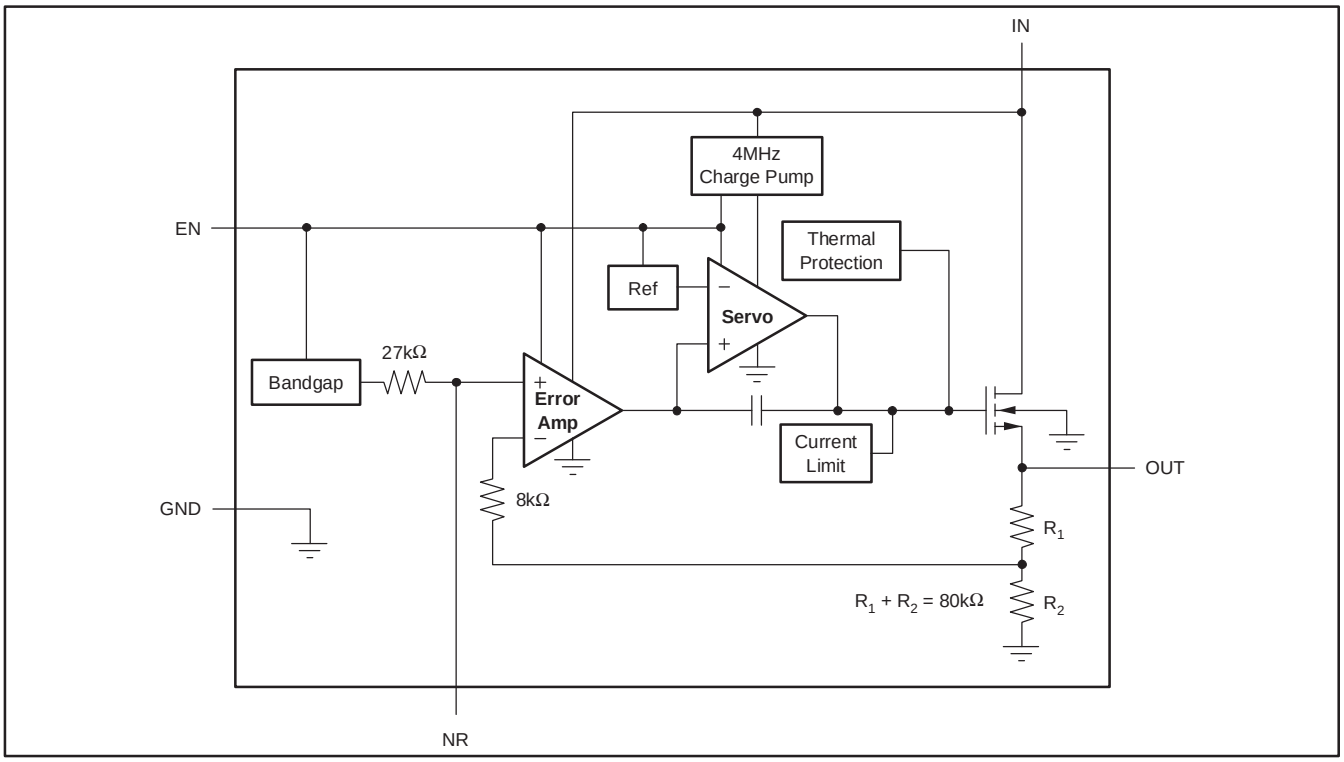
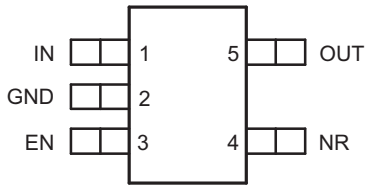


Figure 1. Fixed-Voltage Version

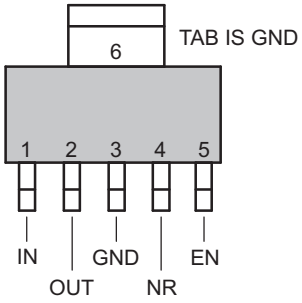
PRODUCT PREVIEW

PIN CONFIGURATIONS

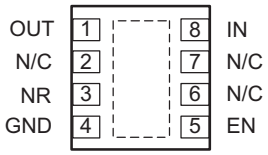
DBV PACKAGE
SOT23
(TOP VIEW)



DCQ PACKAGE
SOT223
(TOP VIEW)



DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



PIN DESCRIPTIONS

NAME	SOT23 (DBV) PIN NO.	SOT223 (DCQ) PIN NO.	3 × 3 SON (DRB) PIN NO.	DESCRIPTION
IN	1	1	8	Input supply
GND	2	3, 6	4, Pad	Ground
EN	3	5	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the ENABLE PIN AND SHUTDOWN section under APPLICATION INFORMATION for more details. Connect EN to IN when not in use.
NR	4	4	3	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
OUT	5	2	1	Output of the Regulator. There are no output capacitor requirements for stability.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

For all voltage versions, at T_A = +25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

LOAD REGULATION

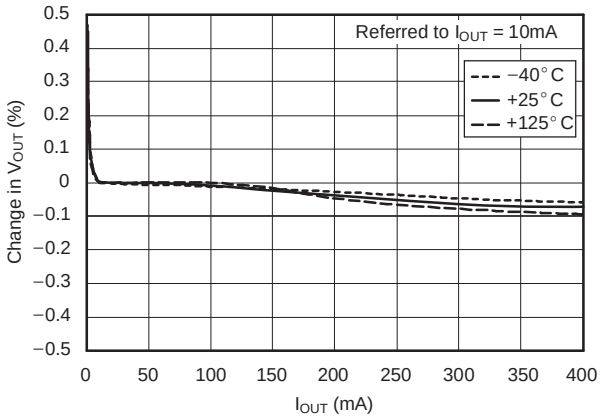


Figure 2.

LINE REGULATION

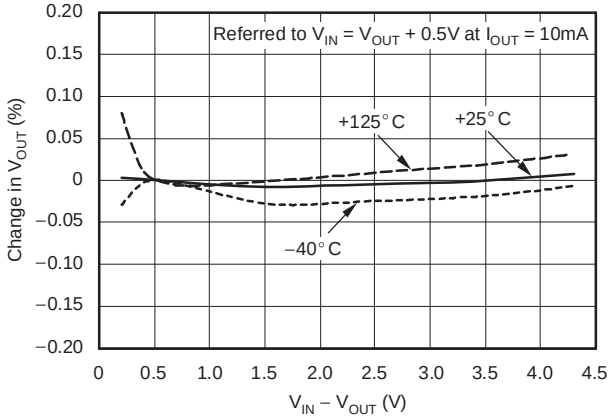


Figure 3.

DROPOUT VOLTAGE vs OUTPUT CURRENT

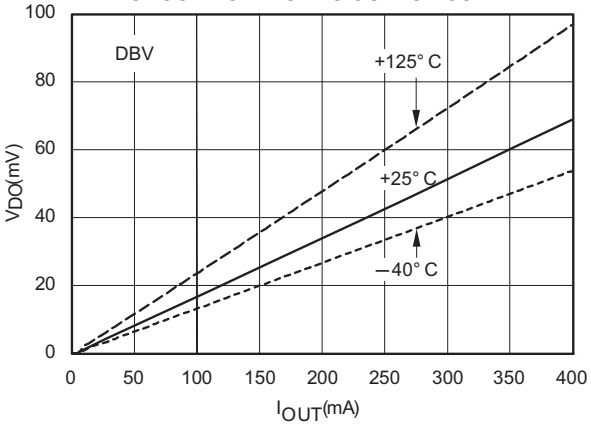


Figure 4.

DROPOUT VOLTAGE vs TEMPERATURE

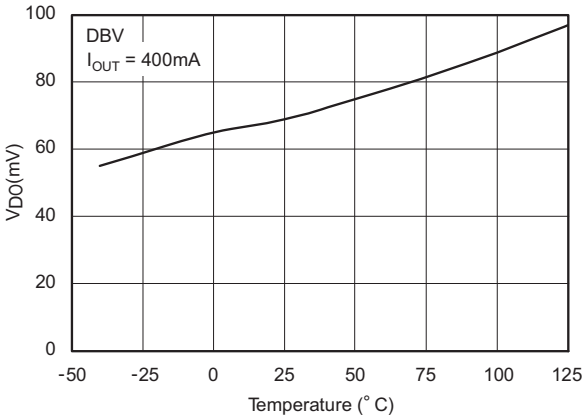


Figure 5.

OUTPUT-VOLTAGE ACCURACY HISTOGRAM

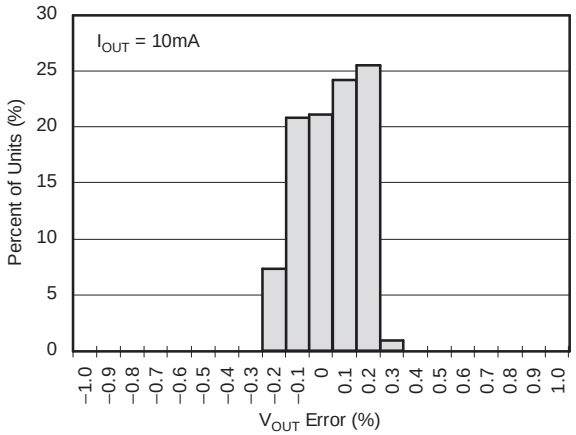


Figure 6.

OUTPUT-VOLTAGE DRIFT HISTOGRAM

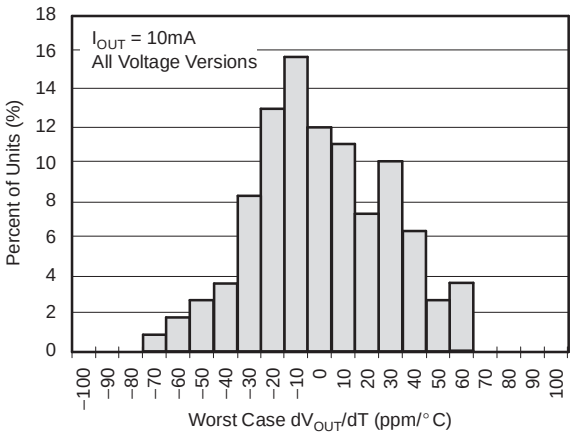


Figure 7.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at T_A = +25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

GROUND PIN CURRENT vs OUTPUT CURRENT

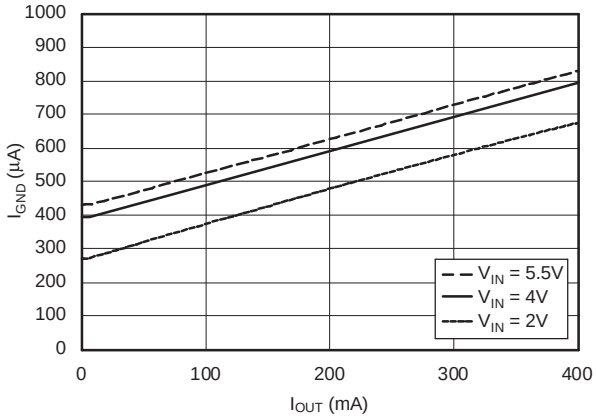


Figure 8.

GROUND PIN CURRENT vs TEMPERATURE

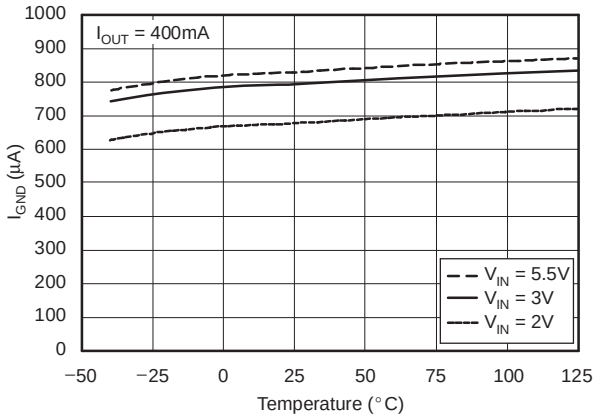


Figure 9.

GROUND PIN CURRENT in SHUTDOWN vs TEMPERATURE

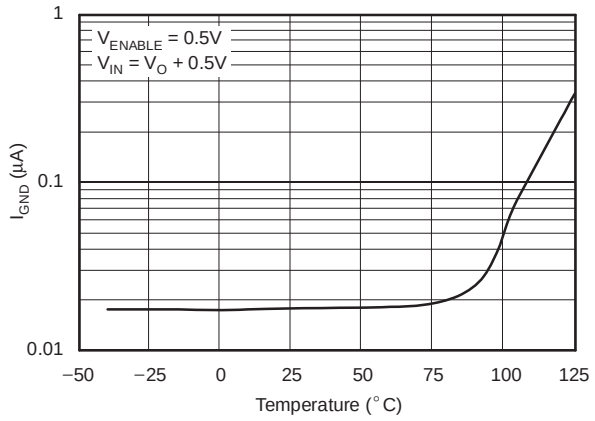


Figure 10.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

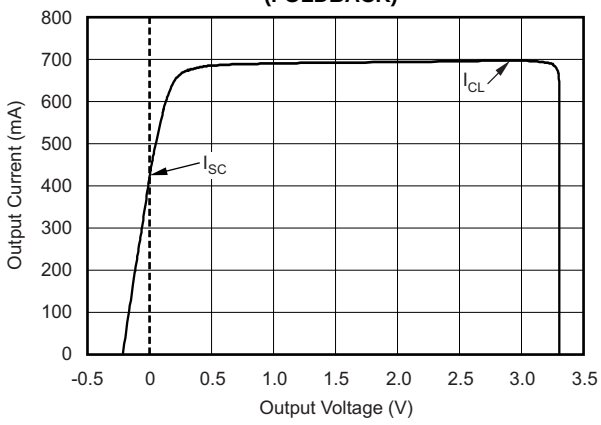


Figure 11.

CURRENT LIMIT vs V_{IN}

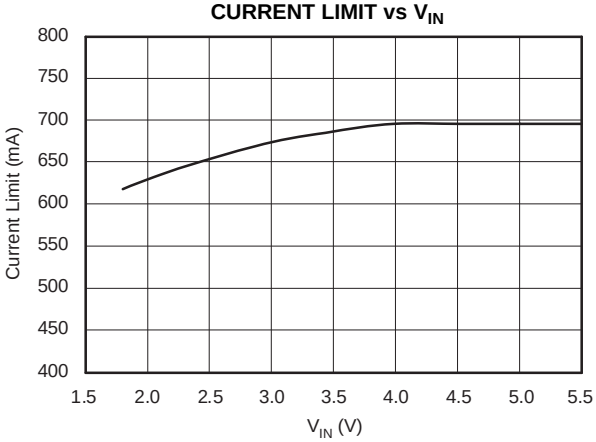


Figure 12.

CURRENT LIMIT vs TEMPERATURE

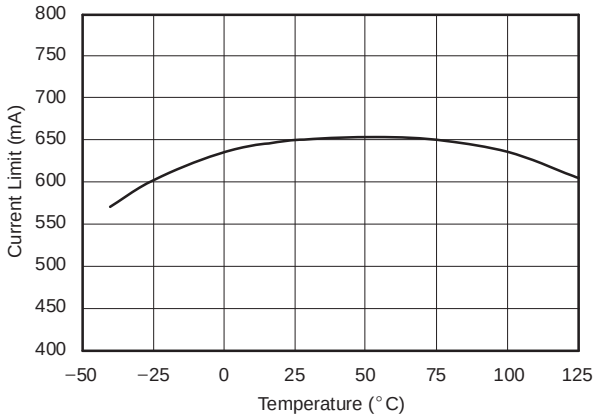


Figure 13.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at T_A = +25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

PSRR (RIPPLE REJECTION) vs FREQUENCY

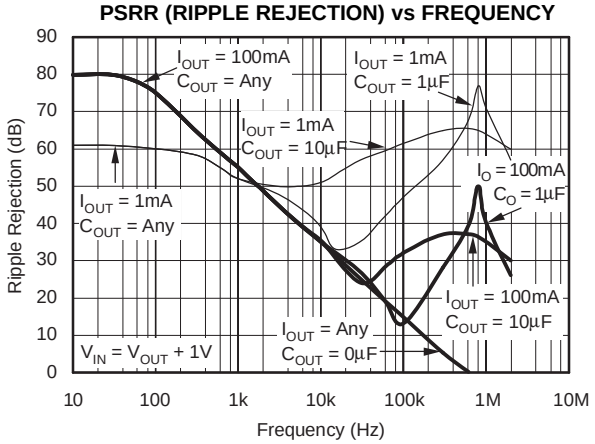


Figure 14.

PSRR (RIPPLE REJECTION) vs V_{IN} – V_{OUT}

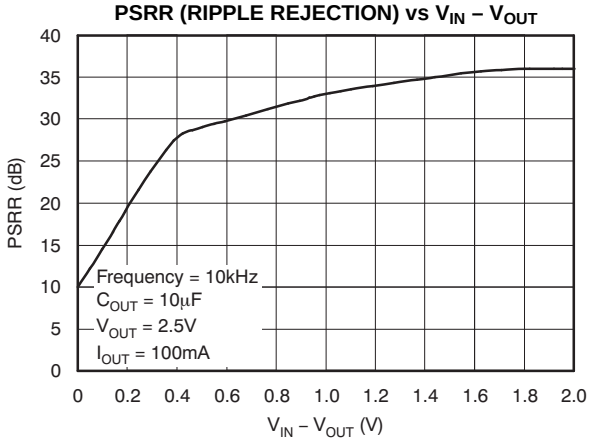


Figure 15.

NOISE SPECTRAL DENSITY
C_{NR} = 0 µF

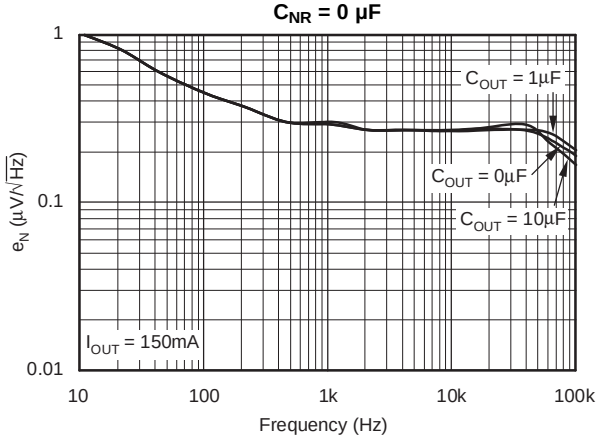


Figure 16.

NOISE SPECTRAL DENSITY
C_{NR} = 0.01 µF

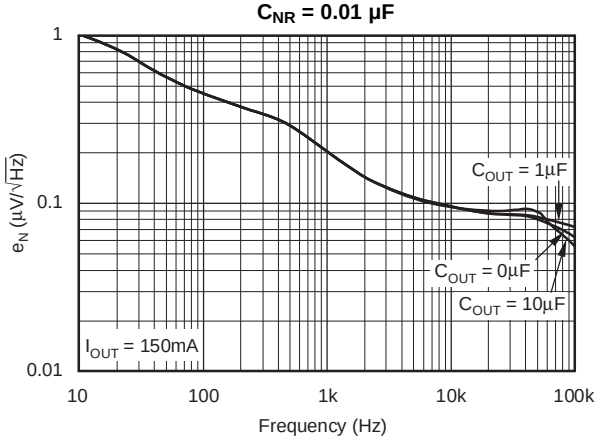


Figure 17.

RMS NOISE VOLTAGE vs C_{OUT}

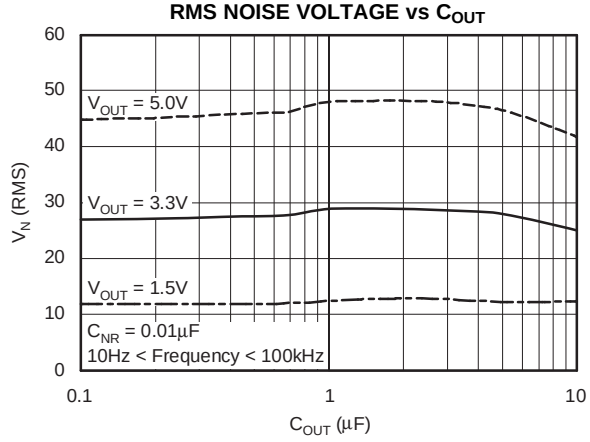


Figure 18.

RMS NOISE VOLTAGE vs C_{NR}

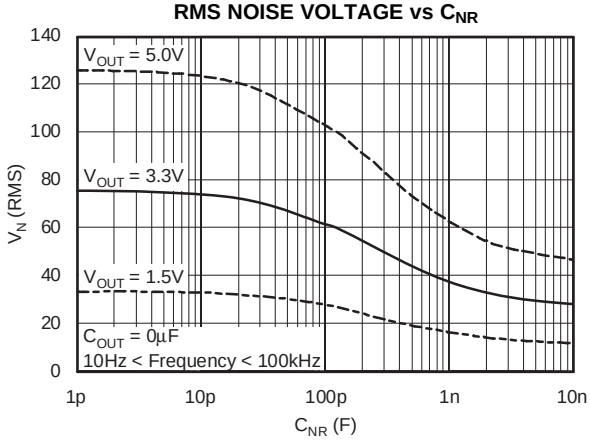


Figure 19.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at T_A = +25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

TPS736xx-Q1
LOAD-TRANSIENT RESPONSE

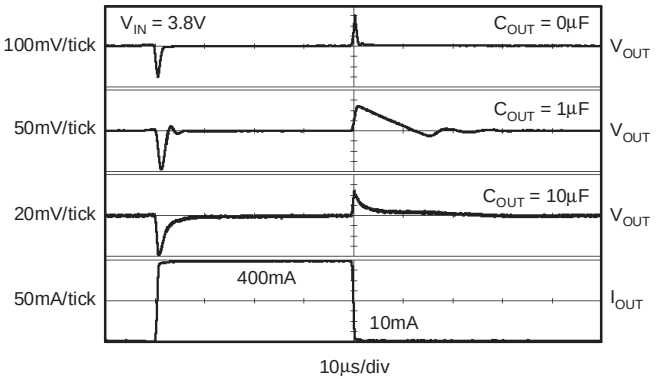


Figure 20.

TPS736xx-Q1
LINE-TRANSIENT RESPONSE

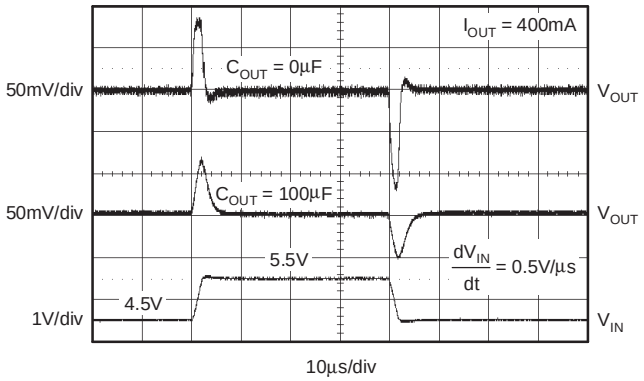


Figure 21.

TPS736xx-Q1
TURNON RESPONSE

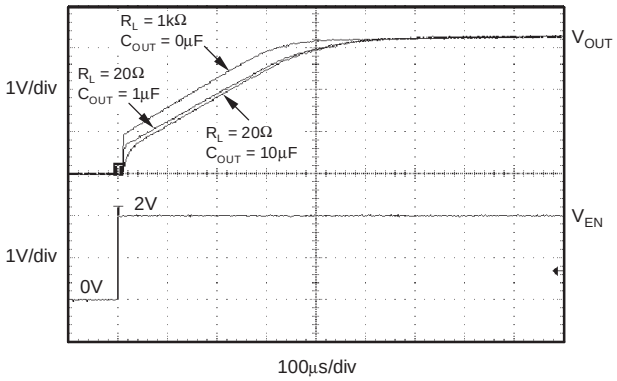


Figure 22.

TPS736xx-Q1
TURNOFF RESPONSE

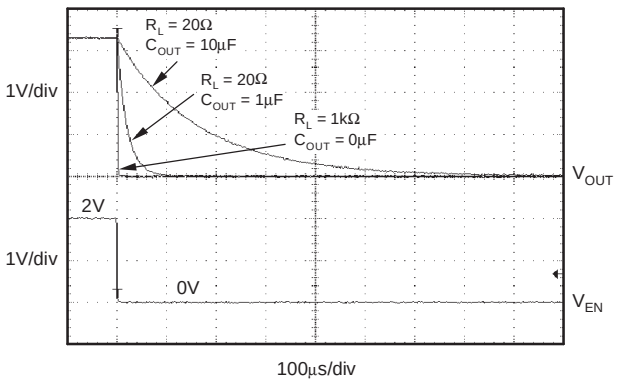


Figure 23.

TPS736xx-Q1
POWER UP / POWER DOWN

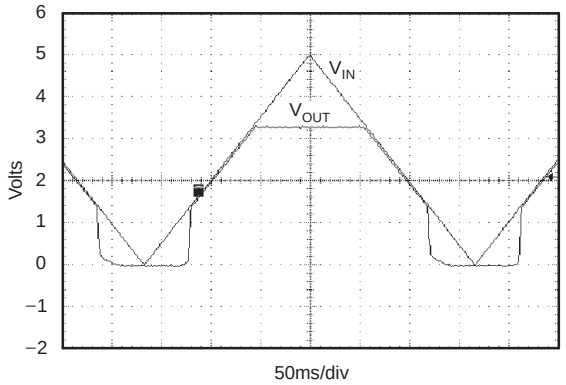


Figure 24.

I_{ENABLE} vs TEMPERATURE

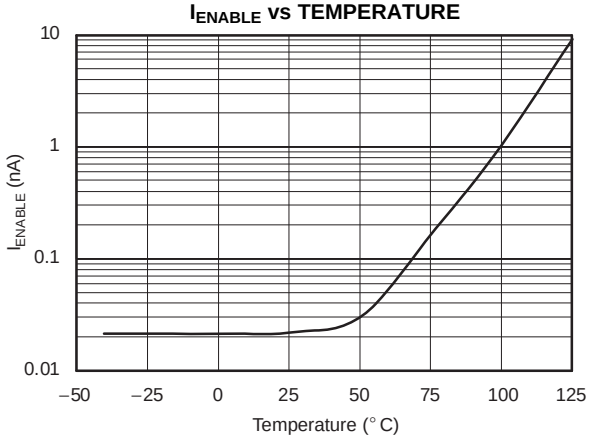


Figure 25.

PRODUCT PREVIEW

APPLICATION INFORMATION

The TPS736xx-Q1 belongs to a family of new-generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output-capacitor constraints. These features, combined with low noise and an enable input, make the TPS736xx-Q1 ideal for portable applications. This regulator family offers a wide selection of fixed-output-voltage versions. All versions have thermal and over-current protection, including foldback current limit. Figure 26 shows the basic circuit connections for the fixed-voltage models.

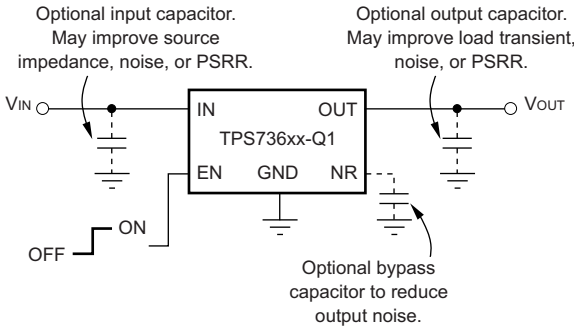


Figure 26. Typical Application Circuit for Fixed-Voltage Versions

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, connecting a 0.1- to 1-μF low-ESR capacitor across the input supply near the regulator is good analog-design practice. This connection counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS736xx-Q1 does not require an output capacitor for stability, and has maximum phase margin with no capacitor. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low-ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder-joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

OUTPUT NOISE

A precision band-gap reference generates the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS736xx-Q1 and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control-loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by Equation 1.

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2 V, this relationship reduces to that shown in Equation 2 for the case of no C_{NR}.

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship as shown in Equation 3 for C_{NR} = 10nF.

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

PRODUCT PREVIEW

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the TYPICAL CHARACTERISTICS section.

Connecting a capacitor, C_{NR}, from the output to the NR pin reduces output noise and improves load transient performance.

The TPS736xx-Q1 uses an internal charge pump to develop an internal supply voltage sufficient enough to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250 µV of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS736xx-Q1 internal current limit helps protect the regulator during fault conditions. Foldback-current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 11 in the TYPICAL CHARACTERISTICS section.

Note from Figure 11 that approximately –0.2 V of V_{OUT} results in a current limit of 0 mA. Therefore, if OUT is forced below –0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS736xx-Q1 must be enabled first.

ENABLE PIN AND SHUTDOWN

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (max) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 22).

When shutdown capability is not required, connect EN to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario results in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

Note that currentlimit foldback prevents device start-up under some conditions. See the *INTERNAL CURRENT LIMIT* section for more information.

DROPOUT VOLTAGE

The TPS736xx-Q1 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in the linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large-step changes in load current, the TPS736xx-Q1 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region causes an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load-current rate, the rate-of-change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS736xx-Q1 takes a couple of hundred microseconds to return to the specified regulation accuracy.

TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage-follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 µF) from the OUT pin to ground reduces undershoot-magnitude but increase the duration. The addition of a capacitor, C_{NR}, from the OUT pin to the NR pin also improves the transient response.

The TPS736xx-Q1 does not have active pull-down when the output is over-voltage which allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot is reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by Equation 4.

(Fixed Voltage Version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

REVERSE CURRENT

The NMOS pass element of the TPS736xx-Q1 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80-kΩ internal resistor-divider to ground (see Figure 1).

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least +35°C above the maximum expected ambient condition of your application which produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736xx-Q1 is designed to protect against overload conditions. The device is not intended to replace proper heat sinking. Continuously running the TPS736xx-Q1 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Using the lowest possible input voltage necessary to assure the required output voltage minimizes power dissipation.

PRODUCT PREVIEW

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS736xx-Q1 are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the Texas Instruments Web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73618QDCQRQ1	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	73618Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

OTHER QUALIFIED VERSIONS OF TPS73618-Q1 :

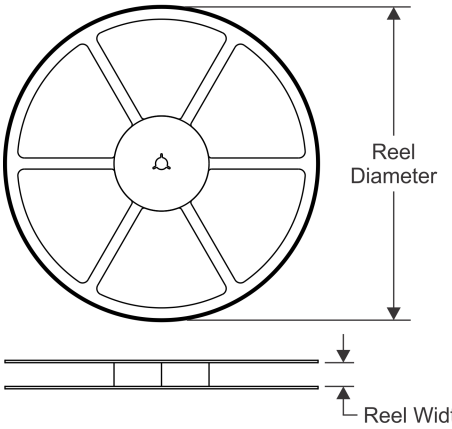
- Catalog: TPS73618
- Enhanced Product: TPS73618-EP

NOTE: Qualified Version Definitions:

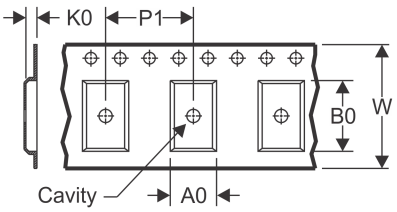
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

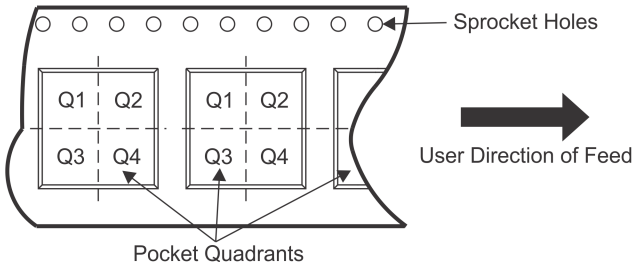


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

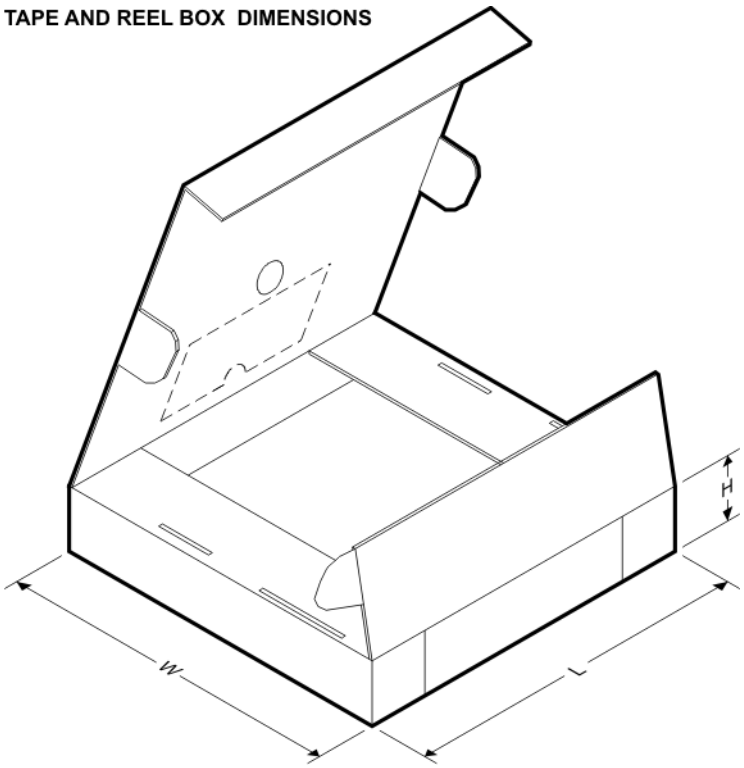
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73618QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

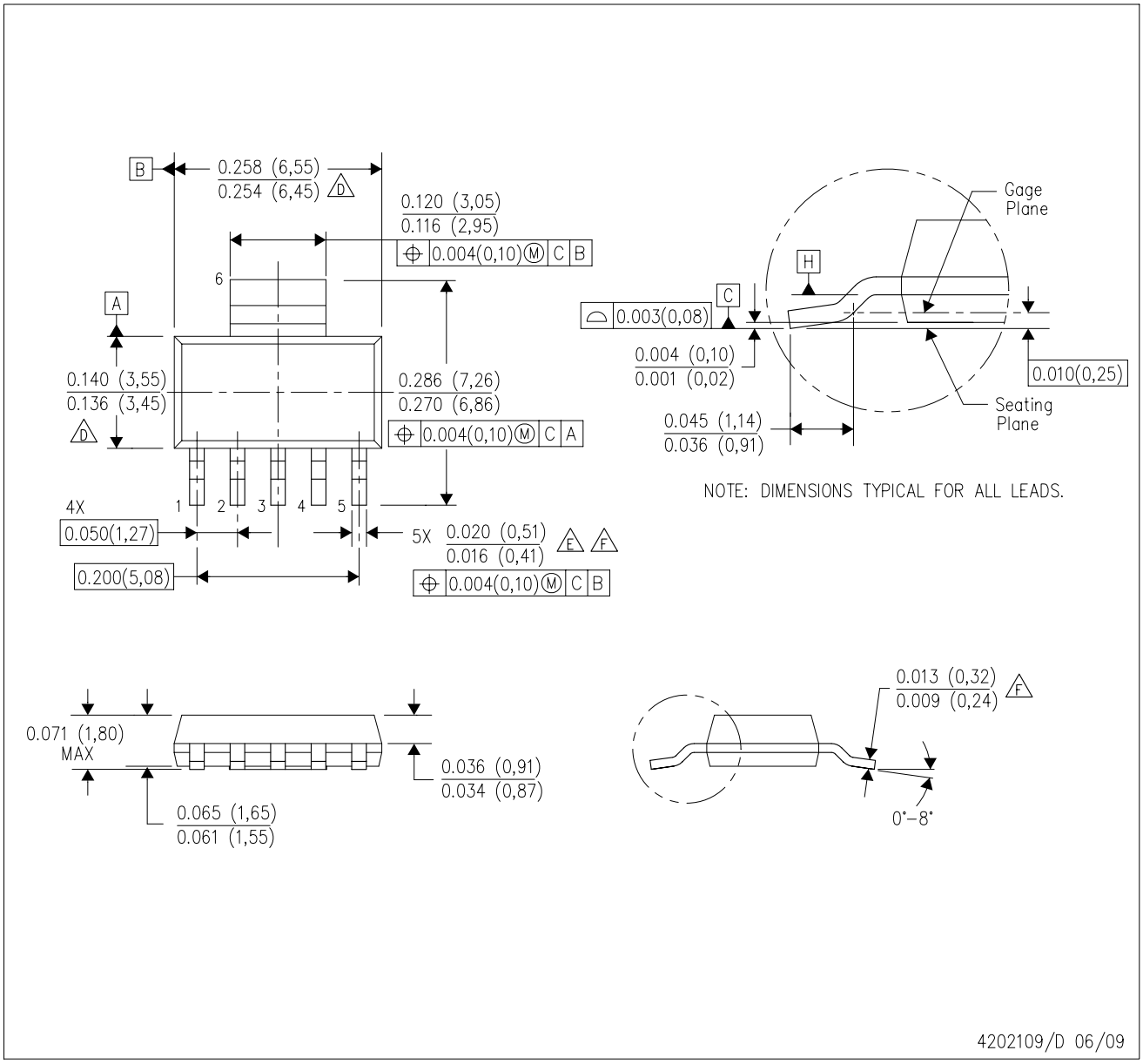
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

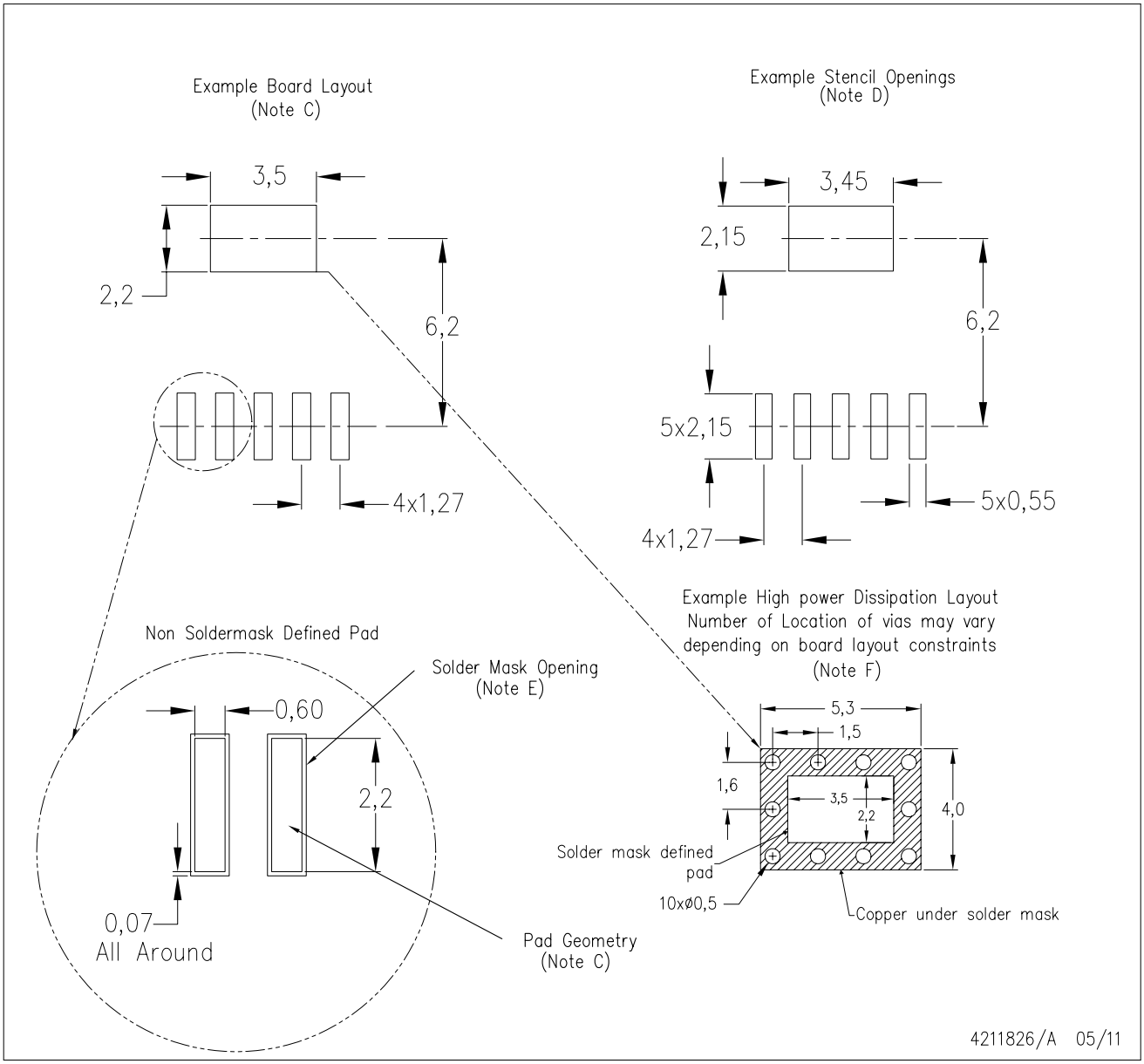
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73618QDCQRQ1	SOT-223	DCQ	6	2500	358.0	335.0	35.0

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.

DCQ (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. Please refer to the product data sheet for specific via and thermal dissipation requirements.

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