

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild  $\mu$ A741**

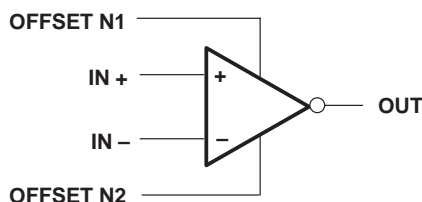
## description

The  $\mu$ A741 is a general-purpose operational amplifier featuring offset-voltage null capability.

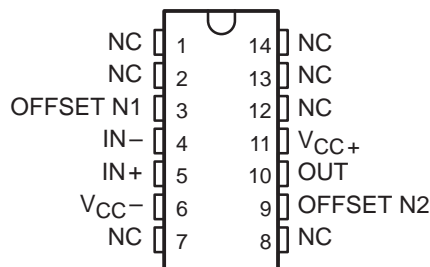
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The  $\mu$ A741C is characterized for operation from 0°C to 70°C. The  $\mu$ A741I is characterized for operation from –40°C to 85°C. The  $\mu$ A741M is characterized for operation over the full military temperature range of –55°C to 125°C.

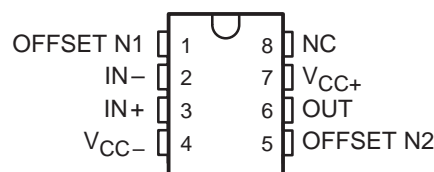
## symbol



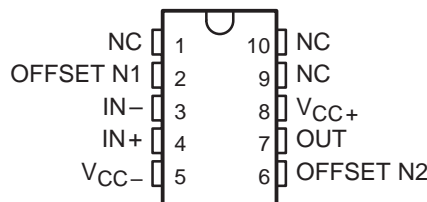
$\mu$ A741M . . . J PACKAGE  
(TOP VIEW)



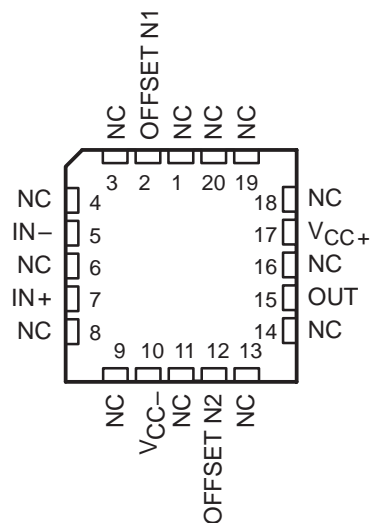
$\mu$ A741M . . . JG PACKAGE  
 $\mu$ A741C,  $\mu$ A741I . . . D, P, OR PW PACKAGE  
(TOP VIEW)



$\mu$ A741M . . . U PACKAGE  
(TOP VIEW)



$\mu$ A741M . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

μA741, μA741Y  
 GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

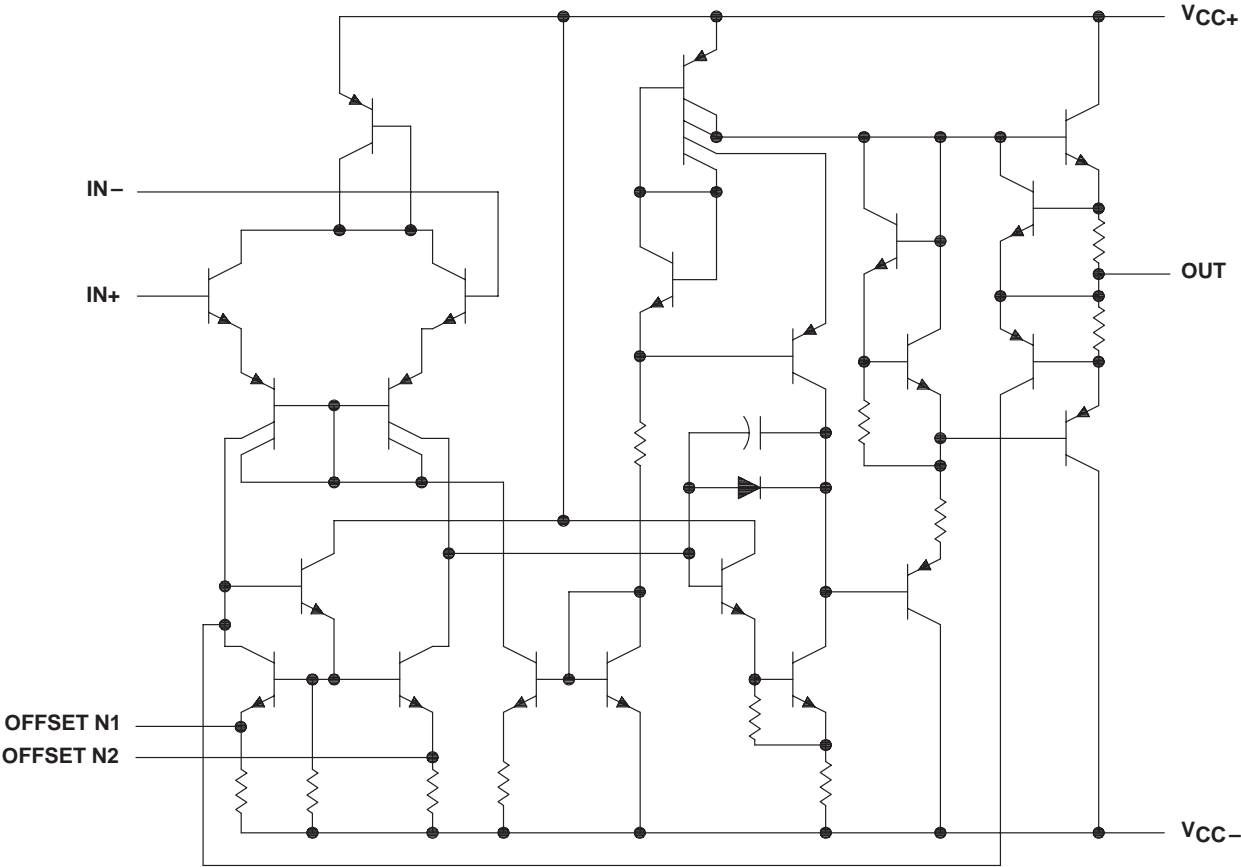
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AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES							CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	
0°C to 70°C	μA741CD				μA741CP	μA741CPW		μA741Y
–40°C to 85°C	μA741ID				μA741IP			
–55°C to 125°C		μA741MFK	μA741MJ	μA741MJG			μA741MU	

The D package is available taped and reeled. Add the suffix R (e.g., μA741CDR).

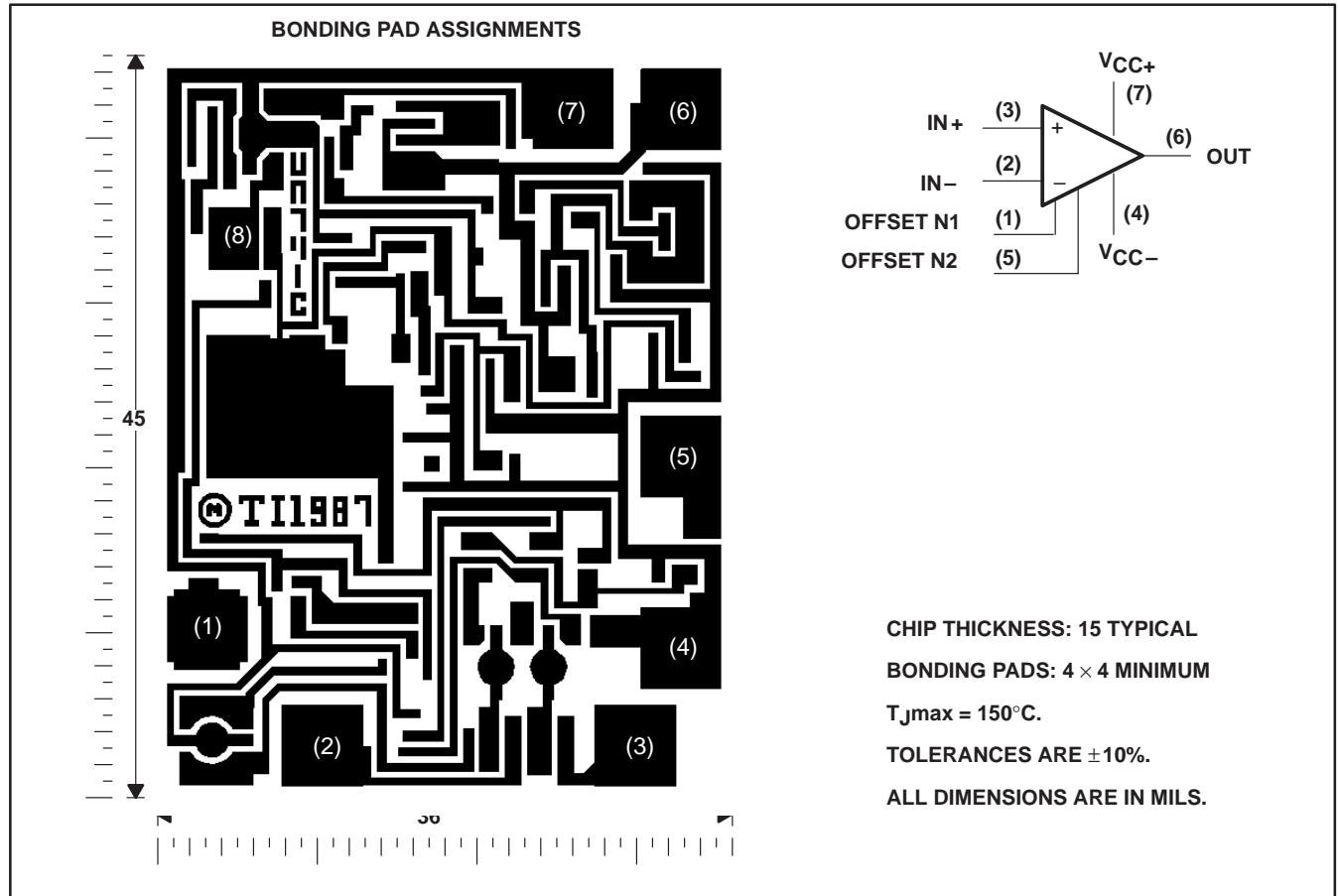
schematic



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

### $\mu$ A741Y chip information

This chip, when properly assembled, displays characteristics similar to the  $\mu$ A741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



# **μA741, μA741Y** **GENERAL-PURPOSE OPERATIONAL AMPLIFIERS**

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## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

	μA741C	μA741I	μA741M	UNIT
Supply voltage, $V_{CC+}$ (see Note 1)	18	22	22	V
Supply voltage, $V_{CC-}$ (see Note 1)	-18	-22	-22	V
Differential input voltage, $V_{ID}$ (see Note 2)	±15	±30	±30	V
Input voltage, $V_I$ any input (see Notes 1 and 3)	±15	±15	±15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and $V_{CC-}$	±15	±0.5	±0.5	V
Duration of output short circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total power dissipation	See Dissipation Rating Table			
Operating free-air temperature range, $T_A$	0 to 70	-40 to 85	-55 to 125	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package		300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, P, or PW package		260	°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at  $IN+$  with respect to  $IN-$ .
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the μA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE $T_A$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

# $\mu\text{A741}$ , $\mu\text{A741Y}$ GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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**electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	$\mu\text{A741C}$			$\mu\text{A741I}$ , $\mu\text{A741M}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
		Full range			7.5			6	
$\Delta V_{IO(\text{adj})}$ Offset voltage adjust range	$V_O = 0$	25°C		$\pm 15$			$\pm 15$		mV
$I_{IO}$ Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
		Full range			300			500	
$I_{IB}$ Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
		Full range			800			1500	
$V_{ICR}$ Common-mode input voltage range		25°C	$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
		Full range	$\pm 12$			$\pm 12$			
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	25°C	$\pm 12$	$\pm 14$		$\pm 12$	$\pm 14$		V
	$R_L \geq 10\text{ k}\Omega$	Full range	$\pm 12$			$\pm 12$			
	$R_L = 2\text{ k}\Omega$	25°C	$\pm 10$	$\pm 13$		$\pm 10$	$\pm 13$		
	$R_L \geq 2\text{ k}\Omega$	Full range	$\pm 10$			$\pm 10$			
$A_{VD}$ Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$	25°C	20	200		50	200		V/mV
	$V_O = \pm 10\text{ V}$	Full range	15			25			
$r_i$ Input resistance		25°C	0.3	2		0.3	2		M $\Omega$
$r_o$ Output resistance	$V_O = 0$ , See Note 5	25°C		75			75		$\Omega$
$C_i$ Input capacitance		25°C		1.4			1.4		pF
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}$	25°C	70	90		70	90		dB
		Full range	70			70			
$k_{SVS}$ Supply voltage sensitivity ( $\Delta V_{IO}/\Delta V_{CC}$ )	$V_{CC} = \pm 9\text{ V to } \pm 15\text{ V}$	25°C		30	150		30	150	$\mu\text{V/V}$
		Full range			150			150	
$I_{OS}$ Short-circuit output current		25°C		$\pm 25$	$\pm 40$		$\pm 25$	$\pm 40$	mA
$I_{CC}$ Supply current	$V_O = 0$ , No load	25°C		1.7	2.8		1.7	2.8	mA
		Full range			3.3			3.3	
$P_D$ Total power dissipation	$V_O = 0$ , No load	25°C		50	85		50	85	mW
		Full range			100			100	

$^\dagger$  All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the  $\mu\text{A741C}$  is 0°C to 70°C, the  $\mu\text{A741I}$  is –40°C to 85°C, and the  $\mu\text{A741M}$  is –55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

**operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	$\mu\text{A741C}$			$\mu\text{A741I}$ , $\mu\text{A741M}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_r$ Rise time	$V_I = 20\text{ mV}$ , $R_L = 2\text{ k}\Omega$		0.3			0.3		$\mu\text{s}$
Overshoot factor	$C_L = 100\text{ pF}$ , See Figure 1		5%			5%		
SR Slew rate at unity gain	$V_I = 10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		0.5			0.5		V/ $\mu\text{s}$



# **μA741, μA741Y** **GENERAL-PURPOSE OPERATIONAL AMPLIFIERS**

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**electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15$  V,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_O = 0$		1	6	mV
$\Delta V_{IO(\text{adj})}$	Offset voltage adjust range	$V_O = 0$		±15		mV
$I_{IO}$	Input offset current	$V_O = 0$		20	200	nA
$I_{IB}$	Input bias current	$V_O = 0$		80	500	nA
$V_{ICR}$	Common-mode input voltage range		±12	±13		V
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	±12	±14		V
		$R_L = 2\text{ k}\Omega$	±10	±13		
$A_{VD}$	Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega$	20	200		V/mV
$r_i$	Input resistance		0.3	2		MΩ
$r_o$	Output resistance	$V_O = 0$ , See Note 5		75		Ω
$C_i$	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}$	70	90		dB
$k_{SVS}$	Supply voltage sensitivity ( $\Delta V_{IO}/\Delta V_{CC}$ )	$V_{CC} = \pm 9\text{ V to } \pm 15\text{ V}$		30	150	μV/V
$I_{OS}$	Short-circuit output current		±25	±40		mA
$I_{CC}$	Supply current	$V_O = 0$ , No load		1.7	2.8	mA
$P_D$	Total power dissipation	$V_O = 0$ , No load		50	85	mW

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

**operating characteristics,  $V_{CC\pm} = \pm 15$  V,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
$t_r$	Rise time	$V_I = 20\text{ mV}$ , $R_L = 2\text{ k}\Omega$ ,		0.3		μs
	Overshoot factor	$C_L = 100\text{ pF}$ , See Figure 1		5%		
SR	Slew rate at unity gain	$V_I = 10\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		0.5		V/μs



## PARAMETER MEASUREMENT INFORMATION

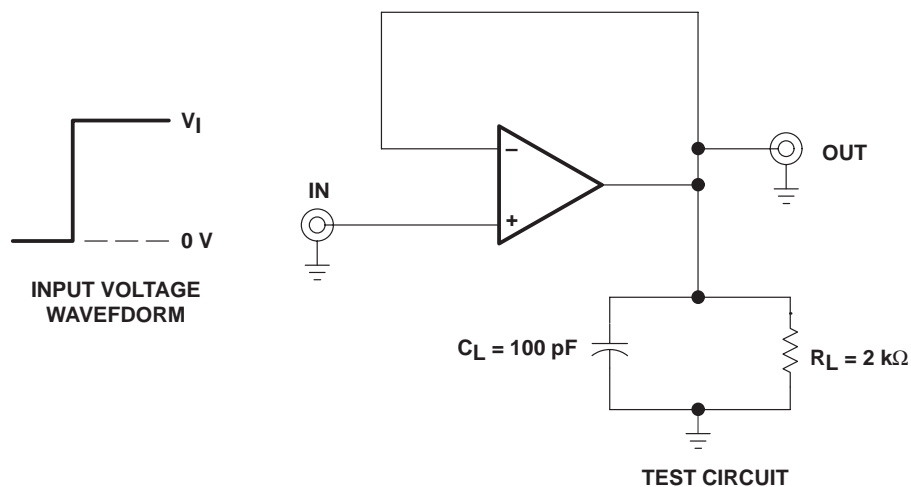


Figure 1. Rise Time, Overshoot, and Slew Rate

## APPLICATION INFORMATION

Figure 2 shows a diagram for an input offset voltage null circuit.

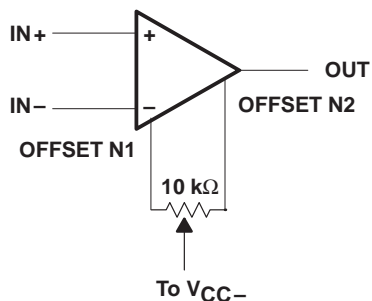


Figure 2. Input Offset Voltage Null Circuit

# $\mu$ A741, $\mu$ A741Y GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS†

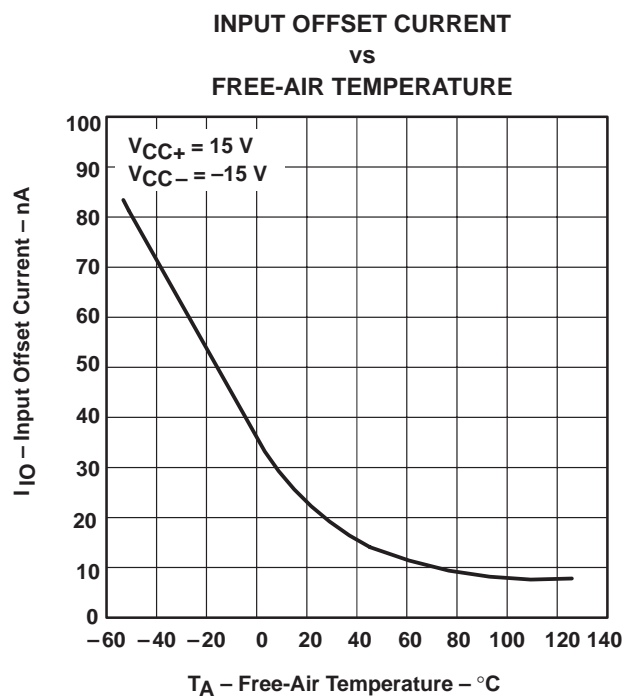


Figure 3

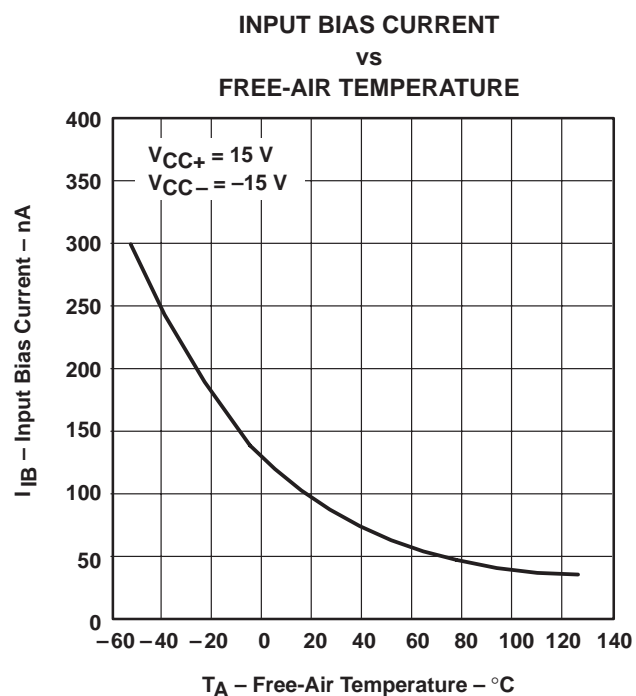


Figure 4

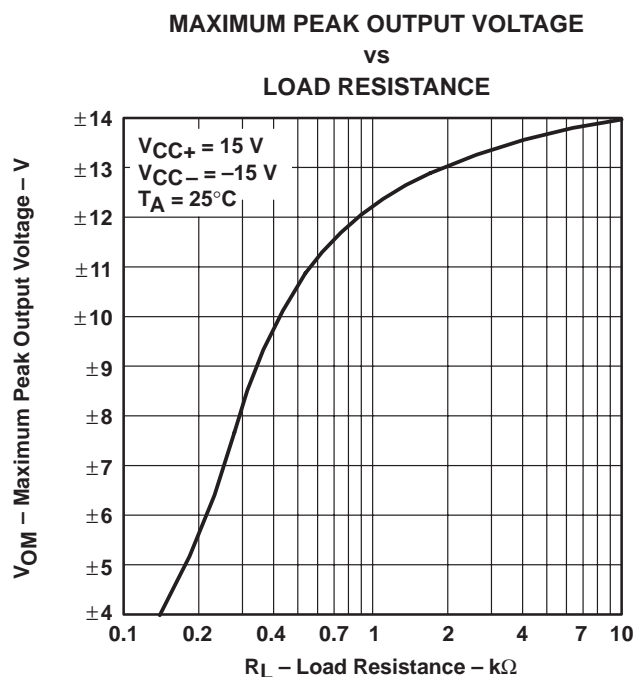


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



## TYPICAL CHARACTERISTICS

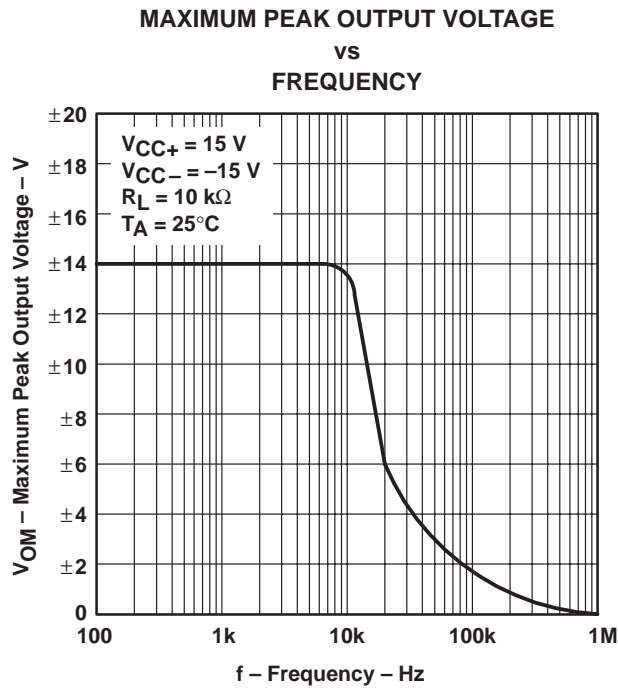


Figure 6

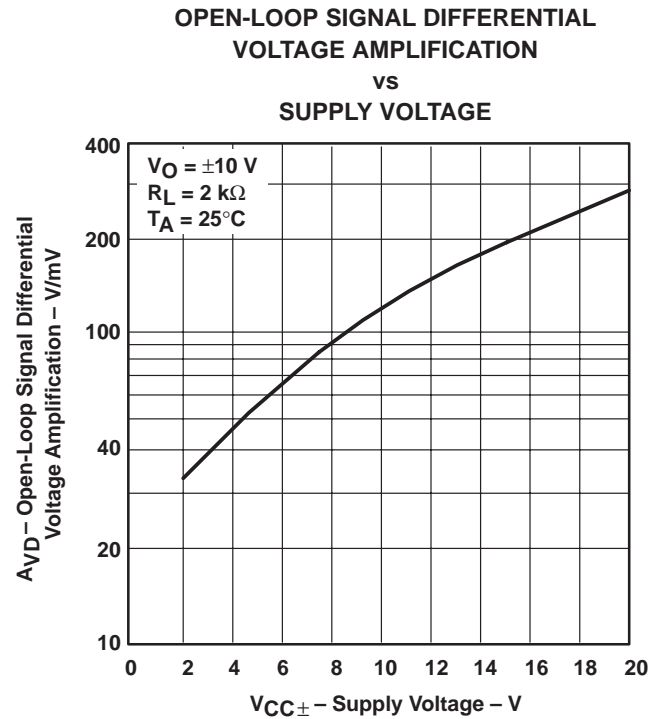
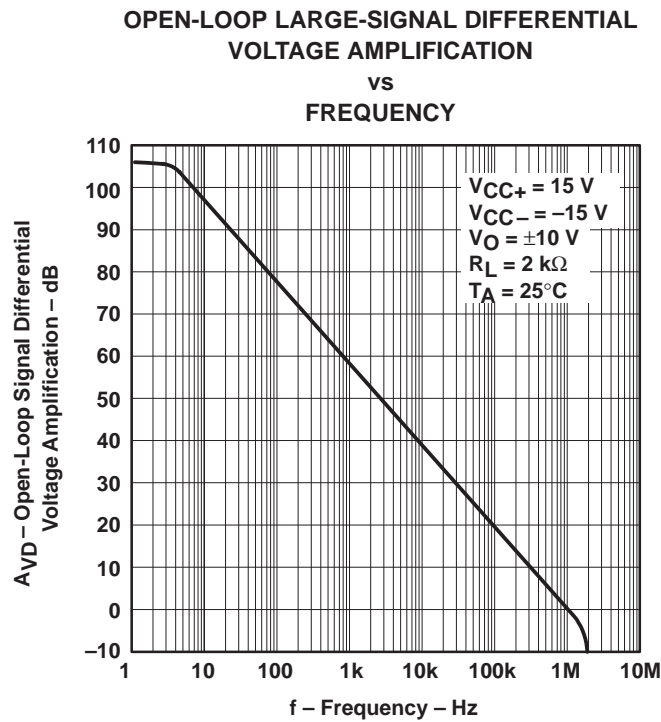


Figure 7



# $\mu$ A741, $\mu$ A741Y GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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## TYPICAL CHARACTERISTICS

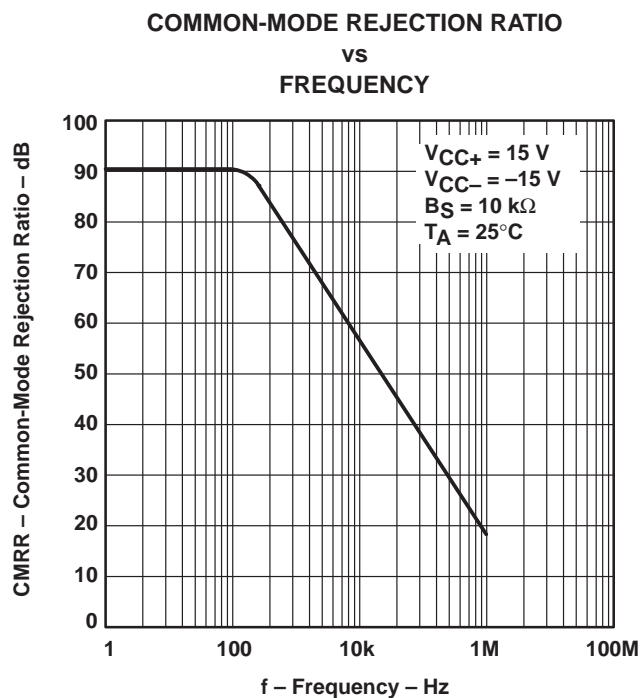


Figure 8

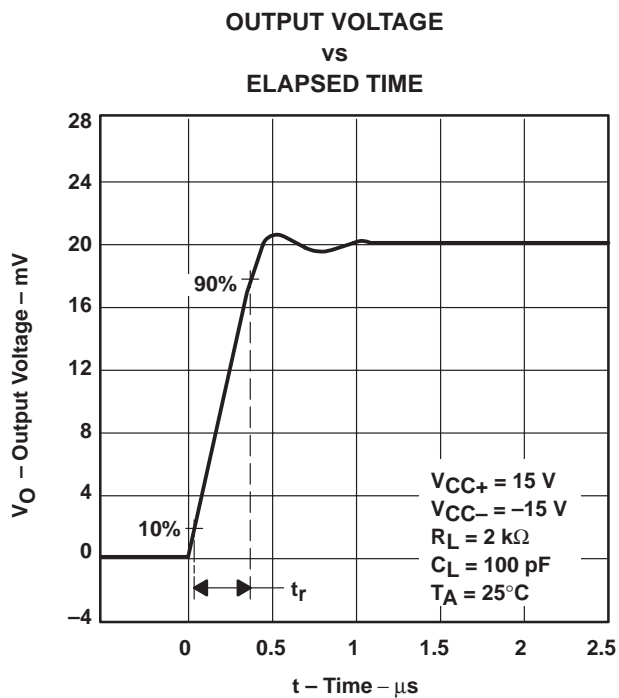


Figure 9

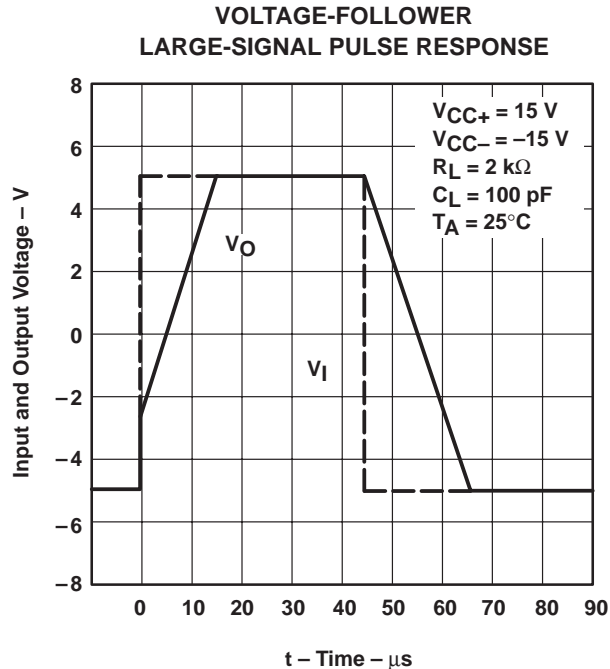


Figure 10

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
UA741CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
UA741CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
UA741CJG	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UA741CJG4	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UA741CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
UA741CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
UA741MFKB	OBSOLETE	LCCC	FK	20		None	Call TI	Call TI
UA741MJ	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
UA741MJB	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
UA741MJG	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI
UA741MJGB	OBSOLETE	CDIP	JG	8		None	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## JG (R-GDIP-T8)

## CERAMIC DUAL-IN-LINE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification.
  - Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE

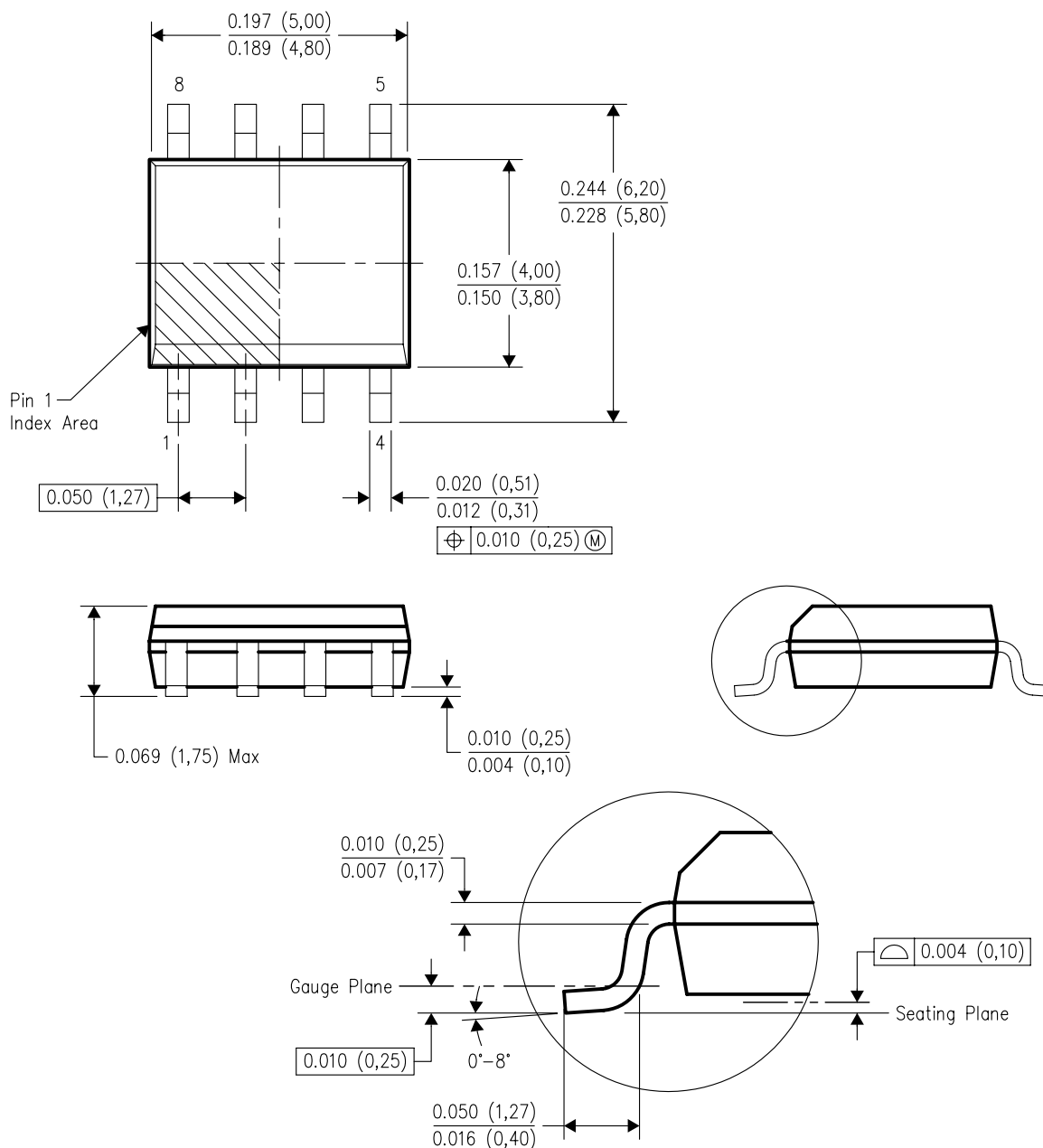


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

## D (R-PDSO-G8)

# PLASTIC SMALL-OUTLINE PACKAGE



4040047-2/F 07/2004

- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-012 variation AA.



## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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