

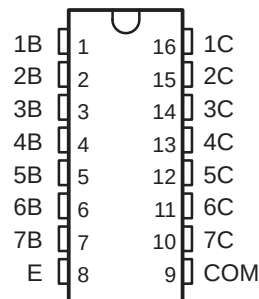
ULQ2003A-Q1, ULQ2004A-Q1, HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SGLS148A – DECEMBER 2002 – REVISED OCTOBER 2004

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

† Contact Texas Instruments for details. Q100 qualification data available on request.

**D PACKAGE
(TOP VIEW)**



description

The ULQ2003A-Q1 and ULQ2004A-Q1 are high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULQ2003A-Q1 has a 2.7-k Ω series base resistor for each Darlington pair, for operation directly with TTL or 5-V CMOS devices. The ULQ2004A-Q1 has a 10.5-k Ω series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULQ2004A-Q1 is below that of the ULQ2003A-Q1.

AVAILABLE OPTIONS

T _A	D PACKAGES†
	SMALL OUTLINE
–40°C to 105°C	ULQ2003ATDQ1 ULQ2003ATDRQ1
	ULQ2004ATDQ1‡ ULQ2004ATDRQ1

† The D package is available taped and reeled. Add the suffix R to device type (e.g., ULQ2003TDADRQ1).

‡ ULQ2004ATDQ1 is Product Preview only.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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ULQ2003A-Q1: $R_B = 2.7\text{ k}\Omega$
ULQ2004A-Q1: $R_B = 10.5\text{ k}\Omega$

ULQ2003A-Q1, ULQ2004A-Q1

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DISSIPATION RATING TABLE

PACKAGE	T _A = 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 85°C POWER RATING	T _A = 105°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW	342 mW

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		ULQ2003A-Q1			ULQ2004A-Q1			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{I(on)}	On-state input voltage, See Figure 6	V _{CE} = 2 V	I _C = 125 mA						5	V
			I _C = 200 mA				2.7		6	
			I _C = 250 mA				2.9			
			I _C = 275 mA						7	
			I _C = 300 mA				3			
			I _C = 350 mA						8	
V _{CE(sat)}	Collector-emitter saturation voltage, See Figure 5	I _I = 250 μA, I _C = 100 mA		0.9	1.2		0.9	1.1	V	
		I _I = 350 μA, I _C = 200 mA		1	1.4		1	1.3		
		I _I = 500 μA, I _C = 350 mA		1.2	1.7		1.2	1.6		
I _{CEX}	Collector cutoff current	V _{CE} = 50 V, I _I = 0, See Figure 1			100			50	μA	
		V _{CE} = 50 V, See Figure 2	I _I = 0				100			
			V _I = 1 V				500			
V _F	Clamp forward voltage, See Figure 8	I _F = 350 mA			1.7	2.2		1.7	2.1	V
I _{I(off)}	Off-state input current, See Figure 3	V _{CE} = 50 V, I _C = 500 μA		30	65		50	65		μA
I _I	Input current, see Figure 4	V _I = 3.85 V			0.93	1.35				mA
		V _I = 5 V					0.35	0.5		
		V _I = 12 V					1	1.45		
I _R	Clamp reverse current, See Figure 7	V _R = 50 V, T _A = 25°C			100			50		μA
		V _R = 50 V			100			100		
C _i	Input capacitance	V _I = 0, f = 1 MHz		15	25		15	25		pF

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ULQ2003A-Q1, ULQ2004A-Q1			UNIT
			MIN	TYP	MAX	
t _{PLH}	Propagation delay time, low-to-high level output	See Figure 9	1		10	μs
t _{PHL}	Propagation delay time, high-to-low level output	See Figure 9	1		10	μs
V _{OH}	High-level output voltage after switching	V _S = 50 V, I _O ≈ 300 mA, See Figure 10	V _S -500			mV



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PARAMETER MEASUREMENT INFORMATION

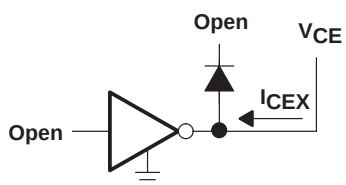


Figure 1. I_{CEX} Test Circuit

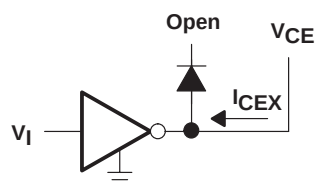


Figure 2. I_{CEX} Test Circuit

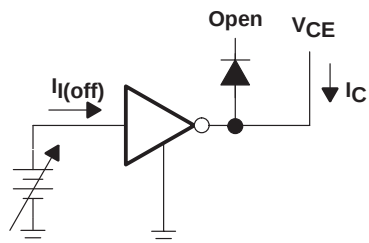


Figure 3. $I_{I(off)}$ Test Circuit

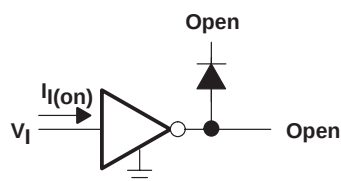
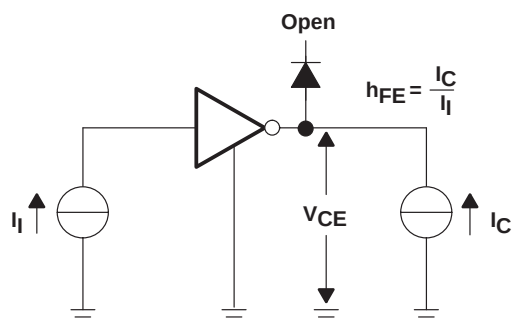


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

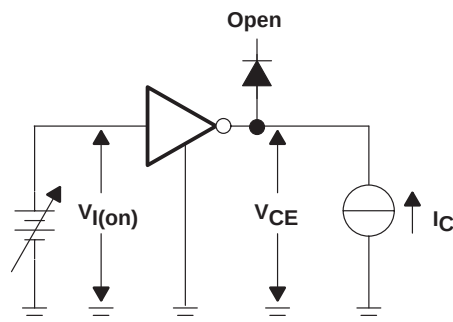


Figure 6. $V_{I(on)}$ Test Circuit

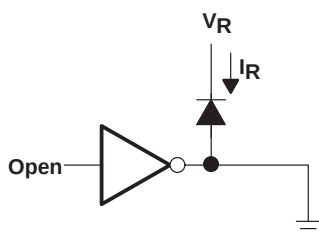


Figure 7. I_R Test Circuit

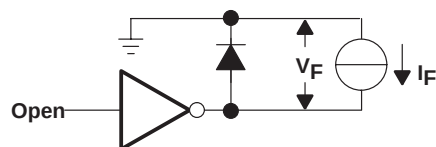


Figure 8. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION

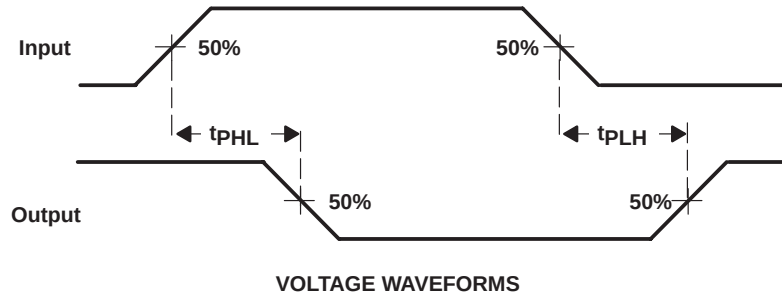
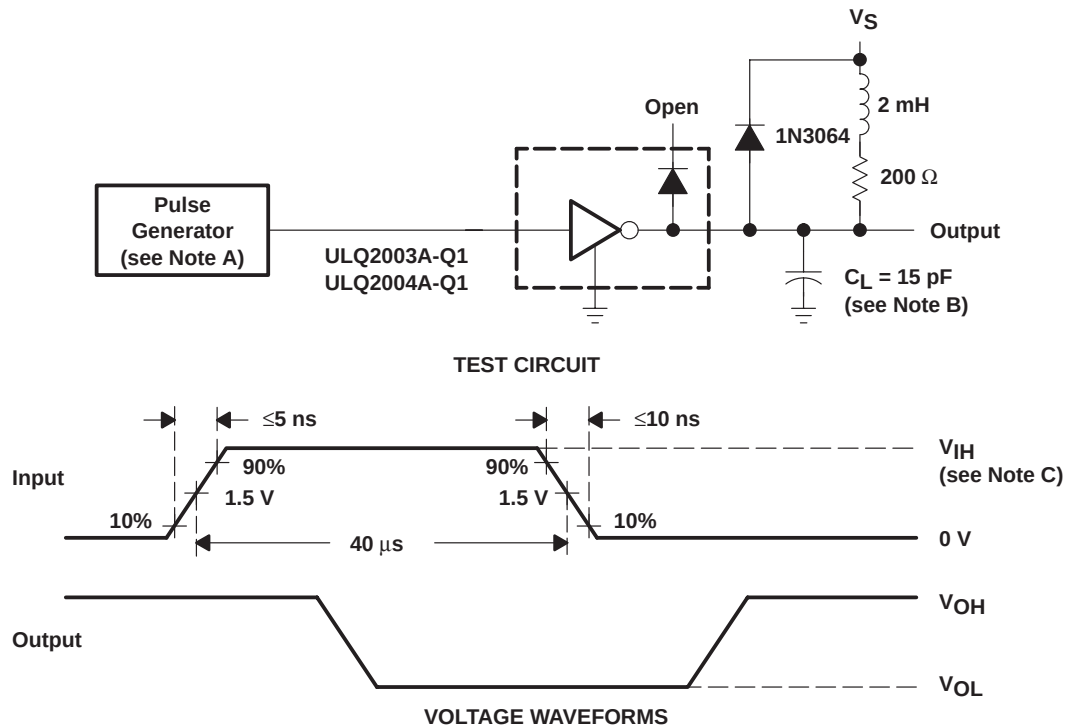


Figure 9. Propagation Delay-Time Waveforms



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. For testing the ULQ2003A-Q1, $V_{IH} = 3 \text{ V}$; for the ULQ2004A-Q1, $V_{IH} = 8 \text{ V}$.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE

VS

COLLECTOR CURRENT
(ONE DARLINGTON)

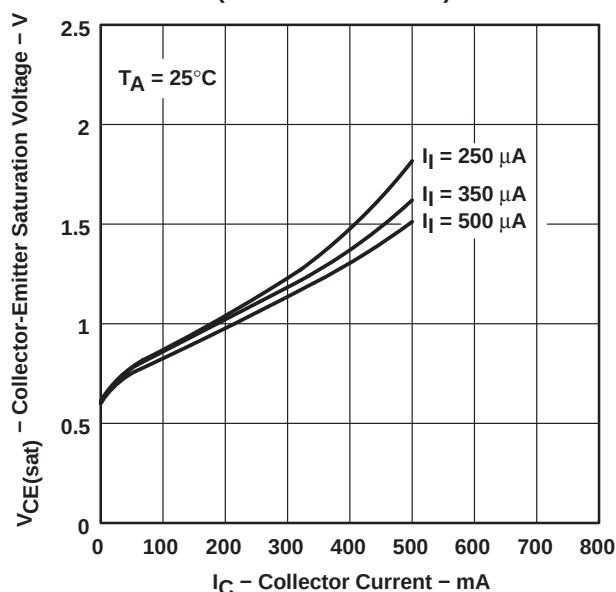


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE

VS

TOTAL COLLECTOR CURRENT
(TWO DARLINGTONS IN PARALLEL)

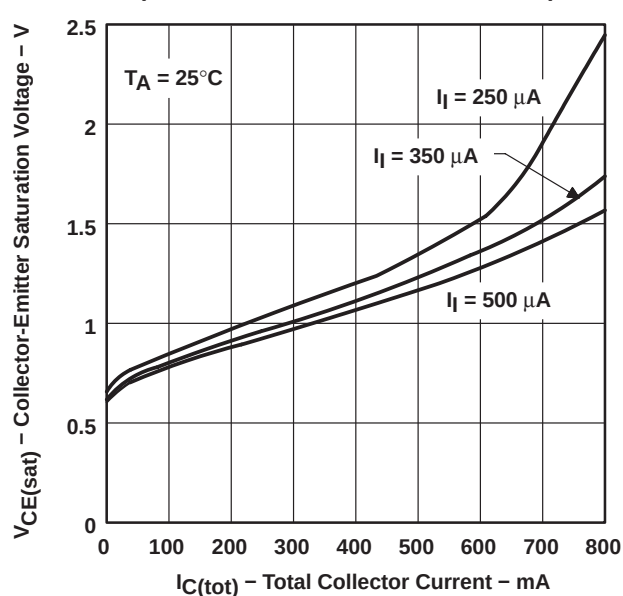


Figure 12

COLLECTOR CURRENT

VS

INPUT CURRENT

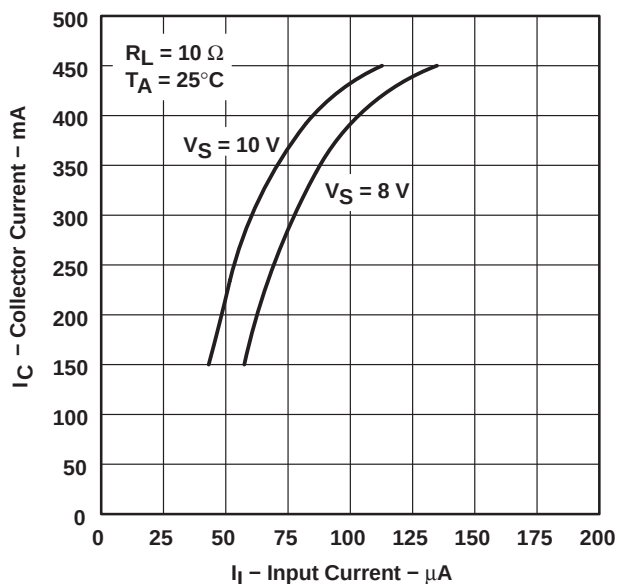


Figure 13

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

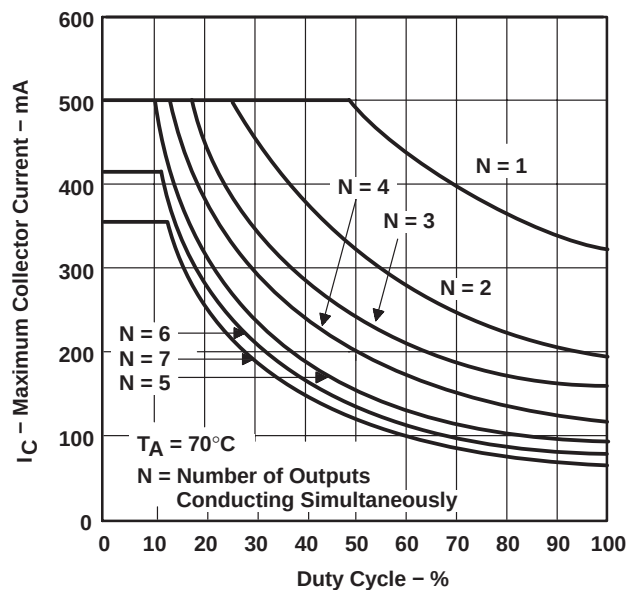


Figure 14

ULQ2003A-Q1, ULQ2004A-Q1, HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

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APPLICATION INFORMATION

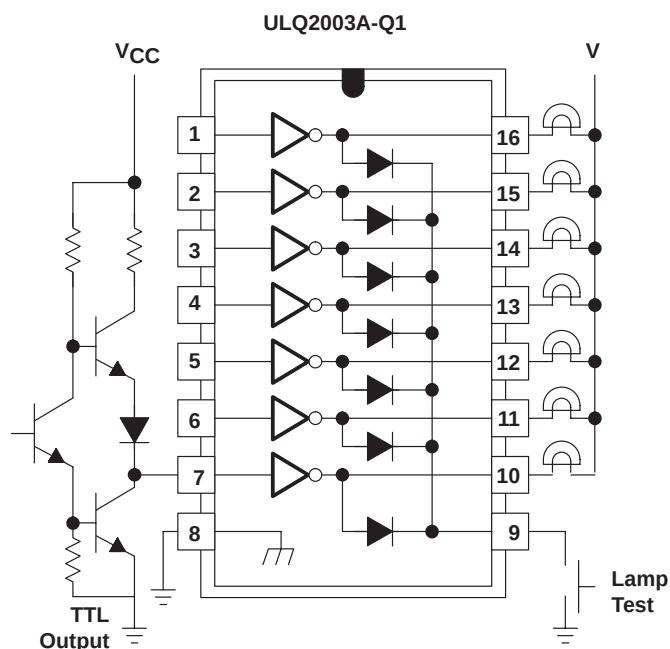


Figure 15. TTL to Load

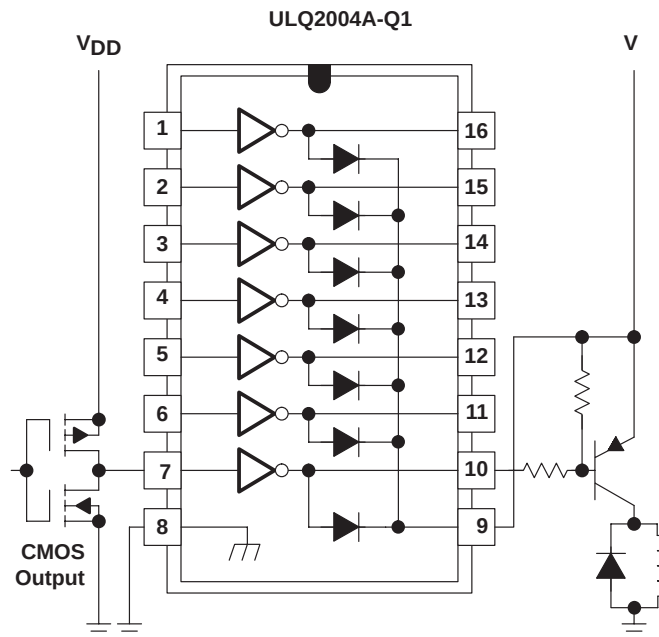


Figure 16. Buffer for Higher Current Loads

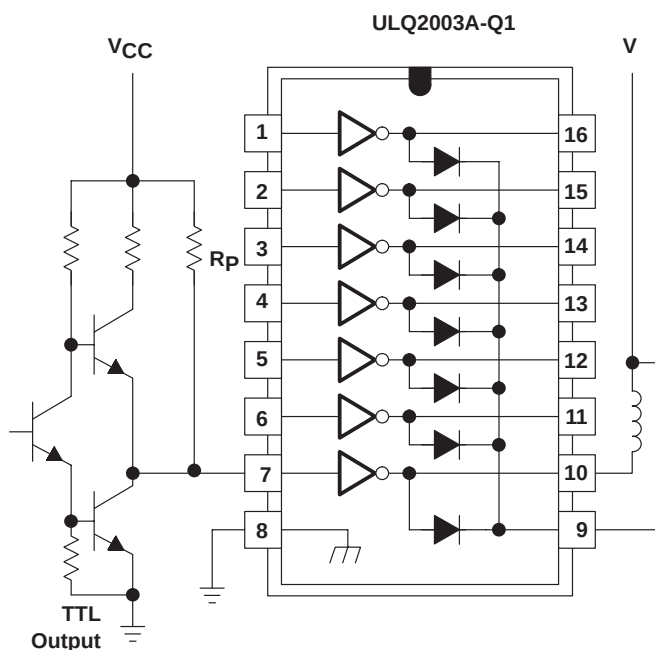


Figure 17. Use of Pullup Resistors
to Increase Drive Current

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ULQ2003ATDQ1	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2003ATDRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2004ATDRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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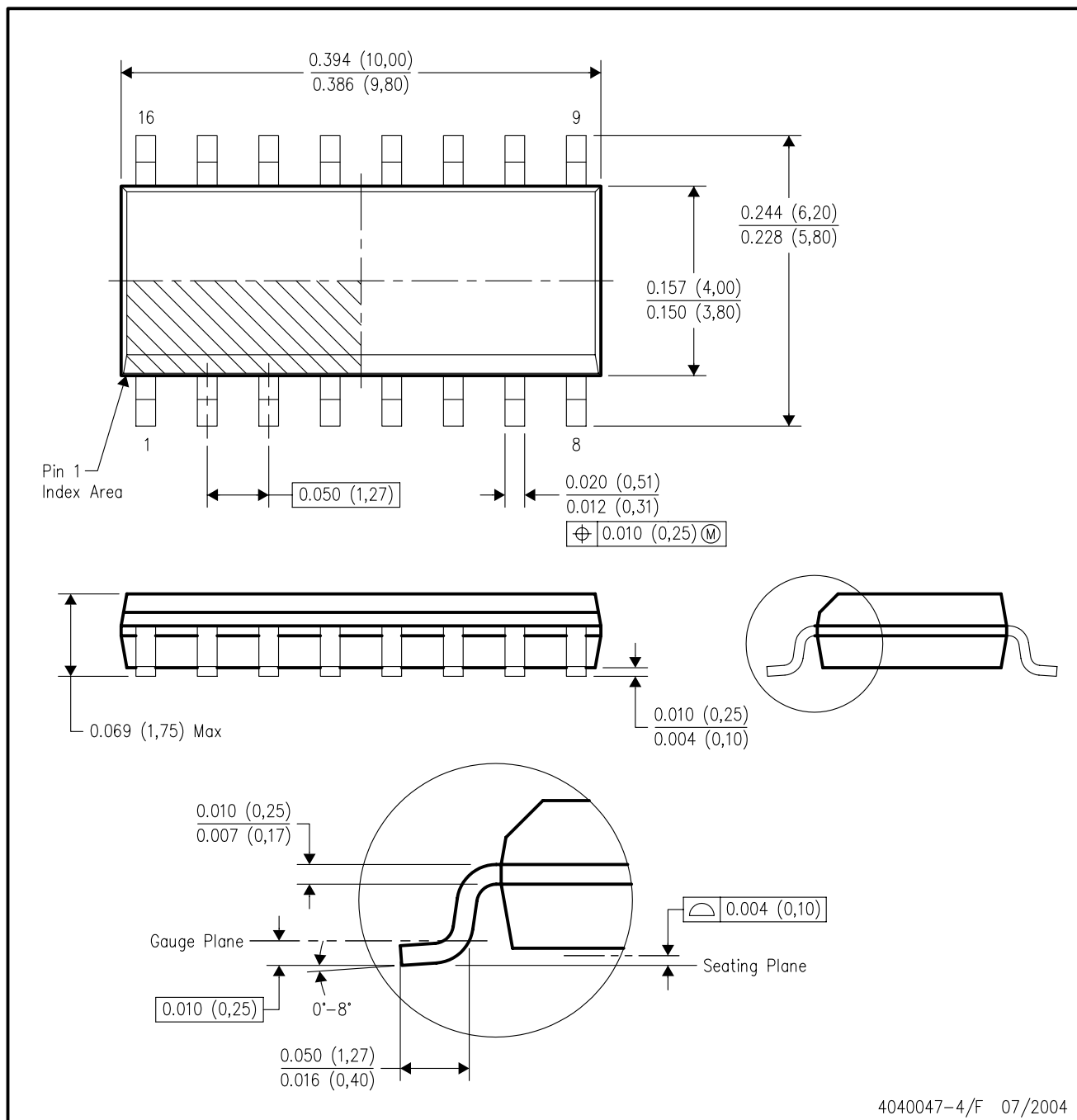
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-012 variation AC.

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