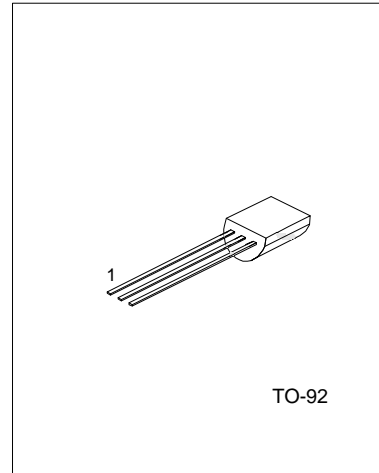


DESCRIPTION

The UTC BT169 is glass passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.



1:CATHODE 2:GATE 3:ANODE

QUICK REFERENCE DATA

| PARAMETER | SYMBOL | MAX(B) | MAX(D) | MAX(E) | MAX(G) | UNIT |
|--------------------------------------|-------------------------------------|--------|--------|--------|--------|------|
| Repetitive peak off-state voltages | V _{DRM} , V _{RRM} | 200 | 400 | 500 | 600 | V |
| Average on-state current | I _{T(AV)} | 0.5 | 0.5 | 0.5 | 0.5 | A |
| RMS on-state current | I _{T(RMS)} | 0.8 | 0.8 | 0.8 | 0.8 | A |
| Non-repetitive peak on-state current | I _{TSM} | 8 | 8 | 8 | 8 | A |

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNIT |
|--|-------------------------------------|--|-----|----------------------------------|------------------|
| Repetitive peak off-state voltages : | V _{DRM} , V _{RRM} | | | B:200 D:400 E:500 G:600 | V |
| Average on-state current | I _{T(AV)} | Half sine wave; T _{lead} ≤ 83°C | | 0.5 | A |
| RMS on-state current | I _{T(RMS)} | All conduction angles | | 0.8 | A |
| Non-repetitive peak on-state current | I _{TSM} | t = 10ms t = 8.3ms half sine wave; T _j = 25°C prior to surge | | 8 9 | A |
| I ² t for fusing | I ² t | t = 10ms | | 0.32 | A ² S |
| Repetitive rate of rise of on-state current after triggering | DI _T /dt | I _{TM} = 2A; I _G = 10mA; di _G /dt = 100mA/μs | | 50 | A/μs |
| Peak gate current | I _{GM} | | | 1 | A |
| Peak gate voltage | V _{GM} | | | 5 | V |
| Peak reverse gate voltage | V _{RGM} | | | 5 | V |

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNIT |
|--------------------------------|--------|-----------------------|-----|-----|------|
| Peak gate power | PGM | | | 2 | W |
| Average gate power | PG(AV) | Over any 20 ms period | | 0.1 | W |
| Storage temperature | Tstg | | -40 | 150 | °C |
| Operating junction temperature | Tj | | | 125 | °C |

THERMAL RESISTANCES

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------------|---------------------------------|-----|-----|-----|------|
| Thermal resistance junction to lead | Rth j-lead | | | | 60 | K/W |
| Thermal resistance junction to ambient | Rth j-a | pcb mounted; lead length=4mm | | 150 | | K/W |

ELECTRICAL CHARACTERISTICS (Tj=25°C unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------------------|--|-----|------|------|------|
| STATIC | | | | | | |
| Gate trigger current | IGT | V _D =12V; I _T =10mA; gate open circuit | | 50 | 200 | μA |
| Latching current | IL | V _D =12V; I _{GT} =0.5mA; R _{GK} =1kΩ | | 2 | 6 | mA |
| Holding current | IH | V _D =12V; I _{GT} =0.5mA; R _{GK} =1kΩ | | 2 | 5 | mA |
| On-state voltage | V _T | I _T =1A | | 1.2 | 1.35 | V |
| Gate trigger voltage | V _{GT} | V _D =12V; I _T =10mA; gate open circuit | | 0.5 | 0.8 | V |
| | | V _D =V _{DRM(max)} ; I _T =10mA; T _j =125°C; gate open circuit | 0.2 | 0.3 | | |
| Off-state leakage current | I _D , I _R | V _D =V _{DRM(max)} ; V _R =V _{R_{RRM(max)}} ; T _j =125°C; R _{GK} =1kΩ | | 0.05 | 0.1 | mA |
| DYNAMIC | | | | | | |
| Critical rate of rise of off-state voltage | dV _D /dt | V _{DM} =67% V _{DRM(max)} ; T _j =125°C; exponential waveform; R _{GK} =1kΩ | | 25 | | V/μs |
| Gate controlled turn-on time | t _{gt} | I _{TM} =2A; V _D =V _{DRM(max)} ; I _G =10mA; dI _G /dt=0.1A/μs | | 2 | | μs |
| Circuit commutated turn-off time | t _q | V _D =67% V _{DRM(max)} ; T _j =125°C; I _{TM} =1.6A; V _R =35V; dI _{TM} /dt=30A/μs; V _D /dt=2V/μs; R _{GK} =1kΩ | | 100 | | μs |

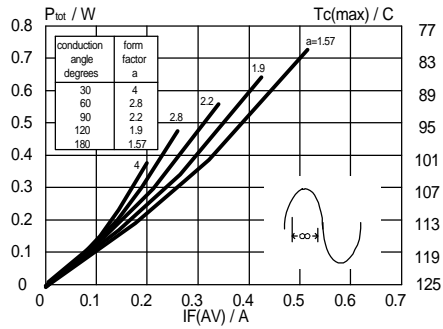


FIG.1 Maximum on-state dissipation, P_{tot} , versus average on-state current, $I_{T(AV)}$, where $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$

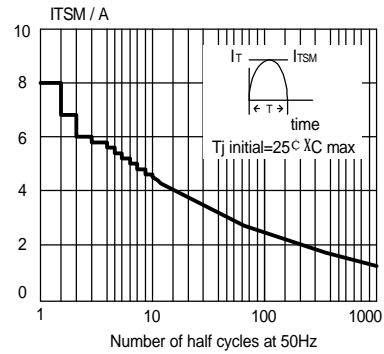


FIG.4 Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50\text{Hz}$.

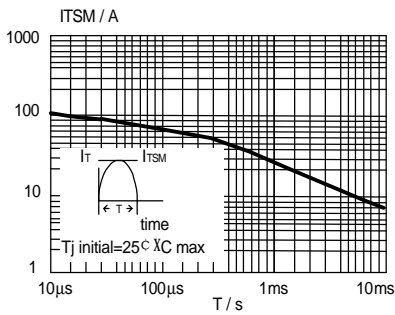


FIG.2 Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 10\text{ms}$.

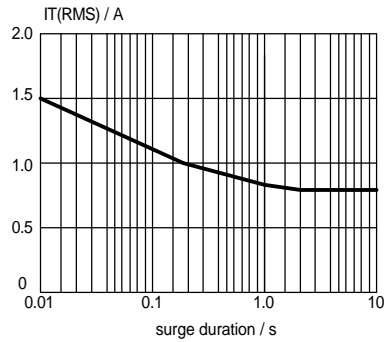


FIG.5 Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50\text{Hz}$; $T_{lead} \leq 83^\circ\text{C}$

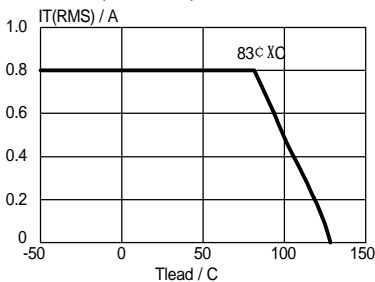


FIG.3 Maximum permissible rms current $I_{T(RMS)}$, versus lead temperature, T_{lead}

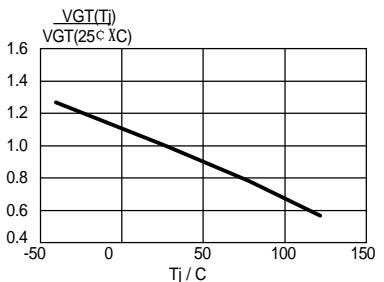


FIG.6 Normalised gate trigger voltage $V_{GT(Tj)} / V_{GT(25^\circ\text{C})}$, versus junction temperature T_j

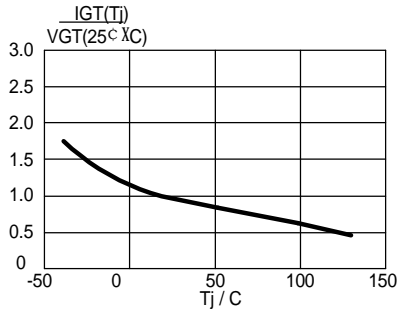


FIG.7 Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j

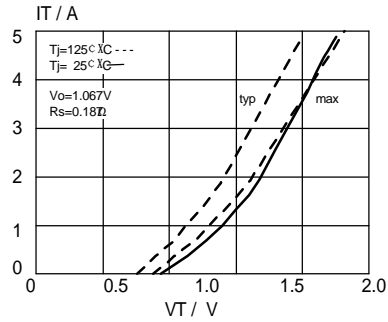


FIG.10 Typical and maximum on-state characteristic.

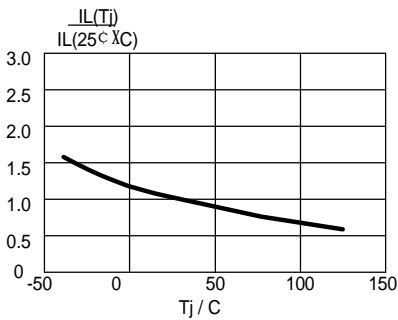


FIG.8 Normalised latching current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j , $R_{GK} = 1\text{K}\Omega$

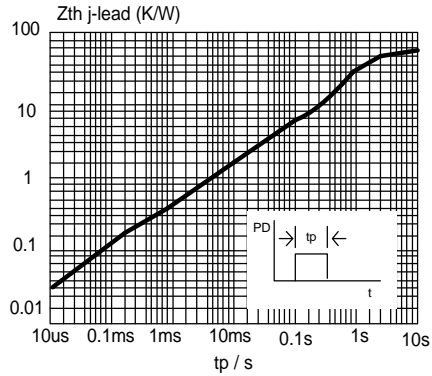


FIG.11 Transient thermal impedance $Z_{th \text{ j-lead}}$, versus pulse width t_p .

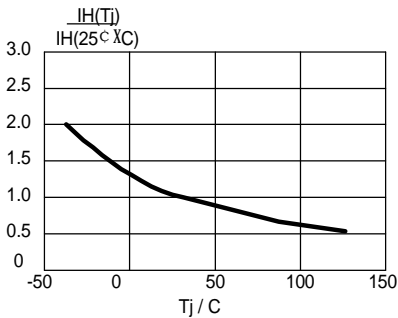


FIG.9 Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j , $R_{GK} = 1\text{K}\Omega$

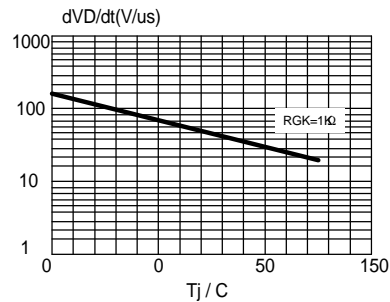


FIG.12 Typical, critical rate of rise of off-state voltage, dV/dt versus junction temperature T_j .