UMC

T-75-37-07

UM2661

Enhanced Programmable Communications Interface (EPCI)

Features

Synchronous Operation

- 5 to 8-bit characters plus parity
- Single or double SYN operation
- Internal or external character synchronization
- Transparent or non-transparent mode
- Transparent mode DLE stuffing (Tx) and detection (Rx)
- Automatic SYN or DLE-SYN insertion
- SYN, DLE and DLE-SYN stripping
- Odd, even, or no parity
- Local or remote maintenance loop back mode
- Baud rate: DC to 1M bps (1X clock)

Asynchronous Operation

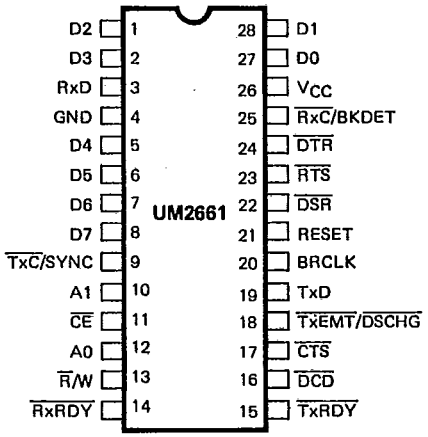
- 5 to 8-bit characters plus parity
- 1, 1½ or 2 stop bits transmitted
- Odd, even, or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loop back mode
- Baud rate: DC to 1M bps (1X clock)
  - DC to 62.5K bps (16X clock)
  - DC to 15.625K bps (64X clock)

Other Features

- Internal or external baud rate clock
- 3 baud rate sets UM2661–1, –2, –3
- 16 internal rates for each set
- Double buffered transmitter and receiver
- Dynamic character length switching
- Full or half duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short circuit protected
- 3 open drain MOS outputs can be wire-ORed
- Single 5V power supply
- No system clock required

I/O And Peripherals

Pin Configuration



Block Diagram

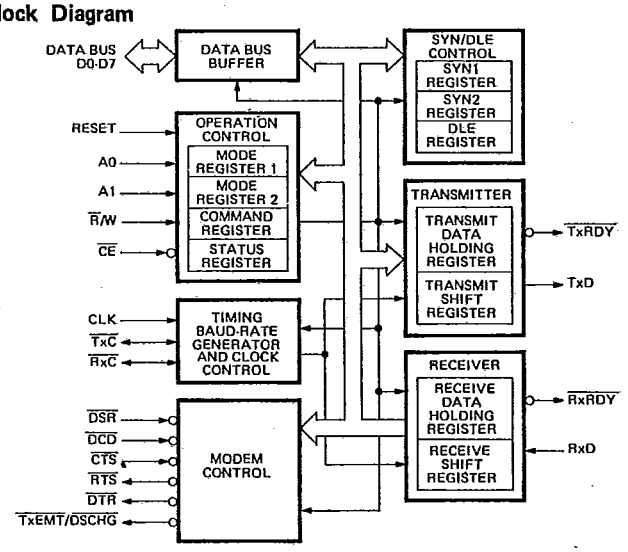


Figure 1. Internal Block Diagram

Absolute Maximum Ratings *

Supply Voltage V_{CC} . . . . . −0.3V to +7.0V
Input/Output Voltage V_{IN} . . . . . −0.3V to +7.0V
Operating Temperature T_{OP} . . . . . 0°C to 70°C
Storage Temperature T_{STG} . . . . . −55°C to 150°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

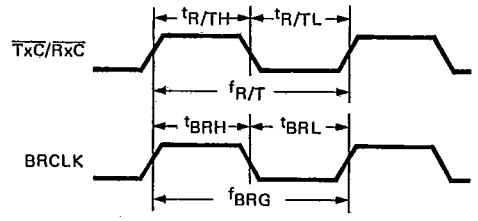
D.C. Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)

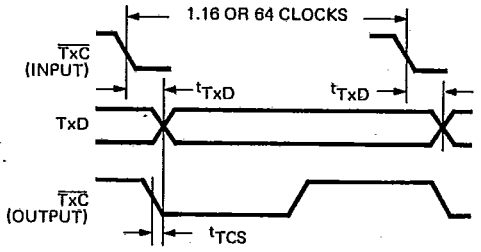
Characteristics	Symbol	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0.8	V
Input Leakage Current V_{IN} = 0 to 5.5V	I_{IN}			10	μA
Input Leakage Current for High Impedance State	I_{TSI}			10	μA
Output High Voltage: I_{LOAD} = −400μA	V_{OH}	2.4			V
Output Low Voltage: I_{LOAD} = 2.2 mA	V_{OL}			0.4	V
Input Capacitance: f_c = 1 MHz	C_{IN}			20	pF
Output Capacitance	C_{OUT}			20	pF
Power Dissipation (V_{CC} = 5.25V)	P_D			650	mW

Receiver/Transmitter Signal Timing

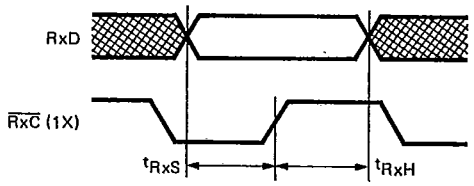
CLOCKS



TRANSMIT TIMING



RECEIVER TIMING

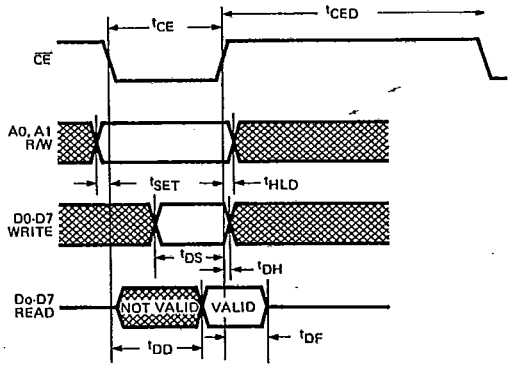


Symbol	Characteristics	Min.	Typ.	Max.	Units
$t_{R/TH}$	TxC or RxC HIGH	500			ns
$t_{R/TL}$	TxC or RxC LOW	500		1.0	ns
$f_{R/T}$	TxC or RxC freq.	DC		1.0	MHz
t_{BRH}	BRCLK HIGH	70			ns
t_{BRL}	BRCLK LOW	70			ns
f_{BRG}	BRCLK freq. (1)		4.9152		MHz
t_{RxS}	RxD SETUP	300			ns
t_{RxH}	RxD HOLD	350			ns
t_{TxD}	TxD DELAY FROM TxC C_L = 150 pF			650	ns
t_{TCS}	SKEW TxD vs TxC C_L = 150 pF		0		ns

Note: f_{BRG} = 4.9152 applicable for -1 and -2, f_{BRG} = 5.0688 for -3.

Read/Write Timing Characteristics

(V_{CC} = 5.0V ± 5%, T_A = 0-70°C, unless otherwise noted)



Symbol	Characteristics	Min.	Max.	Unit
t_{CE}	$\overline{CE}$ Pulse Width	250		ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ Delay	600		ns
t_{SET}	Address and R/W Set Up	10		ns
t_{HLD}	Address and $\overline{R}/W$ Hold	10		ns
t_{DS}	Write Data Set Up	150		ns
t_{DH}	Write Data Hold	0		ns
t_{DD}	Read Data Delay C_L = 150 pF		200	ns
t_{DF}	READ DATA HOLD C_L = 150 pF	10	100	ns

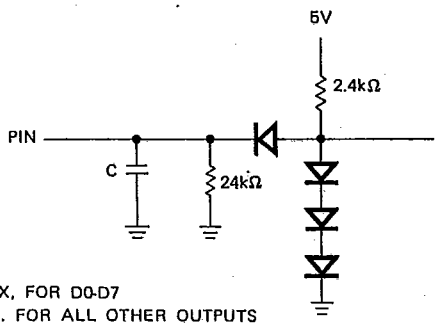
Table 1. Effect of MR17 and MR16 on Character Fill and Character Stripping (Synchronous Mode)

MR17	MR16	Mode	Synchronizing Sequence	Character Fill	Character(s) Stripped CR7=0, CR6=1
0	0	Double SYN Normal	SYN1-SYN2	SYN1-SYN2	SYN1 SYN1-SYN2(1)
1	0	Single SYN Normal	SYN1	SYN1	SYN1(1)
0	1	Double SYN Transparent	SYN1-SYN2	DLE-SYN1	DLE-SYN1(1) SYN1-SYN2(1) (Only Initial Synchronizing Sequence) DLE (also Sets SR3 it is Parity Disabled and not Following a DLE or SYN1) In a DLE-DLE Sequence Only the First DLE is Stripped
1	1	Single SYN Transparent	SYN1	DLE-SYN1	DLE-SYN1(1) SYN1 (only Initial Synchronizing Sequence) DLE and DLE-DLE same as Double SYN Transparent

Note: Symbol indicates SYN DET status set upon detection of initial synchronizing characters and after SYNC has been achieved by detection of DLE-SYN1 pair.

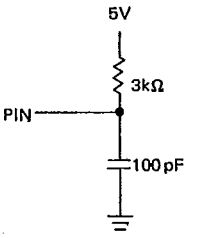
I/O And Peripherals

Test Load



C = 130 pF MAX. FOR D0-D7
C = 30 pF MAX. FOR ALL OTHER OUTPUTS

OPEN COLLECTOR OUTPUT TEST LOAD



Timing Waveforms

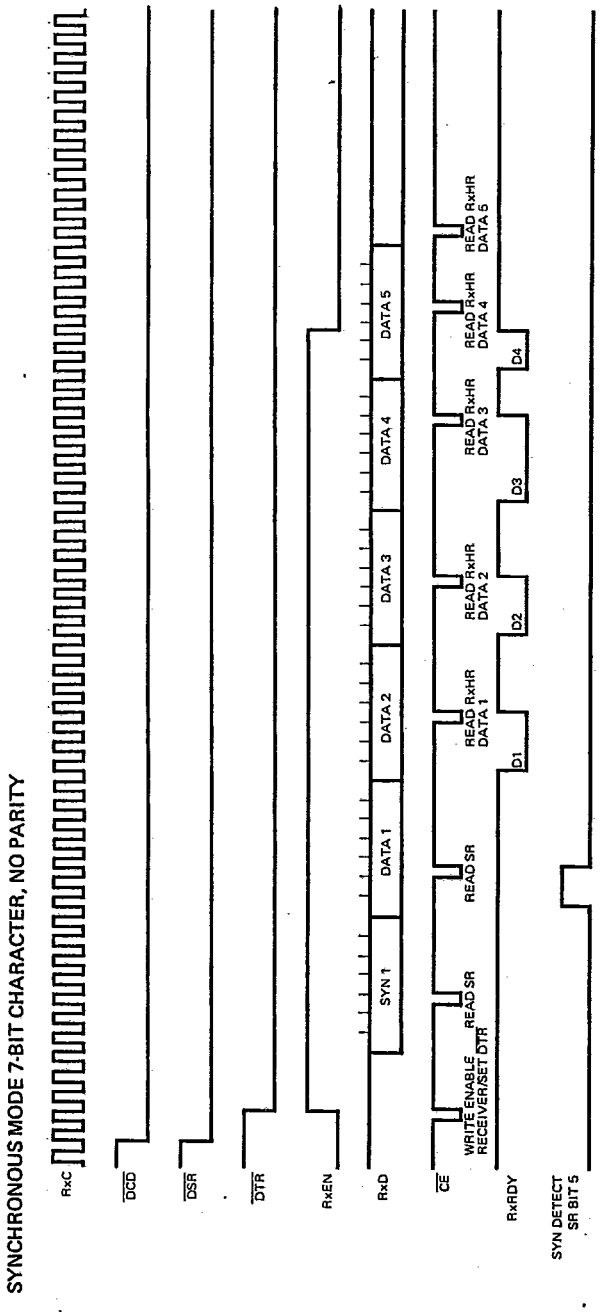


Figure 2. Receiver Operation Timing Diagram

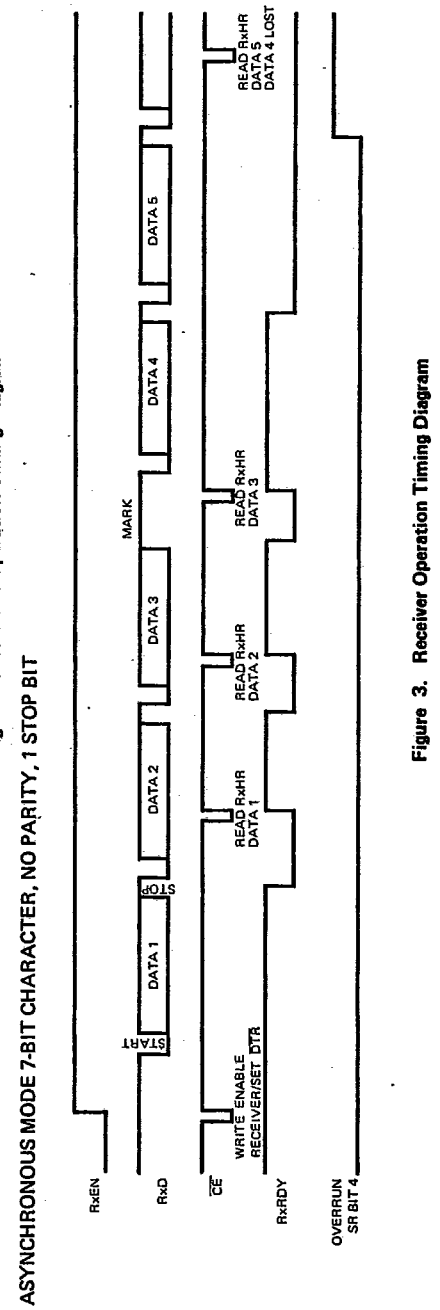


Figure 3. Receiver Operation Timing Diagram

Timing Waveforms (Continued)

SYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY

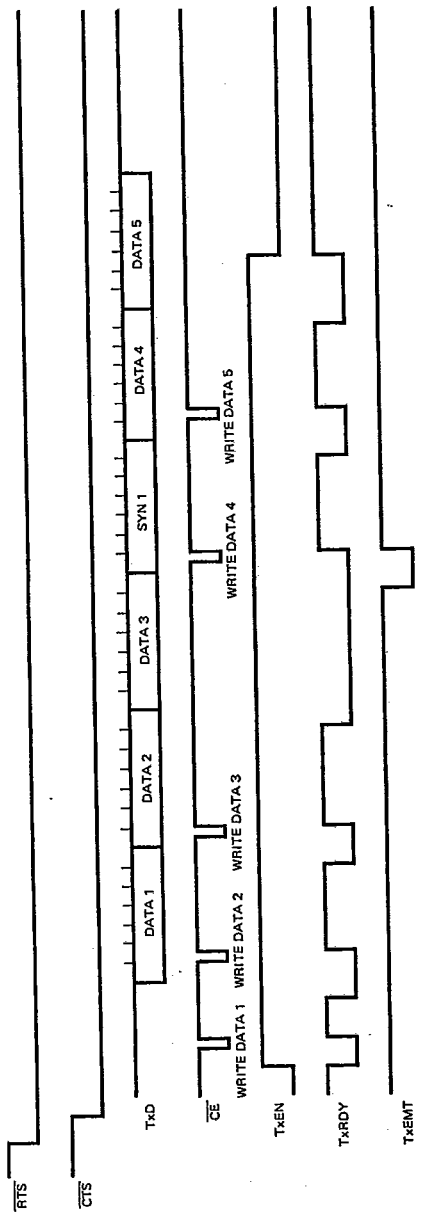


Figure 4. Transmitter Operation Timing Diagram

ASYNCHRONOUS MODE 7-BIT CHARACTER, NO PARITY, 1 STOP BIT

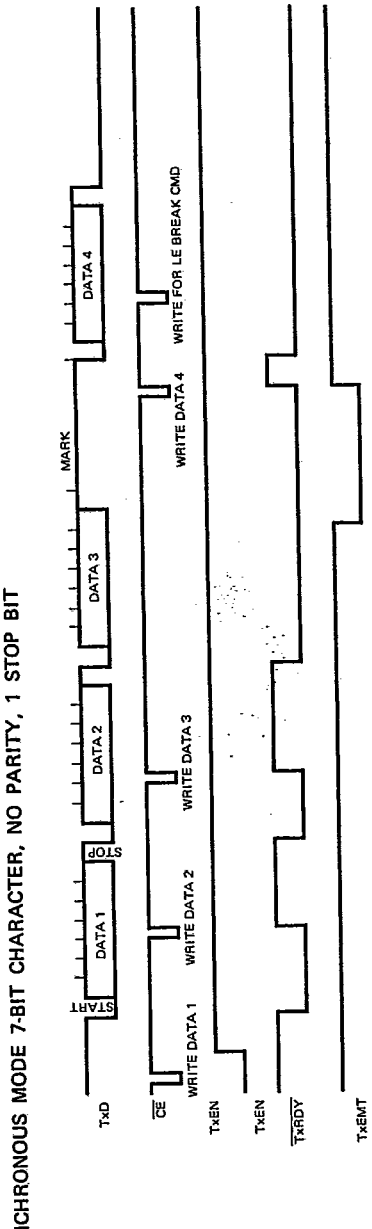


Figure 5. Transmitter Operation Timing Diagram

I/O And Peripherals

Timing Waveforms (Continued)

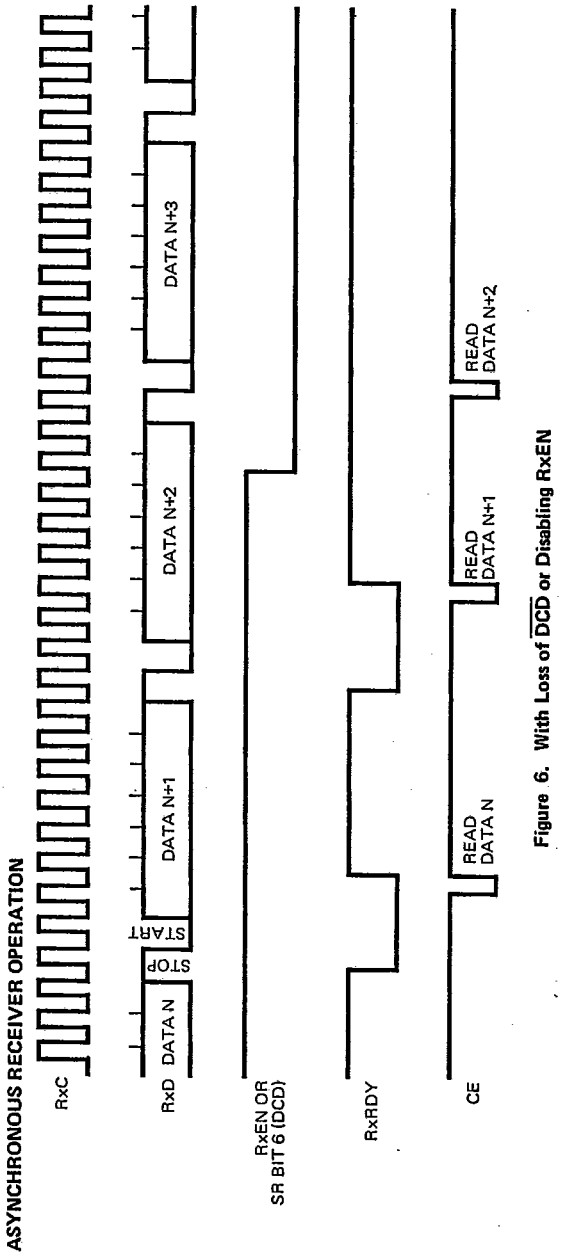


Figure 6. With Loss of $\overline{DCD}$ or Disabling RxEN

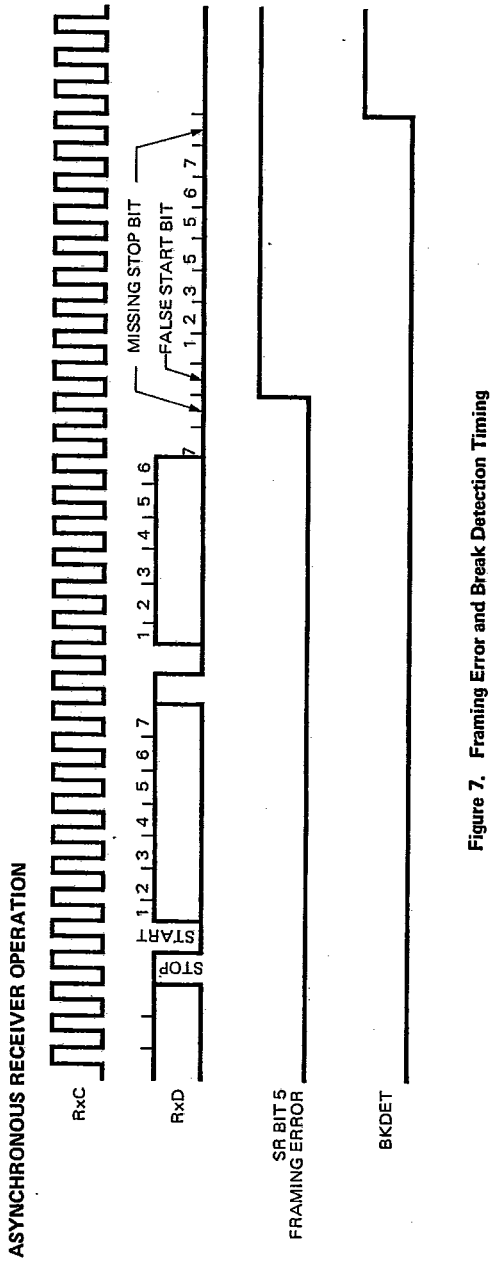


Figure 7. Framing Error and Break Detection Timing

Table 2. Baud Rate Generator Characteristics

UM2661-1 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	–	6144
0	0	0	1	75	1.2	–	4096
0	0	1	0	110	1.7598	–0.01	2793
0	0	1	1	134.5	2.152	–	2284
0	1	0	0	150	2.4	–	2048
0	1	0	1	200	3.2	–	1536
0	1	1	0	300	4.8	–	1024
0	1	1	1	600	9.6	–	512
1	0	0	0	1050	16.8329	0.196	292
1	0	0	1	1200	19.2	–	256
1	0	1	0	1800	28.7438	–0.19	171
1	0	1	1	2000	31.9168	–0.26	154
1	1	0	0	2400	38.4	–	128
1	1	0	1	4800	76.8	–	64
1	1	1	0	9600	153.6	–	32
1	1	1	1	19200	307.2	–	16

UM2661-2 (BRCLK = 4.9152 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	45.5	0.7279	0.005	6752
0	0	0	1	50	0.8	–	6144
0	0	1	0	75	1.2	–	4096
0	0	1	1	110	1.7598	–0.01	2793
0	1	0	0	134.5	2.152	–	2284
0	1	0	1	150	2.4	–	2048
0	1	1	0	300	4.8	–	1024
0	1	1	1	600	9.6	–	512
1	0	0	0	1200	19.2	–	256
1	0	0	1	1800	28.7438	–0.19	171
1	0	1	0	2000	31.9168	–0.26	154
1	0	1	1	2400	38.4	–	128
1	1	0	0	4800	76.8	–	64
1	1	0	1	9600	153.6	–	32
1	1	1	0	19200	307.2	–	16
1	1	1	1	38400	614.4	–	8

UM2661-3 (BRCLK = 5.0688 MHz)

MR 2				Baud Rate	Actual Frequency 16X Clock (KHz)	Percent Error	Divisor
3	2	1	0				
0	0	0	0	50	0.8	–	6336
0	0	0	1	75	1.2	–	4224
0	0	1	0	110	1.76	–	2880
0	0	1	1	134.5	2.1523	0.016	2355
0	1	0	0	150	2.4	–	2112
0	1	0	1	300	4.8	–	1056
0	1	1	0	600	9.6	–	528
0	1	1	1	1200	19.2	–	264
1	0	0	0	1800	28.8	–	176
1	0	0	1	2000	32.081	0.253	158
1	0	1	0	2400	38.4	–	132
1	0	1	1	3600	57.6	–	88
1	1	0	0	4800	76.8	–	66
1	1	0	1	7200	115.2	–	44
1	1	1	0	9600	153.6	–	33
1	1	1	1	19200	316.8	3.126	16

Note: 16X CLK is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for T x C

Signal Descriptions

CPU Interface

Reset (Reset)
A high on this input performs a master reset on the UM2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.

A0, A1 (Address 0, 1)
Address lines used to select the internal registers.

$\overline{R}$/W (Read/Write)
The direction of data transfers between the EPCI and the CPU is controlled by the R/W input. When CE and $\overline{R}$/W are both low the contents of the selected registers will be transferred to the data bus. With CE low and $\overline{R}$/W high a write to the selected register is performed.

$\overline{CE}$ (Chip Enable)
When low, the selected register will be accessed. When high the D0-D7 lines will be placed in the high impedance state.

D0-D7 (Data Bus)
An 8-bit three-state positive true data bus used to transfer commands, data and status between the EPCI and the CPU.

$\overline{TxRDY}$ (Transmitter Ready)
This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (TxHR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt.

$\overline{RxRDY}$ (Receiver Ready)
This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RxHR) has a character ready for input to the CPU. It goes high when the RxHR is read by the CPU and also when the receiver is disabled. It is an open drain output which can be "wire-ORed" to the CPU interrupt line.

$\overline{TxEMT/DSCHG}$
This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the DSR or DCD inputs has occurred. This output goes high when the status register is read by the CPU if the TxEMT condition does not exist. Otherwise, the TxHR must be loaded by the CPU for this line to go high. It is an open drain output which can be "wire OR-ed" to the CPU interrupt line.

Transmitter/Receiver Signals

BRCLK (Baud Rate Clock)
Clock input to the internal baud rate generator. This is not required when external receiver and transmitter clocks are used.

$\overline{RxC}$/BKDET (Receiver Clock, Break Detect)
When the EPCI is programmed for External Receiver Clock, this pin will act as an input and control the rate at which a character is received. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data are sampled on the rising edge. If internal Receiver Clock is programmed this pin will provide an output, either a 1X/16X clock or Break Detect signal determined by programming Mode Register 2.

$\overline{TxC}$/XSYNC (Transmitter Clock/External SYNC)
When the EPCI is programmed for External Transmitter clock, this pin will act as an input and control the rate at which the character is transmitted. The frequency is programmed in Mode Register 1 and may be 1X, 16X or 64X the baud rate. Data changes on the falling edge of this clock. If the UPCI is programmed for Internal Transmitter clock, this pin can be either an output providing a 1X/16X clock or an input for External Synchronization determined by Mode Register 2 programming.

RxD (Receive Data)
RxD is the serial data input to the receiver.

TxD (Transmit Data)
TxD is the serial data output from the transmitter. When the transmitter is disabled the output will be in the high, "Mark", state.

$\overline{DSR}$ (Data Set Ready)
$\overline{DSR}$ is an input that can be used to indicate to the UPCI Data Set Ready or Ring Indicator. Its complement appears in the Status Register as bit SR7. A change of state on $\overline{DSR}$ will cause $\overline{TxEMT/DSCHG}$ to go low if either CR0 or CR2=1.

$\overline{DCD}$ (Data Carrier Detect)
The $\overline{DCD}$ input must be low for the receiver to operate. If DCD goes high while receiving, the RxC is internally inhibited. The complement of $\overline{DCD}$ appears in the Status Register as bit SR6. A change of state in $\overline{DCD}$ will cause $\overline{TxEMT/DSCHG}$ to go low if either CR0 or CR2=1.

$\overline{CTS}$ (Clear To Send)
The $\overline{CTS}$ input must be low for the transmitter to operate. If $\overline{CTS}$ goes high while transmitting, the character currently in the Transmit Shift Register will be transmitted before termination, TxD will then go to the high level (Mark).

$\overline{DTR}$ (Data Terminal Ready)
The $\overline{DTR}$ output is the complement of CR1. It is normally used to indicate Data Terminal Ready.

$\overline{RTS}$ (Request To Send)
The $\overline{RTS}$ output is the complement of CR5. If the Transmit Shift Register is not empty when CR5 is reset, $\overline{RTS}$ will not go high until one TxC after the last serial bit is transmitted.

Functional Description

The internal organization of the EPCI consists of six major blocks, (see Fig. 1). These are the Transmitter, Receiver, Clock Control, Operation Control, Modem Control and SYN/DLE Control. These blocks internally communicate over common data and control buses. The data bus is also linked to the CPU via a bi-directional three-state interface. Briefly, these blocks perform the following functions:

Transmitter
The Transmitter receives parallel data from the CPU and converts it to a serial bit stream, inserting Start, Stop, and Parity bits, as selected by the user, and outputs a composite serial data stream.

Receiver
The Receiver accepts serial data from the sending device, converts it to parallel format checking for appropriate Start, Stop and Parity bits and Control Characters, as selected by the user, and sends the assembled character to the CPU.

Timing Control
The Timing Control block contains a programmable Baud Rate Generator (BRG) which is able to accept external Transmit ($\overline{TxC}$) or Receiver ($\overline{RxC}$) clocks or to divide external clock (BRCLK) for controlling data transfers. The BRCLK input allows the user to program one of 16 commonly used baud rates.

Operating Control
The Operation Control block contains four registers; Mode Registers 1 and 2, (MR1, MR2) the Command Register (CR) and Status Register (SR). These registers are used to store configuration and operation commands from the CPU. They generate the necessary internal control signals for proper device operation, and maintain status information for the CPU.

Modem Control
The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control
This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Operational Description

The EPCI's operation is determined by programming the Mode and Command Registers. Baud rate, asynchronous or synchronous communication, and SYN characters are determined before enabling the transmitter or receiver.

Asynchronous Receiver Operation
After the Mode Registers are configured the receiver is enabled when the RxEN bit in the Command Register (CR2) is set to a 1 and $\overline{DCD}$ is low. The EPCI then monitors the RxD input waiting for a high to low transition. If a transition is detected, the RxD input is again sampled one-half bit time later. If RxD is now high, a search for a valid start bit is begun again. If RxD is still low a valid start bit is assumed and the receiver continues to sample the RxD input at one bit time intervals until the correct number of data bits, parity bit and one stop bit have been assembled. The character is then transferred to the Receive Data Holding Register (RxHR); RxRDY in the status Register is set (SR1); the $\overline{RxRDY}$ output goes low. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundry. See Figures 3 and 6.

If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit) only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins. See Figure 7.

Pin 25 can be programmed as a Break Detect (BKDET) output by setting both bits 4 and 7 of Mode Register 2 (MR2). When these bits are set and a break is detected, the BKDET output will go high. If RxD returns high for at least one RxD time, BKDET will return low.

Synchronous Receiver Operation
When the EPCI is programmed for synchronous operation, the receiver will remain idle until the receiver enable bit

(CR2) is set. At this time the EPCI enters the hunt mode. Data are shifted into the receive data shift register (RxSR) one bit at a time. The contents of RxSR are then compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). See Figure 2.

When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the $\overline{\text{RxRDY}}$ status bit and asserting the $\overline{\text{RxRDY}}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note: the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

By setting MR24 (MR2 bit 4) and MR27=1 pin 9 ($\overline{\text{RxC}}$/SYNC) will be programmed as an external jam synchronization input. When XSYNC is selected internal SYN1, SYN1-SYN2 and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC must be lowered prior to the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Asynchronous Transmitter Operation

When the EPCI is programmed to transmit, the transmitter will remain idle until $\overline{\text{CTS}}$ is low and the TxEN bit (CR0) is set. The EPCI will respond by setting status register (SR) bit 0 and asserting the $\overline{\text{TxRDY}}$ output. When the CPU writes a character into the transmit data holding register (TxHR), SR0 is reset and $\overline{\text{TxRDY}}$ returns high. The character is then transferred to the transmit shift register (TxSR) when it is idle or has completed transmission of the previous character. SR0 is again set, and $\overline{\text{TxRDY}}$ goes low. See Figure 5.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting CR3.

Synchronous Transmitter Operation

When the ECPI is initially programmed for synchronous transmission it will remain in the idle state (RxD high) until TxEN is set. At this point TxD remains high, $\overline{\text{TxRDY}}$ will go low and both will stay in this state until the first character (usually a SYN character) is written into the TxHR. This starts transmission, with $\overline{\text{TxRDY}}$ going low each time a character is shifted from the TxHR to the TxSR. If $\overline{\text{TxRDY}}$ is not serviced before the previous character is shifted out of the TxSR, the $\overline{\text{TxEMT}}$ output will go low and the EPCI will automatically fill the pending gap with SYN1, SYN1, SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR6 and MR17. Transmission will be continuous until TxFN is reset to 0. See Figure 4.

If the send DLE bit (CR3) is set, the DLE character is automatically transmitted prior to the transmission of any character stored in the TxHR. Since this is a one time command, CR3 does not have to be reset.

EPCI Programming

Before data communications can be started the EPCI must be programmed by writing to its mode and command registers. Additionally, if synchronous communication has been selected the appropriate SYN1, SYN2 and DLE registers must be loaded. Reference the Register Addressing Table and Initialization Flow Chart for address requirements and programming procedure.

The Register Addressing Table shows MR1 and MR2 at the same address. The EPCI has an internal pointer that initially directs that first read or write to MR1, then on the next access at the same address the pointer directs the operation to MR2. A similar sequence occurs for the SYN and DLE registers; first SYN1 then SYN2 then DLE. If more than the required number of accesses are made the internal pointer resets to the first register. The pointer is also reset to MR1 and SYN1 by a RESET input or a read of the Command Register, but unaffected by any other read or write operation.

Register Formats

The register formats are summarized in Figures 8 through11 MR1 and MR2 define the general operating characteristics. The Command Register controls the basic operation defined by MR1 and MR2. The Status Register indicates the EPCI operating status and the condition of external

inputs. These registers are cleared by a RESET input (SR6 and SR7 excepted).

Mode Register 1 (MR1)

MR11 and MR10 select the communication mode and baud rate multiplier. Note: the multiplier in asynchronous mode applies only if the external input option is selected by MR24 and RM25.

MR13 and MR12 select Character length. Character length does not include the parity bit, when selected, and does not include the start and stop bits in asynchronous operation.

MR14, when set, selects parity. A parity bit will be transmitted with each character, and a parity check will be performed on each character received.

MR15 selects either odd or even parity.

In the asynchronous mode MR16 and MR17 select the number of stop bits; 1, 1.5 or 2, If 1X baud rate is programmed 1.5 stop bits defaults to 1 on transmit.

In the synchronous mode MR17 controls the number of SYN characters used to establish synchronization, and the number of fill characters to be transmitted when $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are 0.

MR16 controls selection of the transparent mode. When MR16 is set (transparent selected) DLE-SYN1 is used for character fill and SYN detect (SR 5), but the normal synchronization sequence is used to establish character sync. When transmitting in the synchronous transparent mode, a DLE character in the TxHR will cause a second DLE character to be transmitted. Note: If the send DLE command (CR3) is active when a DLE character is in the TxHR, only one additional DLE will be transmitted.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half duplex mode (RxEN=1 or TxEN=1, but not both simultaneously=1). In asynchronous mode, character changes should be made when RxEN and TxEN=0, or when TxEN=1 and the transmitter is marking in half duplex mode (RxEN=0).

To effect assembly/disassembly of the next received/transmitted character, MR12–15 must be changed within n bit times of the active going state of $\overline{\text{RxDRY}}/\overline{\text{TxRDY}}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n = the smaller of the new and old character lengths.)

Mode Register 2 (MR2)

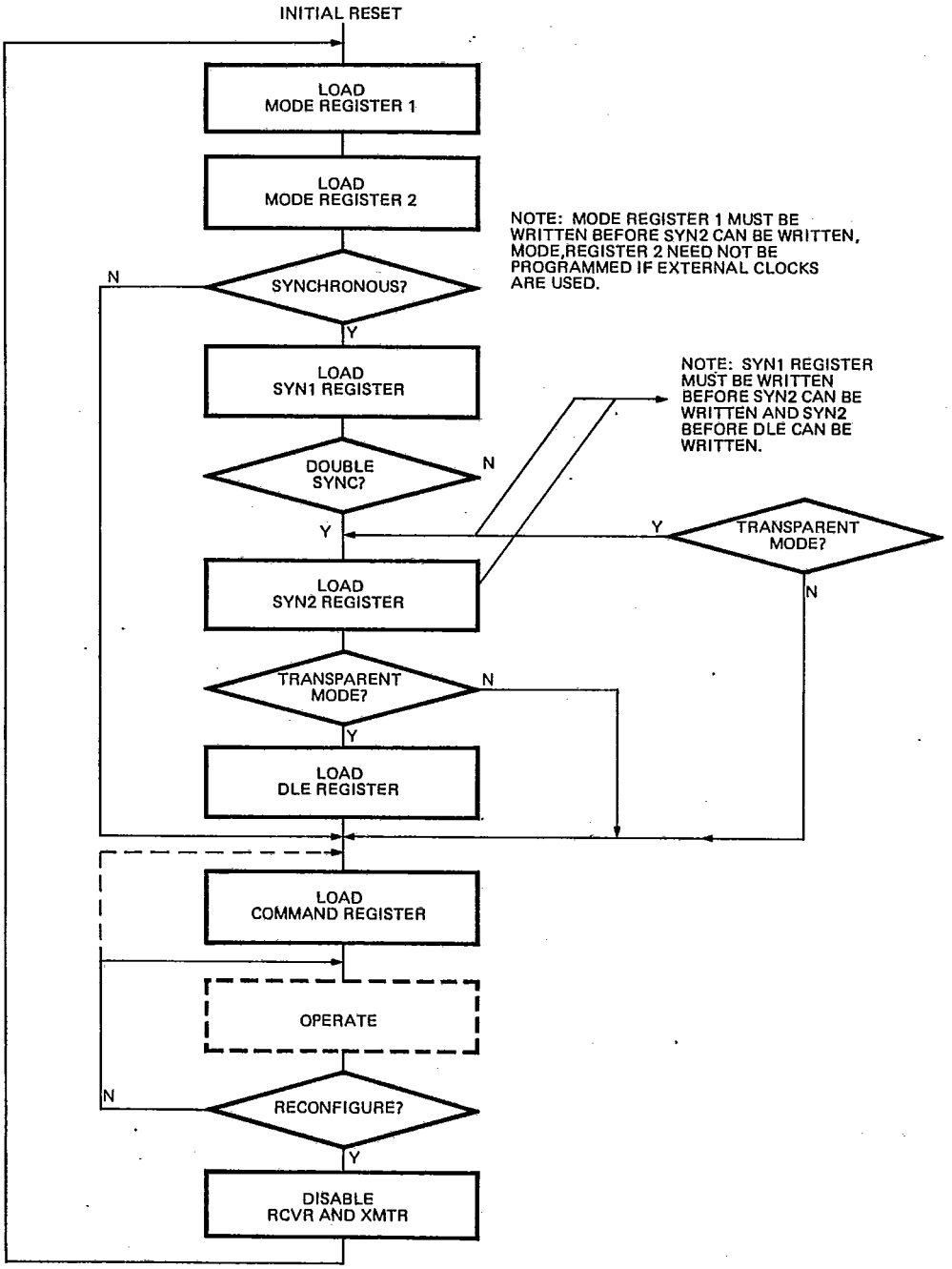
MR20 through MR23 select the internal Baud Rate Generator (BRG). There are sixteen selectable rates for each version as outlined in Table 2.

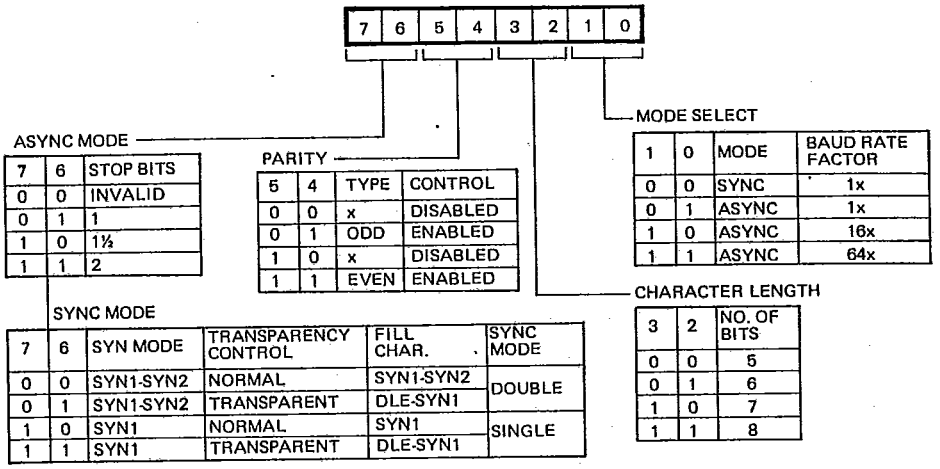
MR24 through MR27 define the receive and transmit clock source and the function of pins 9 and 25. Reference Figure 9.

Table 3. UM2661 Register Addressing

CE	A_1	A_0	$\overline{R/W}$	Functions
1	X	X	X	Three-state Data Bus
0	0	0	0	Read Receive Holding Register (RxHR)
0	0	0	1	Write Transmit Holding Register (TxHR)
0	0	1	0	Read Status Register (SR)
0	0	1	1	Write SYN1/SYN2/DLE Registers
0	1	0	0	Read Mode Registers (MR1, MR1/MR2)
0	1	0	1	Write Mode Registers (MR1, MR1/MR2)
0	1	1	0	Read Command Register
0	1	1	1	Write Command Register

EPCI Initialization Flow Chart





7	6	STOP BITS
0	0	INVALID
0	1	1
1	0	1½
1	1	2

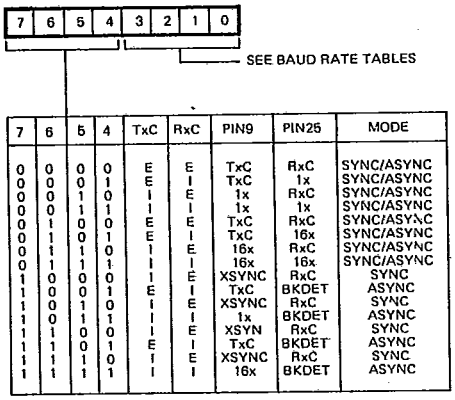
5	4	TYPE	CONTROL
0	0	x	DISABLED
0	1	ODD	ENABLED
1	0	x	DISABLED
1	1	EVEN	ENABLED

1	0	MODE	BAUD RATE FACTOR
0	0	SYNC	1x
0	1	ASYNC	1x
1	0	ASYNC	16x
1	1	ASYNC	64x

3	2	NO. OF BITS
0	0	5
0	1	6
1	0	7
1	1	8

7	6	SYN MODE	TRANSPARENCY CONTROL	FILL CHAR.	SYNC MODE
0	0	SYN1-SYN2	NORMAL	SYN1-SYN2	DOUBLE
0	1	SYN1-SYN2	TRANSPARENT	DLE-SYN1	
1	0	SYN1	NORMAL	SYN1	SINGLE
1	1	SYN1	TRANSPARENT	DLE-SYN1	

Figure 8. Mode Register 1



7	6	5	4	TxC	RxC	PIN9	PIN25	MODE
0	0	0	0	E	E	TxC	RxC	SYNC/ASYNC
0	0	0	1	I	I	TxC	1x	SYNC/ASYNC
0	0	1	0	E	E	1x	RxC	SYNC/ASYNC
0	0	1	1	I	I	1x	1x	SYNC/ASYNC
0	1	0	0	E	E	TxC	RxC	SYNC/ASYNC
0	1	0	1	I	I	TxC	16x	SYNC/ASYNC
0	1	1	0	E	E	16x	RxC	SYNC/ASYNC
0	1	1	1	I	I	16x	16x	SYNC/ASYNC
1	0	0	0	E	E	XSYNC	RxC	SYNC
1	0	0	1	I	I	TxC	BKDET	ASYNC
1	0	1	0	E	E	XSYNC	RxC	SYNC
1	0	1	1	I	I	1x	BKDET	ASYNC
1	1	0	0	E	E	XSYN	RxC	SYNC
1	1	0	1	I	I	TxC	BKDET	ASYNC
1	1	1	0	E	E	XSYNC	RxC	SYNC
1	1	1	1	I	I	16x	BKDET	ASYNC

Figure 9. Function of Pin 9 and Pin 25

Command Register (CR)

CR0 (TxEN) will enable or disable the transmitter. When TxEN=0, TxD, $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ are all high, the transmitter is disabled. When TxEN goes active, $\overline{\text{TxRDY}}$ will go low requesting the first character to be written to the TxHR, and the TxD output will be enabled to transmit. When TxEN goes inactive, the UPCI will complete transmission of any character still in the TxSR. TxD will then go to the marking state and $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ will go high. Refer to Transmit timing diagram.

CR1 controls the $\overline{\text{DTR}}$ output. The $\overline{\text{DTR}}$ output is a logical complement of CR1.

CR2 (RxEN) will enable or disable the receiver. When RxEN=0, the receiver is in an idle mode with $\overline{\text{RxRDY}}$ high. A 0 to 1 transition of RxEN will initiate a start bit search in asynchronous mode or initiate the hunt mode in synchronous transmission. A 1 to 0 transition of RxEN immediately terminates receiver operation.

In the asynchronous mode setting CR3 will force the TxD output low (break condition) at the end of the current transmitted character. TxD will then remain low until CR3 is cleared; at that time TxD will go high for a minimum 1 bit time before resuming normal transmission.

In the synchronous mode setting CR3 will force the transmission of the DLE character prior to sending the character in the TxHR. Because this is a one-time command, bit 3 will automatically reset.

CR5 controls the state of the $\overline{\text{RTS}}$ output. When CR5=1, $\overline{\text{RTS}}$ will go low and the transmit logic will be enabled. A 1 to 0 transition of CR5 will cause $\overline{\text{RTS}}$ to go high one TxC time after the last serial bit is transmitted, (if the TxSR was not already empty).

CR7 and CR6 provide four alternate modes of operation in both synchronous and asynchronous operation. When both bits are 0 normal operation is selected.

In the asynchronous mode, when only CR6 is set automatic echo mode is selected Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. CPU to receiver communications continue normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

I/O And Peripherals

1. Data assembled by the receiver is automatically placed in the transmit holding register and re-transmitted by the transmitter on the TxD output.
2. Transmit clock = receive clock.
3. $\overline{\text{TxRDY}}$ output = 1.
4. The $\overline{\text{TxEMT/DSCHG}}$ pin will reflect only the data set change condition.
5. The TxEN command (CRO) is ignored.

In the synchronous mode, when only the CR6 is set automatic SYN/DLE stripping is performed. The state of MR17 and MR16 controls which characters are stripped. Reference Figure 10 for a detailed example of the characters stripped.

Note: automatic stripping does not affect setting of the SYN and DLE detect status bits.

Two diagnostic modes are achievable in both synchronous and asynchronous operation; local loopback with CR7=1 and CR6=0, and remote loopback with both bits=1.

Local Loop Back

1. The transmitter output is connected to the receiver input.
2. $\overline{\text{DTR}}$ is connected to $\overline{\text{DCD}}$ and $\overline{\text{RTS}}$ is connected to $\overline{\text{CTS}}$.
3. Transmit clock is connected to the receive clock.
4. The $\overline{\text{DTR}}$, $\overline{\text{RTS}}$ and $\overline{\text{TxD}}$ outputs are held high.
5. The $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, $\overline{\text{DSR}}$ and $\overline{\text{RxD}}$ inputs are ignored.

Note: CR bits 0, 1 and 5 must be set, CR2 is a don't care.

Remote Loop Back

1. Data assembled by the receiver are automatically placed in the transmit holding register and re-transmitted by the transmitter on the TxD output.
2. Receive clock is connected to the transmit clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{\text{RxRDY}}$, $\overline{\text{TxRDY}}$, and $\overline{\text{TxEMT/DSCHG}}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

SRD is the transmitter ready ($\overline{\text{TxRDY}}$) status, it is the logical complement of the $\overline{\text{TxRDY}}$ output. This bit indicates the state of the TxHR when the transmitter is enabled (TxEN=1). A 0 indicates TxHR is full, a 1 indicates TxHR is empty and requires servicing by the CPU. This bit is cleared by writing to TxHR or by disabling the transmitter (TxEN=0). Note: SRO is not set in either the auto echo or remote loop back modes.

SR1 is the receiver ready (RxRDY) status. It is the logical complement of the $\overline{\text{RxRDY}}$ output. This bit indicates the state of the RxHR when the receiver is enabled (RxEN=1). A 0 indicates the RxHR is empty, a 1 indicates the RxHR is full and requires servicing by the CPU. This bit is cleared by writing to the TxHR or by disabling the receiver. (RxEN=0).

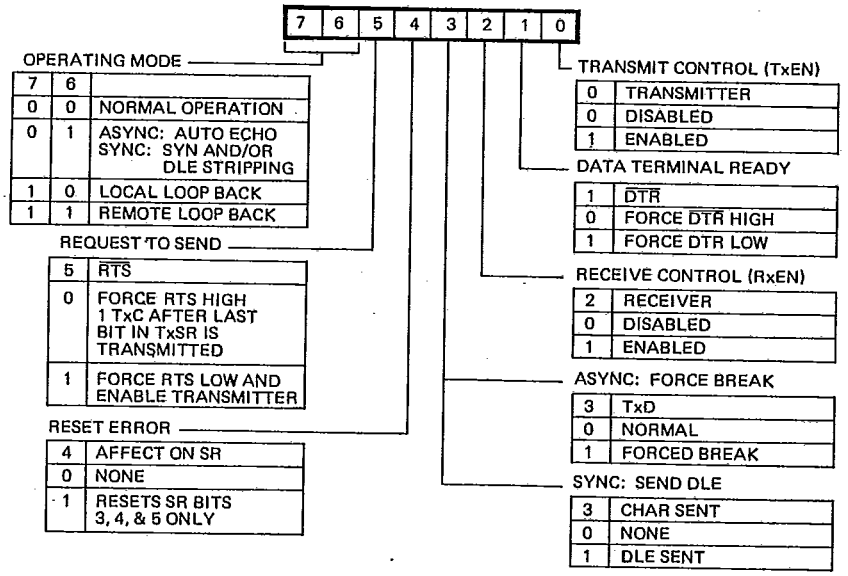


Figure 10. Command Register

SR2 indicates a change of state of either $\overline{DSR}$ or $\overline{DCD}$ or that the TxSR is empty. This bit is the logical complement of the $\overline{TxEMT/DSCHG}$ output. A reading of the status register will clear bit 2 if a state change on DSR or $\overline{DCD}$ has occurred. If a second successive read of the status register indicates bit 2=0, then $\overline{DCD}$ or $\overline{DSR}$ changes. If bit 2 is still set, then the TxSR is empty. Because the transmitter does not start until the first character has been written to the TxHR, $\overline{TxEMT}$ status will not be reflected until transmission of the first character is complete, $\overline{TxEMT}$ status is cleared by writing to the TxHR or disabling the transmitter. Note: $\overline{TxEMT}$ status will be set in synchronous mode even though "fill" characters are being transmitted.

SR3 when set reflects a parity error when parity checking is enabled in both the synchronous and asynchronous modes. In the synchronous transparent mode, (MR16=1) and the parity enable bit (MR14) is 0, SR3 will then indicate DLE detect when set. This indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the RxHR, when the receiver is disabled or by a reset error command.

SR4 indicates an overrun error when set. An overrun condition exists when the CPU does not read the RxHR before the next received character is transferred to it. (The previous character is lost.) SR4 is cleared by the reset error command and when the receiver is disabled.

In the asynchronous mode SR5 indicates that the received character was not framed by a stop bit. If the RxHR is all 0's when bit 5 is set, a break condition was present. In synchronous non-transparent mode, it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the condition of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. Their state is the logical complement of their respective inputs.

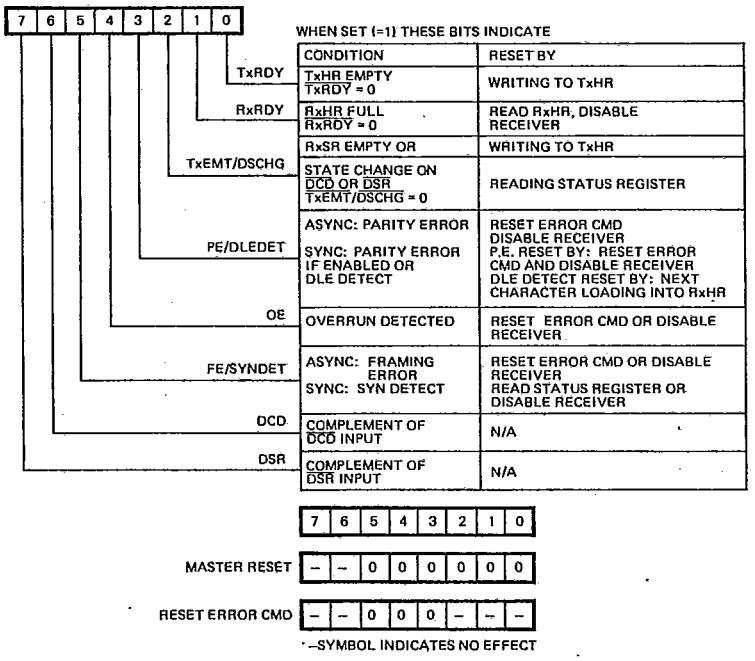


Figure 11. Status Register

Ordering Information

Part Number	BRCLK	Baud Rate
UM2661-1	4.9152 MHz	50 ~19200
UM2661-2	4.9152 MHz	45.5~38400
UM2661-3	5.0688 MHz	50 ~19200