UMC

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UM9151-3

Pulse Dialer

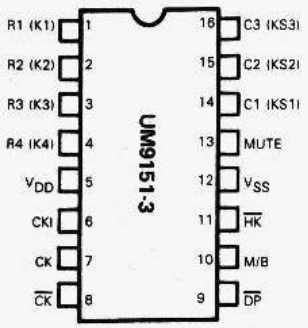
Features

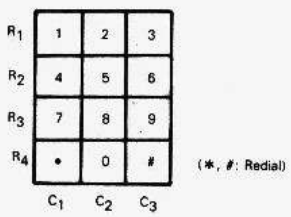
- Direct telephone line operation
- 4 x 3 matrix keyboard interface
- Supply voltage range of 2.0 to 5.5 volts
- Inexpensive RC oscillator
- Low power standby mode for redialing
- 22-digit redial memory
- Redial with either * or # key
- Dialer reset for line power breaks > 200 ms
- 800 ms inter-digit pause
- Selectable make/break ratio
- High speed test capacity

General Description

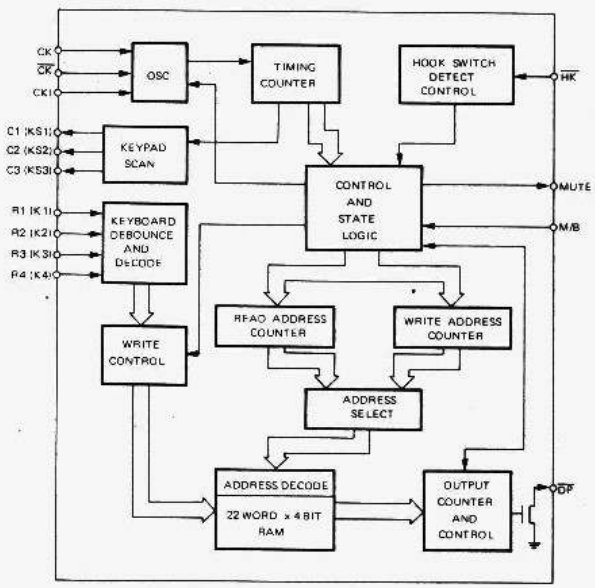
The UM9151-3 pulse dialer is a monolithic CMOS integrated circuit which converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended to replace mechanical telephone dialers and can operate directly from telephone lines. CMOS technology is used to produced this device, resulting in very low power requirements and high noise immunity. The UM9151-3 can be easily interfaced with a variety of telephones, requiring only a minimal number of of external components.

Pin Configuration & Keyboard Assignments





Block Diagram



Absolute Maximum Ratings *

Power Supply Voltage (V_{DD} - V_{SS}) −0.3V to +5.5V
Input Voltage (V_{IN}) ..... −0.3V to V_{DD} + 0.3V
Maximum Power Dissipation (at 25°C) ..... 600 mW
Operating Temperature (Top) ..... −20°C to +70°C
Storage Temperature (T_{STG}) ..... −55°C to +150°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

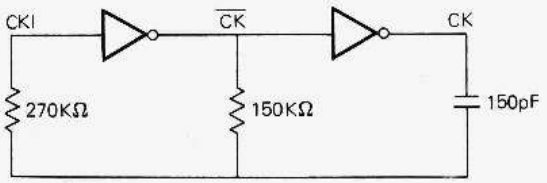
DC Characteristics (V_{DD} = 5.0V, V_{SS} = 0.V, T_{OP} = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Tst.Ckt
Operating Voltage	V_{DD}	2.0		5.5	V	off-hook	B
Memory Retention Current	I_{MR}		0.2	1	μA	V_{DD} = 1.0V, $\overline{HS}$ = V_{DD} all outputs unloaded	B
Supply Operating Current	I_{DD}		30	200	μA	oscillator running, all outputs unloaded	B
Standby Current	I_{SD}		0.5	4	μA	$\overline{HS}$ = V_{DD}, all outputs unloaded	A
Output Sink Current Mute $\overline{DP}$	I_{OL}	2	7		mA	V_{DD} = 2.5V, Vo = 0.5V	C
Output Drive Current Mute	I_{OH}	1	6		mA	V_{DD} = 2.5V, Vo = V_{DD}-1V	C
Input Voltage Range	V_{IH}	0.8V_{DD}		V_{DD}	V_{DD}		
	V_{IL}	Vss		0.2Vss			
Keyboard Input Current	I_{KI}	40	60	150	μA	V_{IN} = V_{SS}, all outputs unloaded	

AC Characteristics (V_{DD} = 3.5V, Vss = 0.V, clock freq. = 18KHz or 36KHz, Top = 25°C unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Make/Break Ratio	M/B	M/$\overline{B}$ = V_{DD}			1/2		
		M/$\overline{B}$ = V_{SS}			2/3		
Dial Pulse Rate	DR	Fosc = 18KHz			10		PPS
		Fosc = 36KHz			20		
Make Time	T_M	10PPS	1/2		33		ms
		10PPS	2/3		40		
		20PPS	1/2		16.6		
		20PPS	2/3		20		
Break Time	T_B	10PPS	1/2		66		ms
		10PPS	2/3		60		
		20PPS	1/2		33		
		20PPS	2/3		30		
Inter-digital Pause Time	T_{IDP}	10PPS	1/2		800		ms
		10PPS	2/3		800		
		20PPS	1/2		400		
		20PPS	2/3		400		
Pre-digital Pause	T_{PDP}	10PPS	1/2		800		ms
		10PPS	2/3		800		
		20PPS	1/2		400		
		20PPS	2/3		400		
Mute Delay Time	T_{MDP}	10PPS	1/2		33		ms
		10PPS	2/3		40		
		20PPS	1/2		16.6		
		20PPS	2/3		20		
Key Depression Period	T_{KDP}	V_{IN} = V_{SS} or V_{DD}		30	40		ms
Key Scan Frequency	F_{KS}	C1~C3, R1~R4, Fosc = 18KHz			200		Hz
Clock Frequency	F_{OSC}	R_{CKI} = 270KΩ	V_{DD} = 2.5V	14.3	17.2	18.1	KHz
		$R_{\overline{CK}}$ = 150K,	V_{DD} = 3.9V	17.2	18.0	18.6	
		C_{CK} = 150pF	V_{DD} = 5.0V	17.8	18.2	19.5	

Pin Description

Pin	Designation	Description
1 2 3 4 14 15 16	R1 - R4 C1 - C3	Key inputs. These inputs can be interfaced to either an XY matrix keyboard or a 2 of 7 type keyboard. The keypad inputs are normally held at high. When a key is depressed, scanning signals (typically 200 Hz) are presented at C1, C2, and C3 inputs; the dialer identifies the key by examining the R1 - R4 inputs. Debouncing is provided to avoid false entry.
5 12	V_{DD} V_{SS}	Positive power supply input. Negative power supply input.
6 7 8	CKI,CK,$\overline{CK}$	Oscillator circuit input/output. The oscillator consists of two inverters, with oscillator frequency controlled by external RC components: R_{CKI} = 270K $R_{\overline{CK}}$ = 150K C_{CK} = 150 pF  Oscillator Circuit
9	$\overline{DP}$	Dialing pulse output. This output consists of an N-channel open drain device. Normally this output will be in off state during make and on during break. Dialing pulse rate = 10 PPS and inter-digital pause = 800 ms when Fosc = 18 KHz in normal mode.
10	M/B	Make/Break ratio select input. In normal mode, this input is used to select the Make/Break ratio: when input = V_{DD}, M/B ratio = 1/2 when input = V_{SS}, M/B ratio = 2/3. When connected to the clock output (pin 7), this input can trigger the UM9151-3 into test mode, generating high speed dialing (DPR = 600 PPS, IDP = 13.3 ms).
11	$\overline{HK}$	Hook switch input. This input is used to detect whether the telephone is in the on-hook or off-hook state: V_{DD} = on-hook V_{SS} = off-hook. (Resetting time = 200 ms minimum.)
13	MUTE	Mute output. This output is an inverter normally at low state when there is no key entry. During outdialing it changes to high state and is used to mute the speech network.

Operational Procedures

Symbol Definitions:
Dp: pulse digit (0 through 9)
ZiZiZi: conversation
O-O↑: off-hook.
O-O↓: on-hook.
[*] or [#] : Redial

Recommended Operations:
Normal dialing:
O-O↑; DP...Dp; ZiZiZi; O-O↓.
Dial pulse begins as soon as first key is entered. Debounced and detected on chip.

Redialing:
O-O↑; [*] or [#] key
([*] or [#] key can be accepted as first key entry after off-hook.)

Functional Description

1) N-channel open drain output — $\overline{DP}$ (figure 1).

2) Clock oscillator.
The clock oscillator consists of two inverters, with the frequency of oscillation controlled by external components connected to pins 6, 7, and 8. The circuit is sufficiently versatile to allow the use of a variety of external component configurations. The oscillator circuit is shown in figure 2.

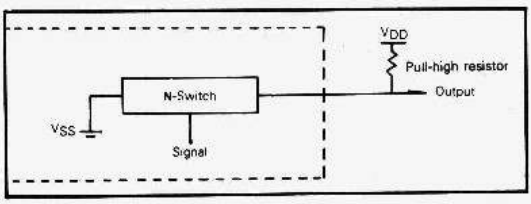


Figure 1

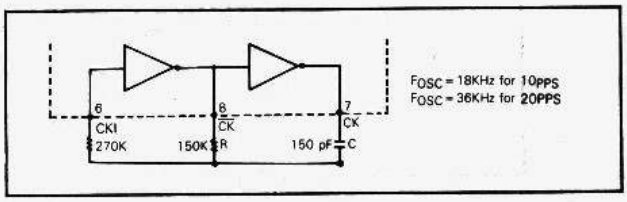


Figure 2

Timing Diagram