



IRF520 IRF521
IRF522 IRF523
R520 R521



**N-Channel Enhancement-Mode
Vertical DMOS Power FETs**

Preliminary
T-39-11

Ordering Information

$BV_{DSS} /$ BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-220	TO-92
100V	0.3Ω	8.0A	IRF520	R520
60V	0.3Ω	8.0A	IRF521	R521
100V	0.4Ω	7.0A	IRF522	—
60V	0.4Ω	7.0A	IRF523	—

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

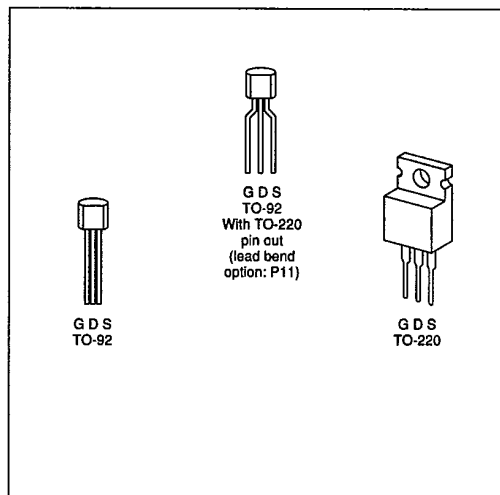
- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options



Thermal Characteristics

IRF520/IRF521/IRF522/IRF523/R520/R521

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JB} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
IRF520, IRF521	8.0A	32.0A	40W	80	3.12	8.0A	32.0A
IRF522, IRF523	7.0A	32.0A	40W	80	3.12	8.0A	32.0A
R520, R521	1.0A	9.0A	1W	170	125	1.0A	9.0A

* I_D (continuous) is limited by max rated T_J .Electrical Characteristics (@ 25°C unless otherwise specified)

T-39-11

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100			V	$V_{GS} = 0, I_D = 250\mu\text{A}$
		60				
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$
I_{GSS}	Gate Body Leakage			500	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			250	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				1000		$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_C = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	8.0			A	$V_{GS} = 10\text{V}$ $V_{DS} > I_{D(ON)} \times R_{DS(ON)} \text{ Max Rating}$
		7.0				
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.3	Ω	$V_{GS} = 10\text{V}, I_D = 4.0\text{A}$
				0.4		
G_{FS}	Forward Transconductance	1.5	2.9		S	$V_{DS} > I_{D(ON)} \times R_{DS(ON)} \text{ Max Rating}$ $I_D = 4.0\text{A}$
C_{ISS}	Input Capacitance			600	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			400		
C_{RSS}	Reverse Transfer Capacitance			100		
$t_{d(ON)}$	Turn-ON Delay Time			40	ns	$V_{DD} = 0.5BV_{DSS}$ $I_D = 4.0\text{A}$ $V_{DS} = 0.8 \text{ Max Rating}$
t_r	Rise Time			70		
$t_{d(OFF)}$	Turn-OFF Delay Time			100		
t_f	Fall Time			70		
V_{SD}	Diode Forward Voltage Drop			2.5	V	$V_{GS} = 0\text{V}, I_{SD} = 1\text{A}$
				2.3		$V_{GS} = 0\text{V}, I_{SD} = 8\text{A}$
t_{rr}	Reverse Recovery Time		280		ns	$T_J = 150^\circ\text{C}, I_F = 8.0\text{A},$ $dI_{F}/dt = 100\text{A}/\mu\text{S}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu\text{s}$ pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

