

## **Design Considerations for a Low Voltage N-Channel H-Bridge Motor Drive**

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### **INTRODUCTION**

In low voltage motor drives, it is common practice to use complementary MOSFET half-bridges to simplify the gate drive design. However, the P-channel FET within the half-bridge usually has a higher on resistance or is larger and more expensive than the N-channel FET. The alternative solution is to design in an N-channel half-bridge. The N-channel half-bridge uses silicon more efficiently, while minimizing conduction losses and power device expense. The tradeoff to take advantage of N-channel devices is found in increased gate drive design complexity. Minimizing the gate drive complexity in a brushed DC motor drive with an

all N-channel H-bridge is the focus of this note. In addition, design considerations, diode snap and shoot-through current are discussed and circuit solutions are given.

The result of the design is evaluation board DEVB151 shown in Figure 1. DEVB151 features an MPM3017 N-channel, H-bridge and circuitry designed to interface power devices within the MPM3017 to microprocessor outputs. The board drives 24-volt to 48-volt motors and can handle 8 amps of continuous motor current. A detailed description of the evaluation board is presented within this Application Note.

Figure 1. N-channel, H-bridge Motor Drive (DEVB151)



## DESIGN CONSIDERATIONS

### High-side Gate Drive Voltage

Using N-channel half-bridges requires circuitry that produces voltage above the motor voltage rail and turns the upper transistors on. One method of accomplishing this task is to use a charge pump. The charge pump shown in Figure 2 provides a constant voltage greater than 12 volts above the motor rail at all motor speeds, unlike the capacitor bootstrap approach, and is less expensive than a transformer isolated gate drive.

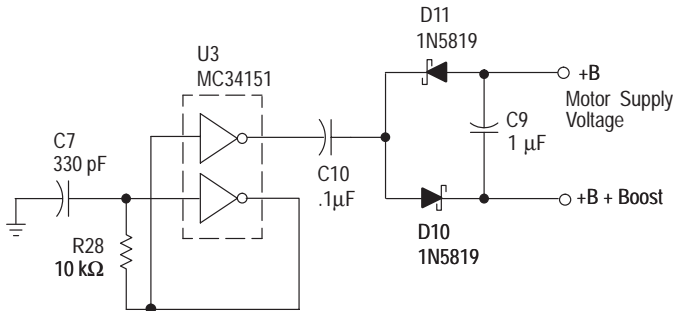


Figure 2. Charge Pump

An oscillator, two capacitors and two diodes are all the components necessary to build a charge pump. The inverter, MC34151, is configured as an oscillator with C7 and R28 determining the frequency. The charge pump action is as follows. C10 charges up to the rail voltage minus a diode drop when the IC's output is low. When the IC's output swings high, C10 dumps charge into C9. The cycle is continuously

repeated. In steady state, the voltage across C9 is the voltage swing of the IC's output minus two diode drops. This voltage is in series with the rail voltage, B+, and the sum is sufficient to drive the high-side FETs.

Voltage losses in the charge pump are from the diode forward drops and the IC's output voltage swing. To minimize the diode voltage drops, Schottky diodes are implemented. The loss in the IC's output voltage swing is dependent on the level of current the charge pump is asked to support. For example, if the charge pump is to support 50 mA, the IC's output swing diminishes by approximately 2 V. This is of particular concern when operating from a voltage source less than 15 V. Gate drive voltage is compromised when operating from a supply voltage of less than 15 volts which results in increased power dissipation.

### High-side Gate Drive

Now that boost voltage is available for the high-side FETs, a means of switching this voltage to the gate is needed. Together the MDC1000A and a switched current source, shown in Figure 3, accomplish this requirement.

The MDC1000A, a MOS turn-off device (MTO), is very useful in the high-side FET applications. It discharges the gate-to-source capacitance quickly and contains a zener clamp for gate protection. To charge the gate-to-source capacitance, the MTO passes current to the gate of the FET. When the gate-to-source voltage reaches the zener clamp voltage, the current is shunted through the zener. When the current source is turned off, a resistor internal to the MTO pulls down on the anode of the series diode. After the anode voltage falls approximately one diode drop, the internal SCR fires, discharging the gate-to-source capacitance. The series gate resistor, R19, limits the rate of discharge of the gate and therefore determines the turn-off time. It will be shown

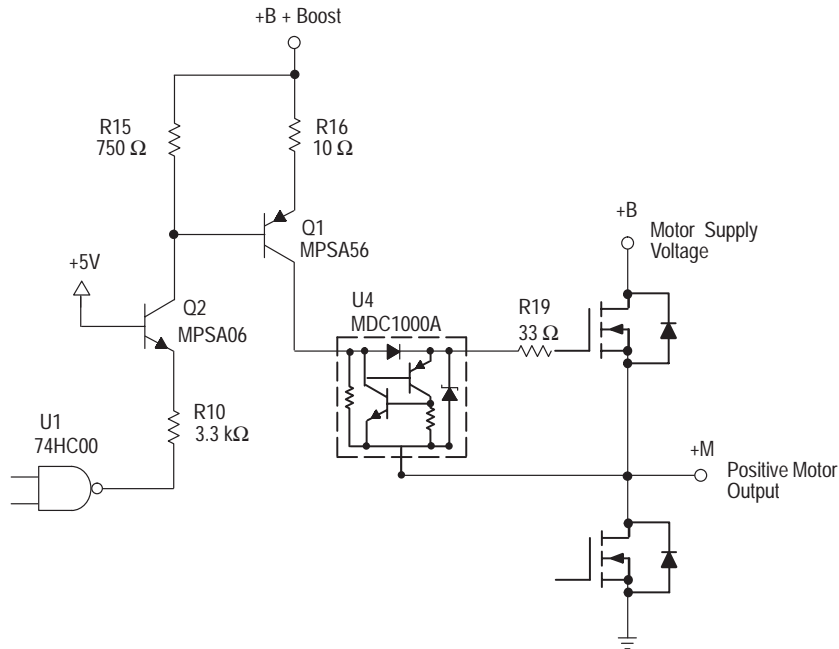


Figure 3. High-side Gate Drive

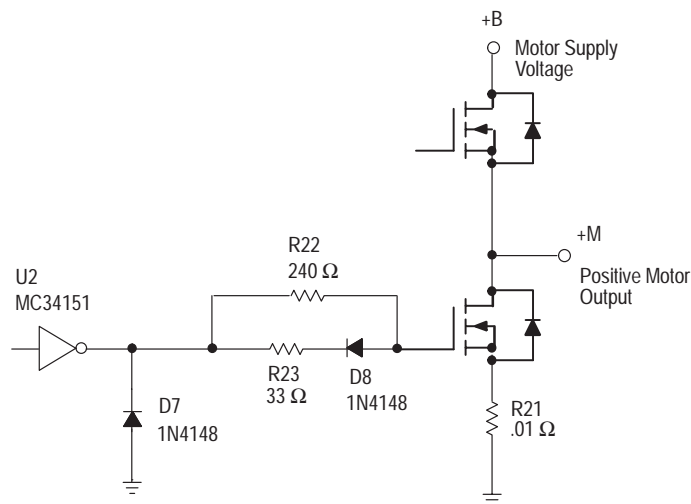


Figure 4. Low-side Gate Drive

later that this resistor also plays a key role in solving the dynamic issues of the motor drive.

The current source used with the MTO consists of a PNP transistor, Q1, and resistors R15 and R16. The FET turn-on time is determined by the sourced current. The reference current is the collector current of the level shifting transistor, Q2, and is set by resistor R10. The reference current is established when the NAND gate output is logic 0. The reference current, though small, must be supported by the charge pump.

**Low-side Gate Drive**

The low-side gate drive design, as shown in Figure 4, is relatively simple compared to the high side. The MC34151, used before as an oscillator in the charge pump, is an integrated circuit specifically designed to drive the gate of a power MOSFET. The input to this device can be a 5 volt logic level signal like that of a microcontroller. The MC34151 is capable of sourcing and sinking approximately 1.5 amperes. Therefore, to limit the current into the gate and control the turn-on time, a resistor, R22, is needed between the IC and FET. An additional resistor, R23, in series with

a diode, D8, is placed in parallel with R22 to implement a faster turn-off time. The need for separate turn-on and turn-off times will become clear when the dynamic characteristics are explained.

**Dynamic Issues**

In addition to static gate drive designs, more difficult dynamic design challenges must be addressed. These issues include diode snap and shoot-through current. A description of these issues and solutions follows.

A pulse width modulated motor drive is usually a continuous mode clamped inductive load – i.e. – current continually flows through the inductance. Referring to the simplified half-bridge circuit of Figure 5, current through the motor ramps up when Q2 is on and freewheels through Q1's internal diode when Q2 is switched off.

When Q2 turns on again, the stored charge within Q1's diode must be cleared. The resulting drain current of Q2 is shown in the turn-on waveform of Figure 6.

The first current peak in Figure 6 shows up as current from the rail to ground, bypassing the motor. This current has two components. The first is the expected reverse recovery

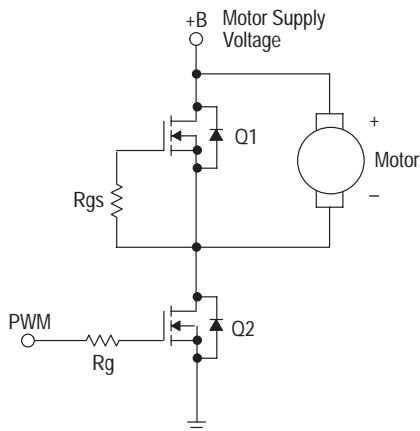


Figure 5. Simplified Half-Bridge

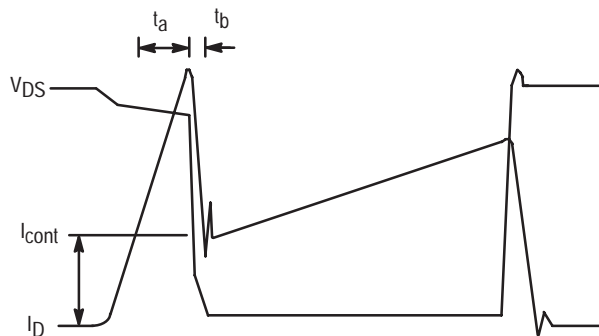


Figure 6. Turn-on Wave Form

current of the internal diode of Q1. The second is  $dv/dt$  generated shoot-through current.

Reverse recovery characteristics of the freewheeling diode are at the root of the system design challenges. Referring to Figure 6, FET intrinsic diode reverse recovery tends to be fairly snappy;  $t_b$  is much shorter than  $t_a$ . It follows that  $di/dt$  during  $t_b$  is greater than during  $t_a$ , and if unmanageably high, invites unpredictable behavior and unwanted voltage spikes. In addition,  $V_{DS}$  falls very rapidly during  $t_b$ . Referring to Figure 5, the  $dv/dt$  created during  $t_b$  couples through to the gate-to-drain capacitance of the upper FET. A current proportional to  $dv/dt$  and  $C_{DG}$  flows through the top FET gate impedance, develops a gate-to-source voltage, and turns the FET on. The result is current from the supply to ground through the half-bridge called shoot-through current.

Shoot-through and reverse-recovery current bypass the motor and therefore only contribute to power dissipation. Other unwanted side effects consist of EMI and unpredictable gate drive performance from high  $di/dts$  acting upon lead and stray PCB trace inductance. However, control of diode snap and shoot-through current is accomplished by employing a gate drive impedance strategy.

The gate-to-source impedance of the upper FET as shown in Figure 5, controls the voltage developed across

gate to source during  $t_b$  and therefore controls the shoot-through current. A low impedance will obviously minimize shoot-through current, but there exists a value that lets an optimal portion of shoot-through current pass. This impedance can be adjusted until the turn-on waveform appears to be critically damped. The FET is conducting as the diode is snapping. If the total current is dominated by the FET condition, the sharp snap of the diode is hidden. The net effect is a softer recovery characteristic.

The turn-on gate impedance of the bottom pulse width modulated FET of Figure 5 also plays a key role in softening the reverse recovery characteristic. This impedance sets the positive  $di/dt$  during  $t_a$ . The stored charge in the freewheeling diode is a function of applied  $di/dt$  and as  $t_a$  becomes shorter, the diode snaps more severely. This implies that the turn-on gate impedance must be set to a value that will create a manageable positive  $di/dt$  and enable the strategy undertaken to control diode snap.

An increase in power dissipation is sacrificed for a more desirable turn-on waveform. Considering the problems that arise with unmanageable  $di/dts$ , such as EMI, voltage spikes, possible oscillation at turn-on, and possibly a large amount of power dissipation, the trade-off is to the designer's advantage.

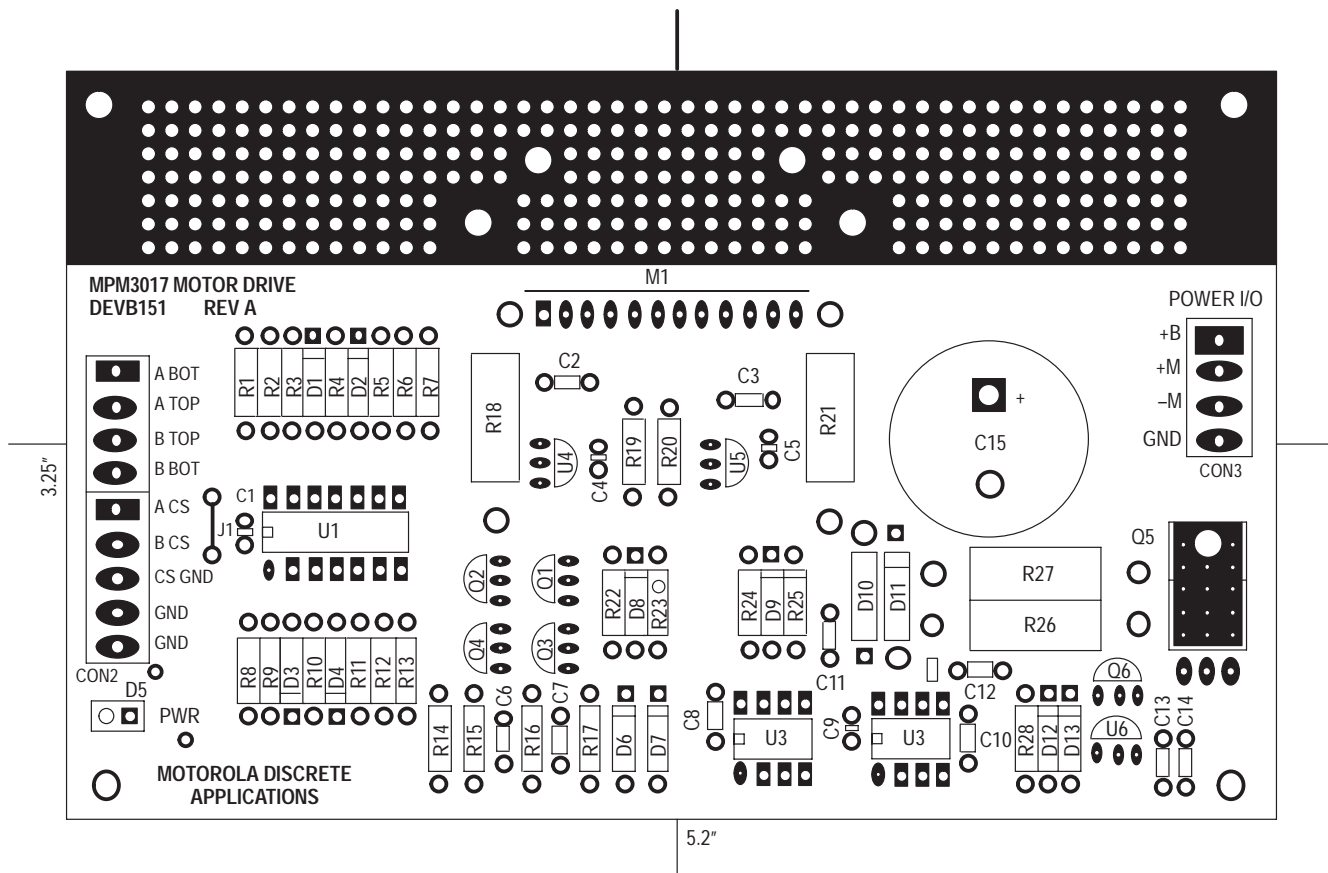


Figure 7. Component Layout

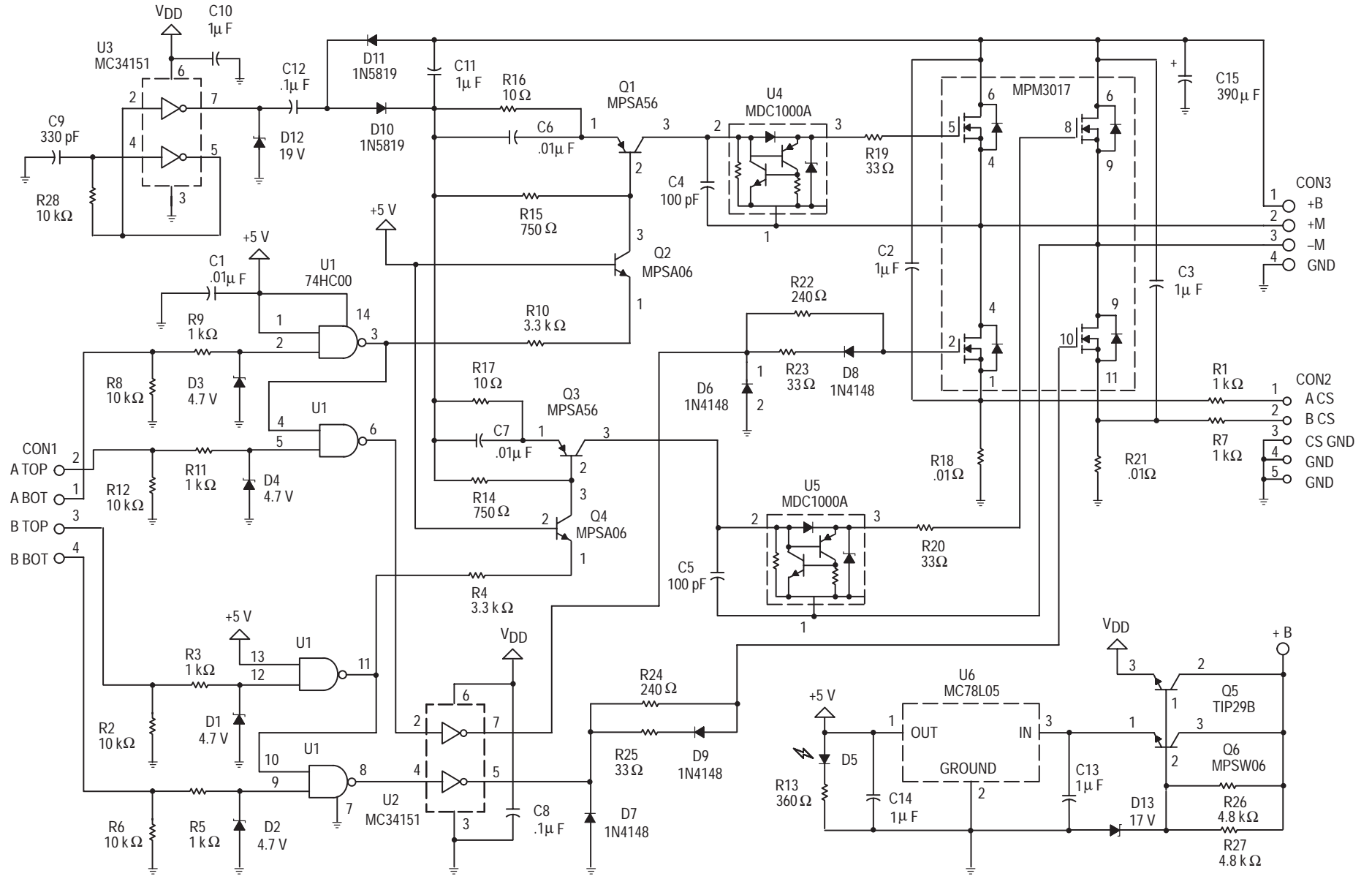


Figure 8. MPM3017 Motor Drive Schematic

Table 1. Parts List

Designators	Quantity	Description	Rating	Manufacturer	Part Number
C1,C6,C7	3	.01 $\mu$ F Ceramic Cap	100 V		
C2,C3,C10,C11,C13,C14	6	1 $\mu$ F Ceramic Cap	100 V		
C4,C5	2	100 pF Ceramic Cap	100 V		
C6,C8,C12	2	.1 $\mu$ F Ceramic Cap	100 V		
C9	1	330 pF Ceramic Cap	100 V		
C15	1	390 $\mu$ F Electrolytic Cap	100 V	Sprague	80D391P100HA2
CON1,CON3	1	4 Terminal Connector			
CON2	1	5 Terminal Connector			
D1,D2,D3,D4	4	4.7 V Zener	500 mW	Motorola	1N5230B
D5	1	LED (RED)		GI	MV57124A
D6,D7,D8,D9	4	Diode		Motorola	1N4148
D10,D11	2	Diode Schottky	1 A,40 V	Motorola	1N5819
D12	1	19 V Zener	500 mW	Motorola	1N5249B
D13	1	17 V Zener	500 mW	Motorola	1N5247B
M1	1	N-ch H-Bridge	60 V/25 A	Motorola	MPM3017
Q1,Q3	2	PNP Transistor	80 V	Motorola	MPSA56
Q2,Q4	2	NPN Transistor	80 V	Motorola	MPSA06
Q5	1	NPN Transistor	80 V/2 W	Motorola	TIP29B
Q6	1	NPN Transistor	80 V/1 W	Motorola	MPSW06
R1,R3,R5,R7,R9,R11	6	1 k $\Omega$ Resistor	.25 W		
R2,R6,R8,R12,R28	5	10 k $\Omega$ Resistor	.25 W		
R4,R10	2	3.3 k $\Omega$ Resistor	.25 W		
R13	1	360 $\Omega$ Resistor	.25 W		
R14,R15	2	750 $\Omega$ Resistor	.25 W		
R16,R17	2	10 $\Omega$ Resistor	.25 W		
R18,R21	2	.01 $\Omega$ Resistor	2.25 W	Mills	MRP-2-NI
R19,R20,R23,R25	4	33 $\Omega$ Resistor	.25 W		
R22,R24	2	240 $\Omega$ Resistor	.25 W		
R26,R27	2	4.8k $\Omega$ Resistor	1 W		
U1	1	Quad 2 input NAND		Motorola	MC74HC00AN
U2,U3	2	MOSFET Driver		Motorola	MC34151P
U4,U5	2	MOS Turn-off Device		Motorola	MDC1000A
U6	1	3-pin Voltage Regulator		Motorola	MC78L05ACP

Additional decoupling capacitors across each half-bridge provide high frequency current for reverse recovery. Any sharp voltage spikes created during reverse recovery are smoothed out and kept from propagating to the other half-bridge creating unwanted noise. These decoupling capacitors should be physically placed as close to the half-bridge as possible.

The PCB layout is also a very important design consideration. Care must be taken to minimize the source inductance and any stray inductance in the high current paths. This is done by keeping the high current traces as wide and as short as possible. Another rule to follow is that the low current ground traces or trace should tie to the high current trace at one central grounding point. Typically the sources of the power transistors are used as the grounding point. If using current sense resistors, the leads terminating to ground must be the central grounding point.

The dynamic design challenges are solved simply by employing a gate drive impedance strategy. The different gate impedances in Figures 2 and 3 are optimized to control the turn-on  $di/dt$ , shoot-through current and diode snap. Faster turn-off of the bottom FETs minimizes turn-off switching losses.

## BOARD DESCRIPTION

Evaluation board DEVB151 was designed to be an electronic building block that interfaces a microcontroller to a motor. This board translates HCMOS logic signals, like those from a microprocessor or microcontroller, to motor turning power. DEVB151 can drive a brushed DC motor in both directions or drive one phase of a stepper motor. Four inputs to the board control the gates of H-Bridge configured FETs. The outputs of the board include + and – terminals for the motor and current-sense terminals for each half-bridge. A single voltage power source is all that is required to operate the board. A silk-screen plot and a full schematic are shown in Figures 7 and 8, respectively. The board content is listed in Table 1.

All control inputs and current sense outputs are on the left side of the board. Inputs A TOP, A BOT, B TOP, and B BOT each correspond to a similarly labeled power FET and have positive logic. For example, when B TOP is logic 1 its corresponding transistor is on. To prevent an accidental simultaneous conduction of either half-bridge (A TOP=A BOT=1 or B TOP=B BOT=1), protection circuitry was added

to the design. Cross-coupled NAND gates disable the bottom transistor when the top transistor is on. This protection scheme has another advantage. Inputs A BOT and B BOT can be tied together and share the same PWM signal. The logic of the upper transistors determines which bottom transistor is pulse width modulated. Resistors and zeners are additions to the board inputs to deter static damage of the NAND gates. The NAND inputs are directly compatible with 5 volt HCMOS logic and form a direct interface to microcontrollers and microprocessors.

The voltages at output terminals A CS and B CS are the representations of the current through each half-bridge, respectively. Current is related to the voltage present at these terminals by a ratio of 100 amps per volt. To incorporate a single-current sense voltage, jumper J1, can be installed. This ties the current sense resistors from each half-bridge together. In this case, the output voltage at A CS or B CS is related to the current by a ratio of 200 amps per volt. The voltage representation of the currents at these terminals is very noisy. To obtain a clean sense voltage, low pass filtering is recommended before sampling. CS GND terminal is ground for the current sense outputs. Along with this ground, two more terminals are labeled ground. One is used for the ground lead from the microcontroller and the other is available as an instrument grounding point.

All power connections are on the right side of the board. Power to the board is brought in on the +B and GND terminals. The power outputs to the motor are the +M and – M terminals.

The heart of DEVB151 is the MPM3017. The MPM3017 is made up of four N-channel power MOSFETs which have an  $R_{DS(on)}$  rating of 40 m $\Omega$  maximum, a breakdown voltage of 60 volts and are energy rated. The remainder of operating specifications are listed in Table 2.

Application of DEVB151 is shown in the diagram of Figure 9. An 8 bit microcontroller, such as the MC68HC11, can be readily programmed to generate the required signals to operate this evaluation board. This microcontroller contains a general purpose timer used to perform the time-intensive tasks of generating a PWM signal. The cross-coupled NAND gates at the inputs of DEVB151 allow the use of only one PWM signal. The direction signals can simply be outputs from an available parallel port. In Figure 8, two bits of port B are used as the direction signals, and port A, pin 6 is the output carrying the PWM signal.

**Table 2. Electrical Characteristics**

Characteristic	Symbol	Min	Typ	Max	Units
Input voltage	+B	18		48	Volts
Peak motor current	$I_{PK}$			30	Amps
Continuous motor current	$I_C$			8	Amps
Minimum logic 1 input voltage	$V_{IH}$		2.7		Volts
Maximum logic 0 input voltage	$V_{IL}$		2.0		Volts
Power dissipation	$P_D$			7	Watts
Sense voltage	$V_{sense}$		10		mV/A

\* Additional heat sinking will increase the maximum power dissipation rating.

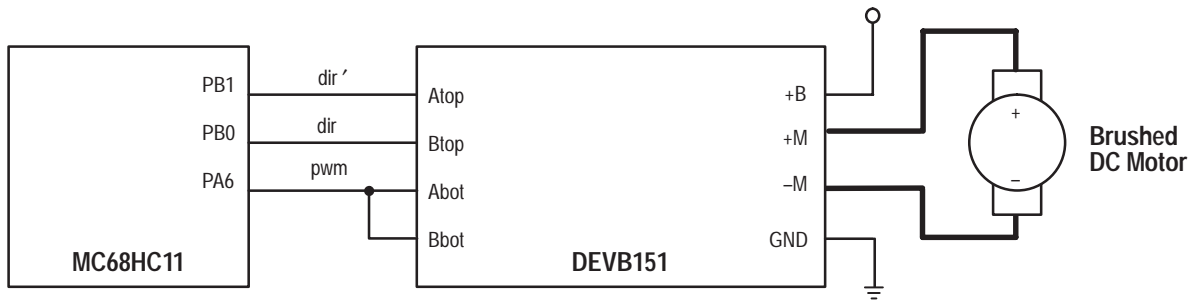


Figure 9. Application Block Diagram

## CONCLUSIONS

N-channel half-bridges increase performance of motor drive systems over that of complementary half-bridges. However, the dynamic issues of the design remain constant for both topologies. Shoot-through current and diode snap are managed by relatively simple circuit solutions. These circuit solutions stem from the optimization of the gate impedances for separate turn-on and turn-off speeds. The additional voltage needed to drive the upper half of the N-channel half-bridges above the motor voltage is derived from a charge pump.


DEVB151 is more efficiently used if the bottom transistors are pulse-width modulated rather than the upper transistors. The top transistors can be pulse-width modulated, however, due to limitations of the high-side gate drive, top FET turn-on speed is slower than that of the bottom FETs. The slower turn-on speed leads to greater switching losses.

Losses in the charge pump circuitry limit the low end supply voltage to 15 volts, therefore DEVB151 does not address the 12 volt market. However, implementing a voltage tripler, a modified charge pump, will allow operation down to 12 volts.

Looking at DEVB151 as a building block between a microcontroller and a motor, the board is kept simple and is protected from accidental misuse. DEVB151 only needs a single voltage source from which different voltage levels are supplied to the various internal devices. The cross-coupled NAND gates prohibit the user from accidentally destroying the power transistors on the board. All inputs and outputs are clearly labeled and are fairly self-explanatory.

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