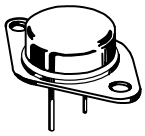
2N5038

NPN Silicon Transistors

. . . fast switching speeds and high current capacity ideally suit these parts for use in switching regulators, inverters, wide–band amplifiers and power oscillators in industrial and commercial applications.

- High Speed – t_f = 0.5 μs (Max)
- High Current – $I_{C(max)}$ = 30 Amps
- Low Saturation – $V_{CE(sat)}$ = 2.5 V (Max) @ I_C = 20 Amps

20 AMPERE
NPN SILICON
POWER TRANSISTOR
90 VOLTS
140 WATTS



CASE 1–07
TO–204AA
(TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CBO}	150	Vdc
Collector–Emitter Voltage	V_{CEV}	150	Vdc
Emitter–Base Voltage	V_{EBO}	7	Vdc
Collector Current – Continuous Peak (1)	I_C I_{CM}	20 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	140 0.8	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.25	°C/W

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 10 ms, Duty Cycle ≤ 50%.

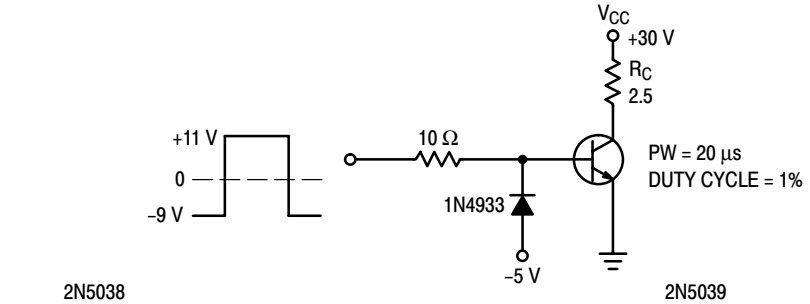


Figure 1. Switching Time Test Circuit

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Publication Order Number:
2N5038/D

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (2) (I_C = 200 mAdc, I_B = 0)		$V_{CEO(sus)}$	90	–	Vdc
Collector Cutoff Current (V_{CE} = 140 Vdc, $V_{BE(off)}$ = 1.5 V) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	– –	50 10	mAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0) (V_{EB} = 7 Vdc, I_C = 0)		I_{EBO}	– –	5 50	mAdc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 12 Adc, V_{CE} = 5 Vdc)		h_{FE}	20	100	–
Collector–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{CE(sat)}$	–	2.5	Vdc
Base–Emitter Saturation Voltage (I_C = 20 Adc, I_B = 5 Adc)		$V_{BE(sat)}$	–	3.3	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common–Emitter Small–Signal Short–Circuit Forward Current Transfer Ratio (I_C = 2 Adc, V_{CE} = 10 Vdc, f = 5 MHz)		$\|h_{fe}\|$	12	–	–
SWITCHING CHARACTERISTICS					
RESISTIVE LOAD					
Rise Time	(V_{CC} = 30 Vdc)	t_r	–	0.5	μs
Storage Time	(I_C = 12 Adc, I_{B1} = I_{B2} = 1.2 Adc)	t_s	–	1.5	μs

*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width ≤ 300, μs, Duty Cycle ≤ 2%.

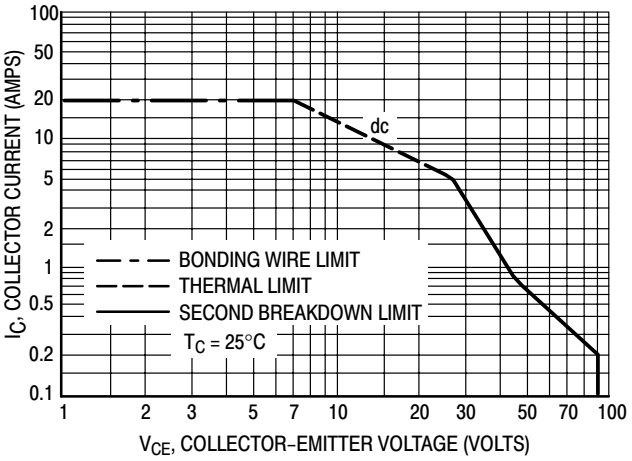


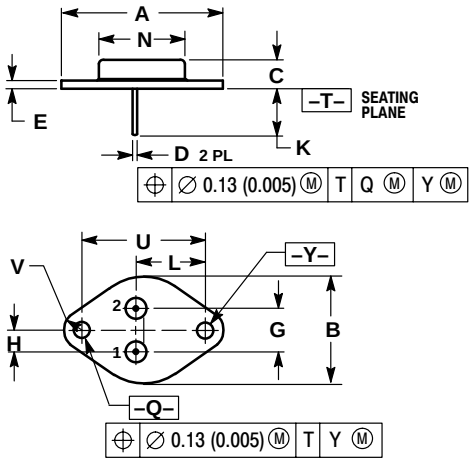
Figure 2. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Second breakdown pulse limits are valid for duty cycles to 10%. At high case temperatures, thermal limitations may reduce the power that can be handled to values less than the limitations imposed by second breakdown.

PACKAGE DIMENSIONS

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

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