

High-Voltage - High Power Transistors

... designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

- High Collector Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 140 \text{ Vdc}$
- High DC Current Gain – @ $I_C = 8.0 \text{ Adc}$
 $h_{FE} = 15 \text{ (Min)}$
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 10 \text{ Adc}$

MAXIMUM RATINGS (1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	140	Vdc
Collector–Base Voltage	V_{CB}	140	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current – Continuous Peak	I_C	16 20	A dc
Base Current – Continuous	I_B	5.0	A dc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.

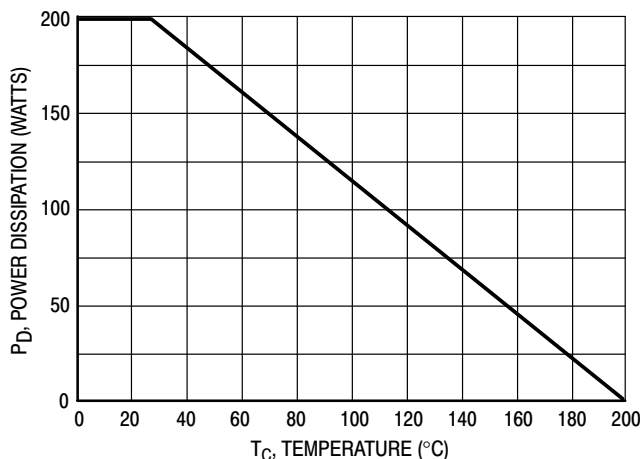
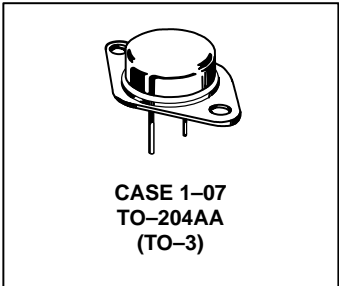


Figure 1. Power Derating

Safe Area Curves are indicated by Figure 5. All Limits are applicable and must be observed.

**NPN
2N5631
PNP
2N6031**

**16 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
140 VOLTS
200 WATTS**



2N5631 2N6031

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (2) (I _C = 200 mA _{dc} , I _B = 0)	V _{CEO(sus)}	140	–	V _{dc}
Collector–Emitter Cutoff Current (V _{CE} = 70 V _{dc} , I _B = 0)	I _{CEO}	–	2.0	mA _{dc}
Collector–Emitter Cutoff Current (V _{CE} = Rated V _{CB} , V _{EB(off)} = 1.5 V _{dc}) (V _{CE} = Rated V _{CB} , V _{EB(off)} = 1.5 V _{dc} , T _C = 150°C)	I _{CEX}	–	2.0 7.0	mA _{dc}
Collector–Base Cutoff Current (V _{CB} = Rated V _{CB} , I _E = 0)	I _{CBO}	–	2.0	mA _{dc}
Emitter–Base Cutoff Current (V _{BE} = 7.0 V _{dc} , I _C = 0)	I _{EBO}	–	5.0	mA _{dc}

ON CHARACTERISTICS (2)

DC Current Gain (I _C = 8 A _{dc} , V _{CE} = 2.0 V _{dc}) (I _C = 16 A _{dc} , V _{CE} = 2.0 V _{dc})	h _{FE}	15 4.0	60 –	–
Collector–Emitter Saturation Voltage (I _C = 10 A _{dc} , I _B = 1.0 A _{dc}) (I _C = 16 A _{dc} , I _B = 4.0 A _{dc})	V _{CE(sat)}	– –	1.0 2.0	V _{dc}
Base–Emitter Saturation Voltage (I _C = 10 A _{dc} , I _B = 1.0 A _{dc})	V _{BE(sat)}	–	1.8	V _{dc}
Base–Emitter On Voltage (I _C = 8.0 A _{dc} , V _{CE} = 2.0 V _{dc})	V _{BE(on)}	–	1.5	V _{dc}

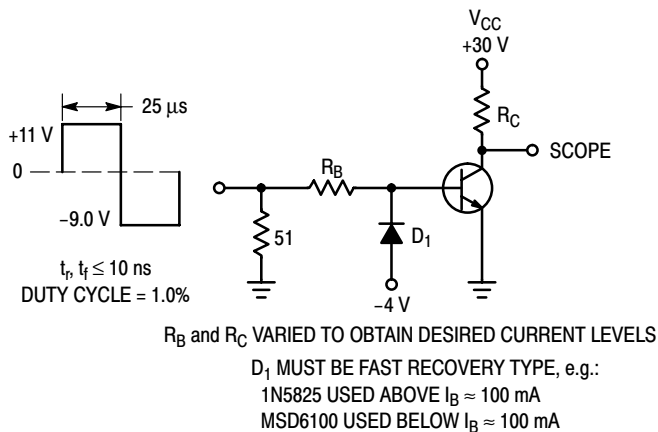
DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (3) (I _C = 1.0 A _{dc} , V _{CE} = 20 V _{dc} , f _{test} = 0.5 MHz)	f _T	1.0	–	MHz
Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f = 0.1 MHz)	2N5631 2N6031 C _{ob}	– –	500 1000	pF
Small–Signal Current Gain (I _C = 4.0 A _{dc} , V _{CE} = 10 V _{dc} , f = 1.0 kHz)	h _{fe}	15	–	–

*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.

(2) f_T = |h_{fe}| • f_{test}



For PNP test circuit, reverse all polarities and D1.

Figure 2. Switching Times Test Circuit

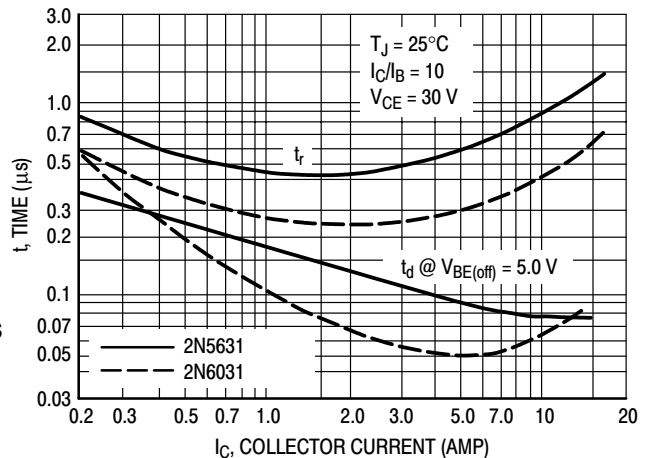


Figure 3. Turn–On Time

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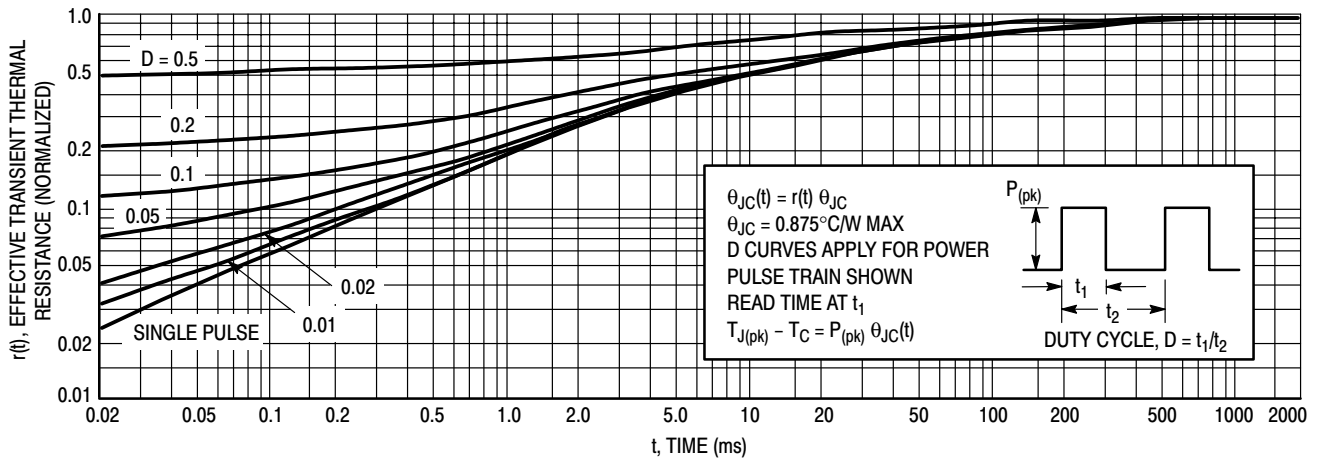


Figure 4. Thermal Response

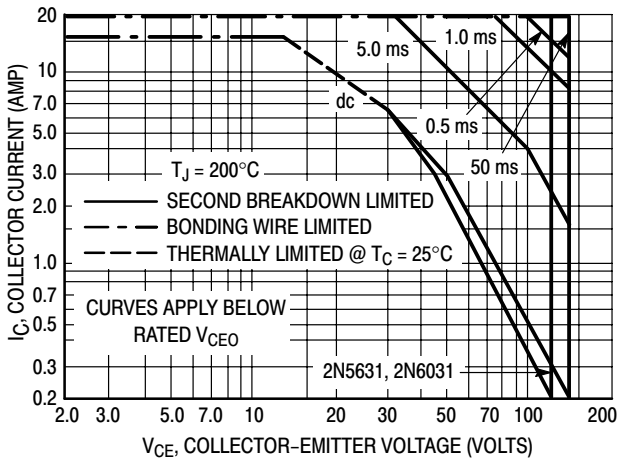


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

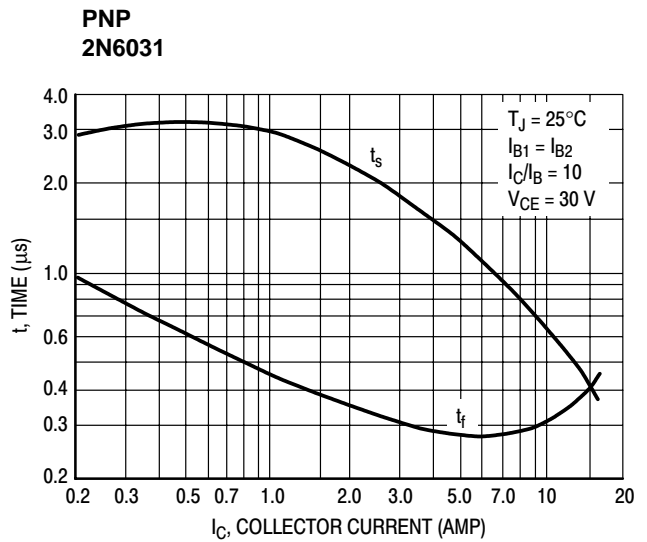
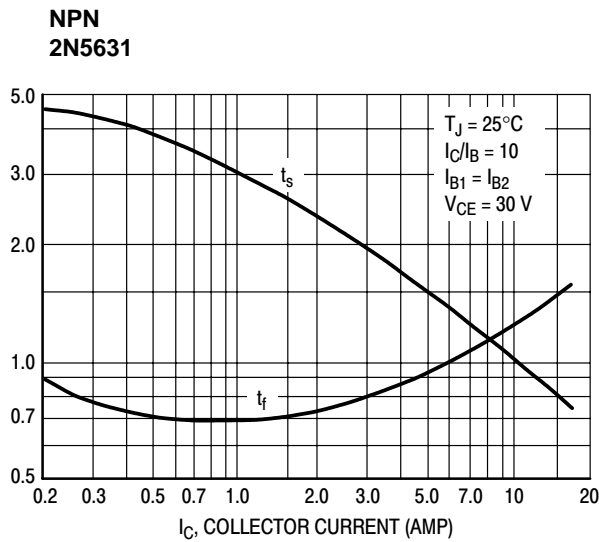


Figure 6. Turn-Off Time

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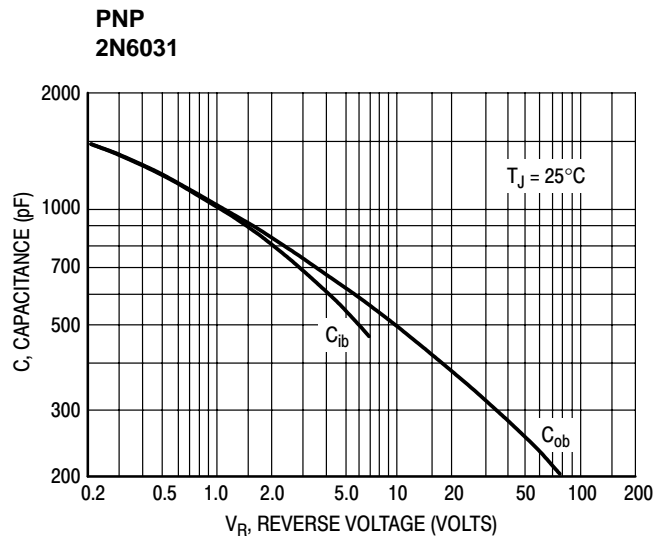
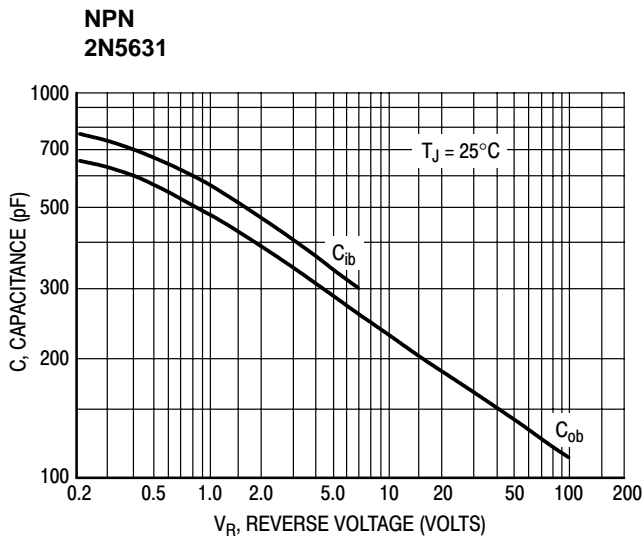


Figure 7. Capacitance

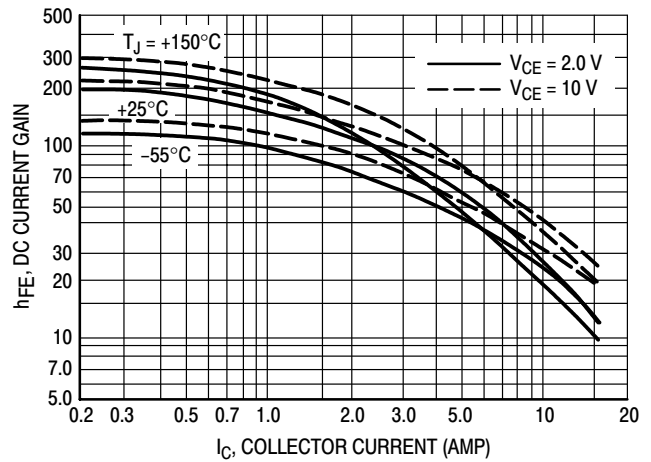
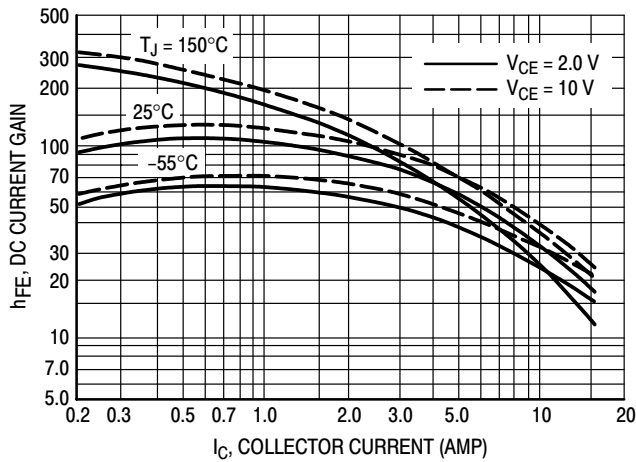


Figure 8. DC Current Gain

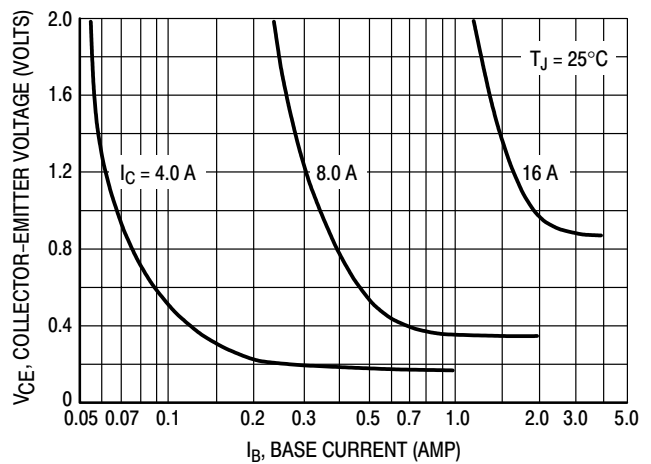
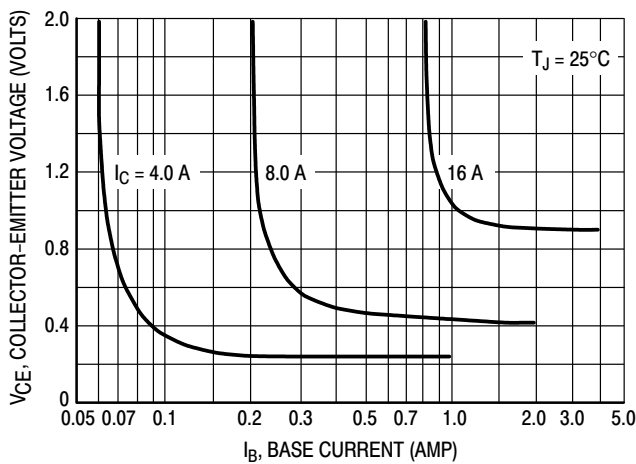


Figure 9. Collector Saturation Region

Notes

Notes

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