PNP 2N5883, 2N5884*, NPN 2N5885, 2N5886*

Preferred Device

Complementary Silicon High-Power Transistors

. . . designed for general–purpose power amplifier and switching applications.

- Low Collector–Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 1.0 Vdc, (max) at I_C = 15 Adc
- Low Leakage Current
  I_{CEX} = 1.0 mAdc (max) at Rated Voltage
- Excellent DC Current Gain –
  h_{FE} = 20 (min) at I_C = 10 Adc
- High Current Gain Bandwidth Product –
  f_τ = 4.0 MHz (min) at I_C = 1.0 Adc

MAXIMUM RATINGS (No

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector–Emitter Voltage	V_{CEO}	60	80	Vdc
Collector–Base Voltage	V_{CB}	60	80	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous Peak	I_C	25 50		Adc
Base Current	I_B	7.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	200 1.15		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.875	°C/W

1. Indicates JEDEC registered data. Units and conditions differ on some parameters and re–registration reflecting these changes has been requested. All above values most or exceed present JEDEC registered data.

ON Semiconductor®

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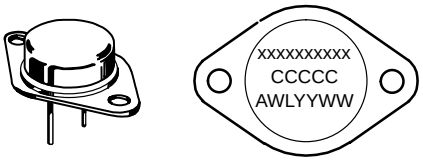
25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60 – 80 V 200 W

MARKING DIAGRAM



CASE 1–07
TO–204AA
(TO–3)

xx = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
CCCCC = Non USA Country Code

Preferred devices are recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (Note 2) (I_C = 200 mAdc, I_B = 0)	2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0)	2N5883, 2N5885 2N5984, 2N5886	I_{CEO}	– –	2.0 2.0	mAdc
Collector Cutoff Current		I_{CEX}			mAdc
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5883, 2N5885		–	1.0	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N5884, 2N5886		–	1.0	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5883, 2N5885			10	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N5884, 2N5886		–	10	
Collector Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 60 Vdc, I_E = 0)	2N5883, 2N5885		–	1.0	
(V_{CB} = 80 Vdc, I_E = 0)	2N5884, 2N5886		–	1.0	
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc

ON CHARACTERISTICS

DC Current Gain (Note 2)	(I_C = 3.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc) (I_C = 25 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	35 20 4.0	– 100	–
Collector–Emitter Saturation Voltage (Note 2)	(I_C = 15 Adc, I_B = 1.5 Adc) (I_C = 25 Adc, I_B = 6.25 Adc)	$V_{CE(sat)}$	– –	1.0 4.0	Vdc
Base–Emitter Saturation Voltage (Note 2)	(I_C = 25 Adc, I_B = 6.25 Adc)	$V_{BE(sat)}$	–	2.5	Vdc
Base–Emitter On Voltage (Note 2)	(I_C = 10 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 3)	(I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	2N5883, 2N5884 2N5885, 2N5886	C_{ob}	– –	1000 500	pF
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f_{test} = 1.0 kHz)		h_{fe}	20	–	–

SWITCHING CHARACTERISTICS

Rise Time	(V_{CC} = 30 Vdc, I_C = 10 Adc, I_{B1} = I_{B2} = 1.0 Adc)	t_r	–	0.7	μs
Storage Time		t_s	–	1.0	μs
Fall Time		t_f	–	0.8	μs

*Indicates JEDEC Registered Data.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. $f_T = |h_{fe}| \bullet f_{test}$.

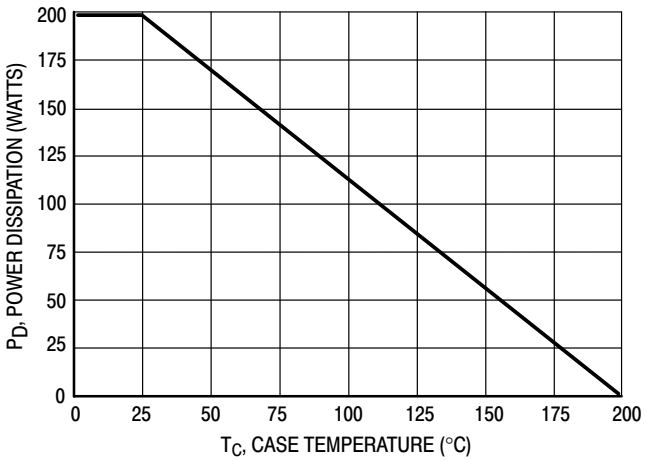
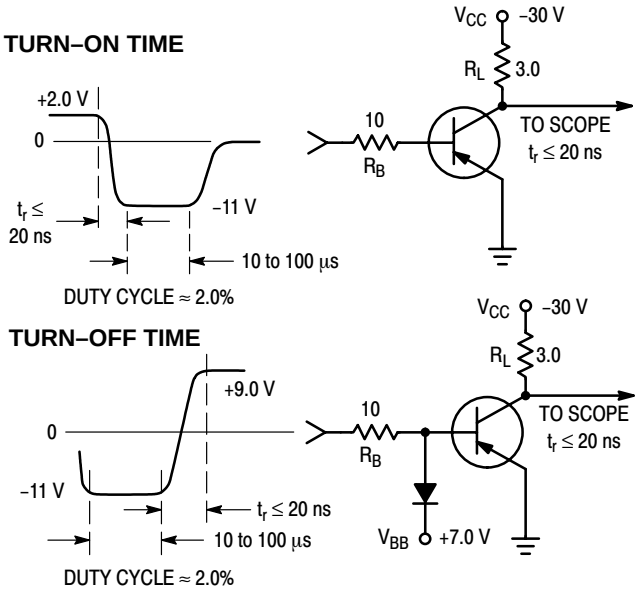


Figure 1. Power Derating



FOR CURVES OF FIGURES 3 & 6, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

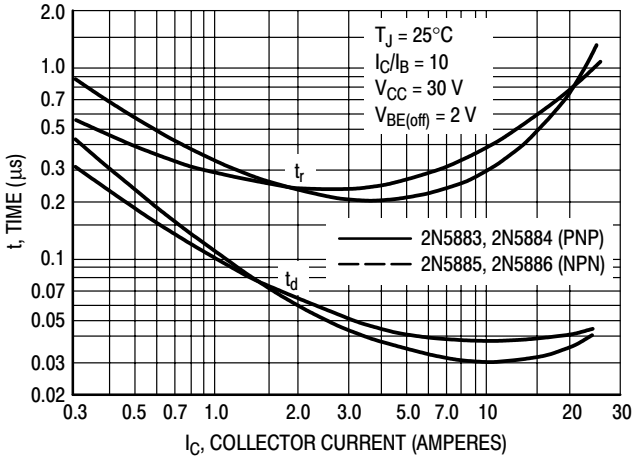


Figure 3. Turn–On Time

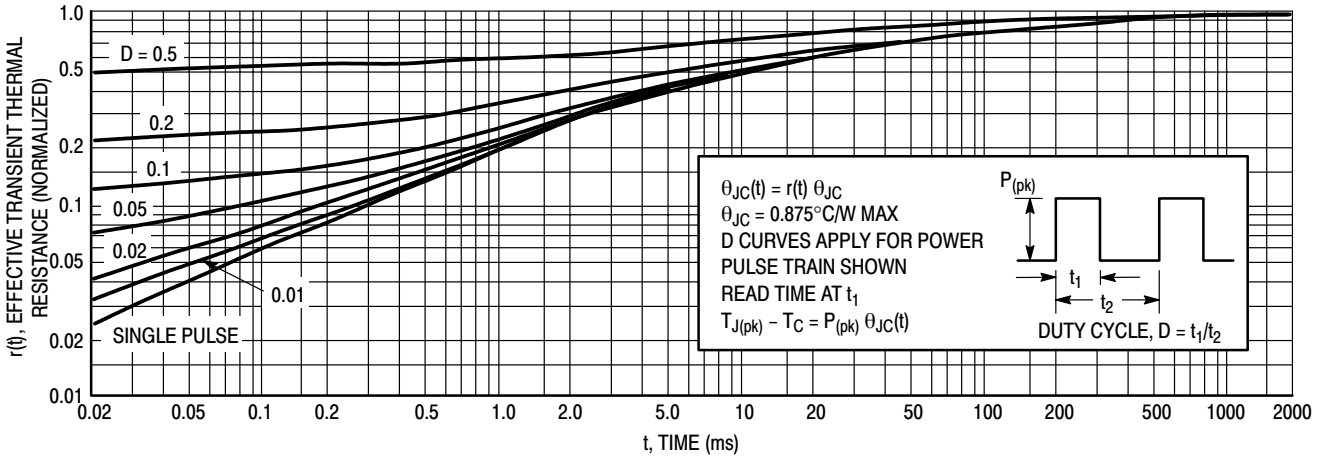


Figure 4. Thermal Response

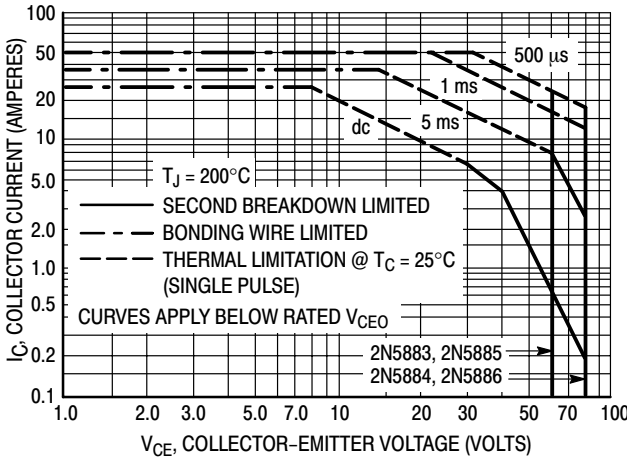


Figure 5. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

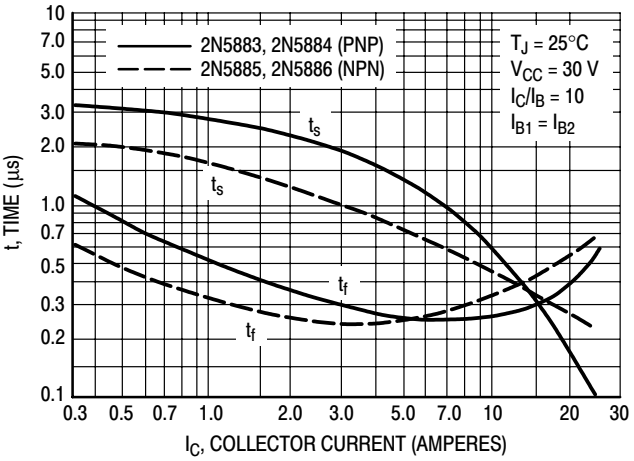


Figure 6. Turn−Off Time

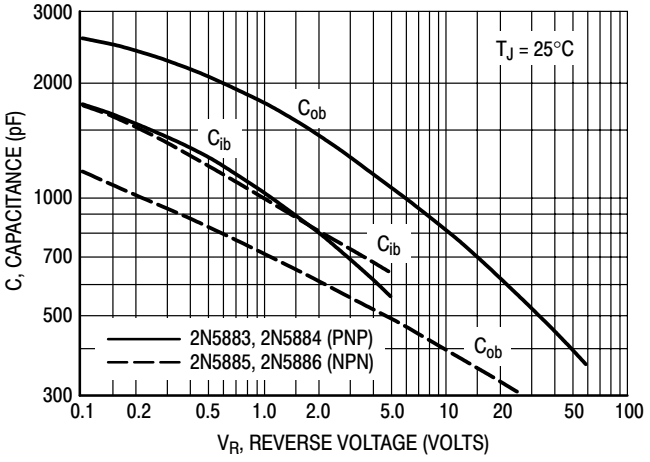


Figure 7. Capacitance

PNP DEVICES
2N5883 and 2N5884

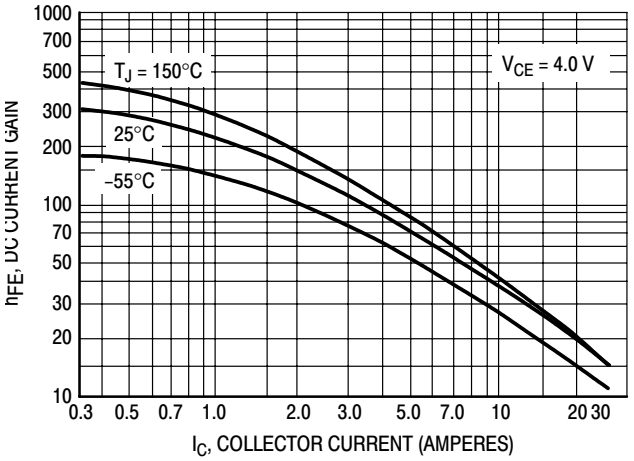


Figure 8. DC Current Gain

NPN DEVICES
2N5885 and 2N5886

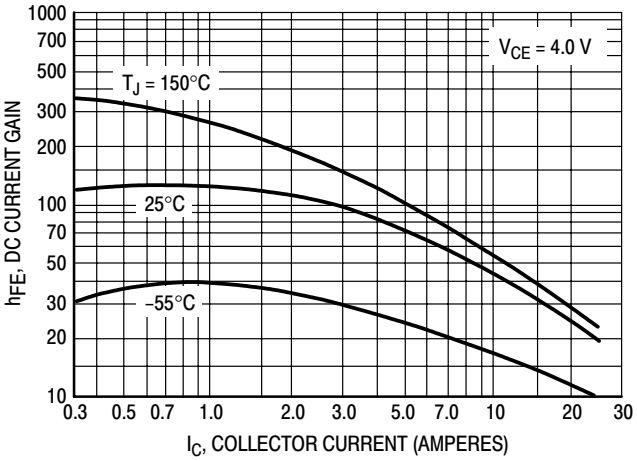


Figure 9. DC Current Gain

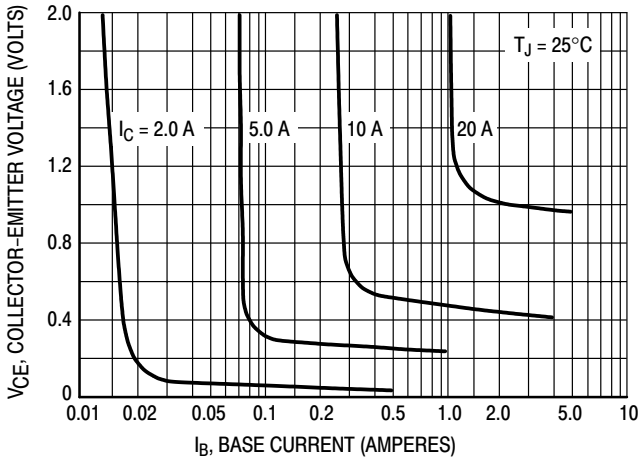


Figure 10. Collector Saturation Region

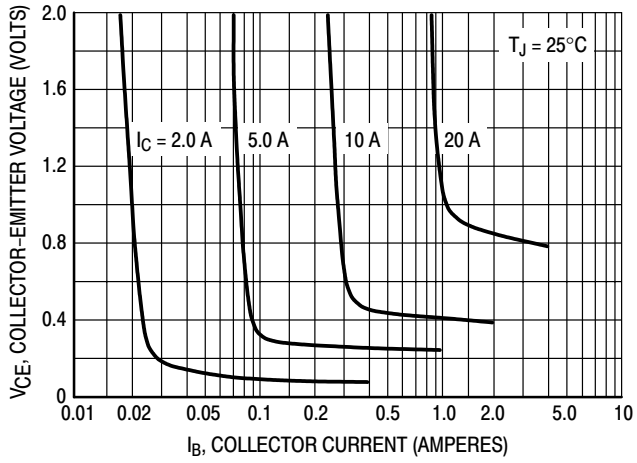


Figure 11. Collector Saturation Region

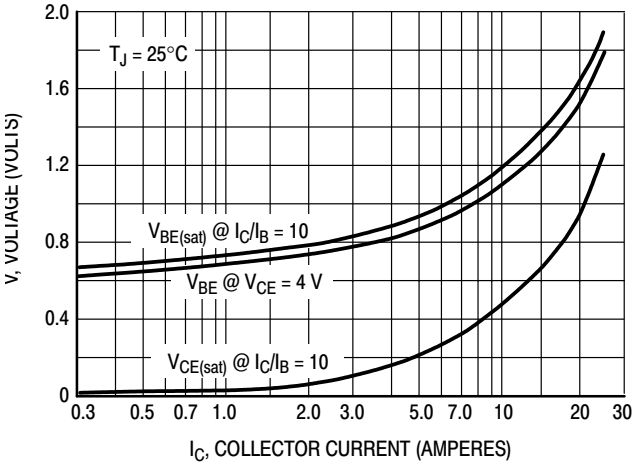


Figure 12. “On” Voltages

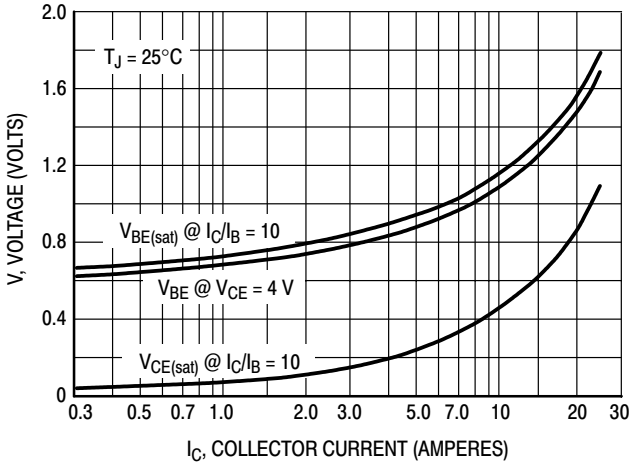
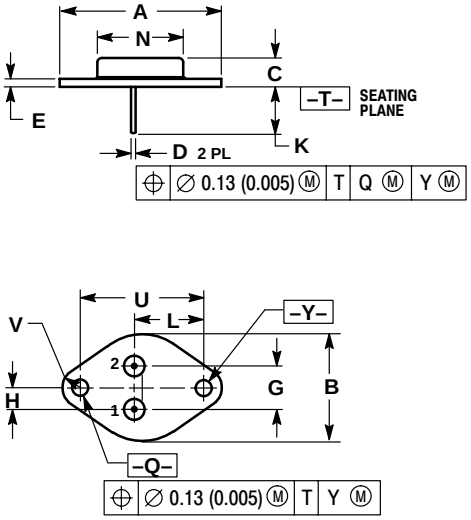


Figure 13. “On” Voltages

PACKAGE DIMENSIONS

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

Notes

PUBLICATION ORDERING INFORMATION

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