

NPN Darlington Silicon Power Transistor

... designed for general-purpose amplifier and low frequency switching applications.

- High DC Current Gain —
 $h_{FE} = 3000$ (Typ) @ $I_C = 4.0$ Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA
 $V_{CEO(sus)} = 80$ Vdc (Min)
- Low Collector–Emitter Saturation Voltage —
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ $I_C = 4.0$ Adc
 $= 3.0$ Vdc (Max) @ $I_C = 8.0$ Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

MAXIMUM RATINGS (1)

| Rating | Symbol | Max | Unit |
|--|----------------|--------------|------------------------------------|
| Collector–Emitter Voltage | V_{CEO} | 80 | Vdc |
| Collector–Base Voltage | V_{CB} | 80 | Vdc |
| Emitter–Base Voltage | V_{EB} | 5.0 | Vdc |
| Collector Current — Continuous Peak | I_C | 8.0 16 | Adc |
| Base Current | I_B | 120 | mAdc |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 100 0.571 | Watts $\text{W}/^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | –65 to +200 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--------------------------------------|-----------------|------|---------------------------|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 1.75 | $^\circ\text{C}/\text{W}$ |

(1) Indicates JEDEC Registered Data

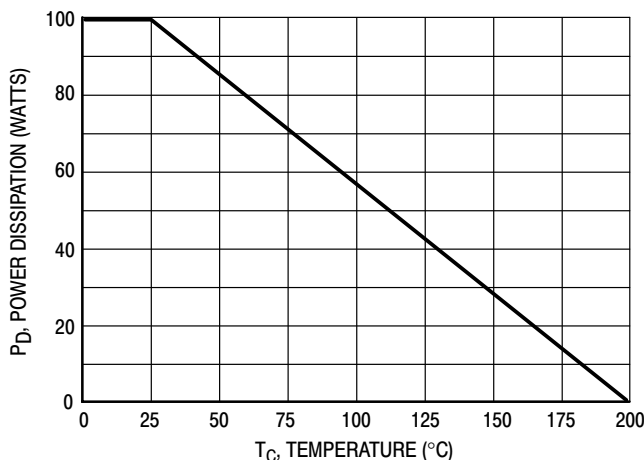
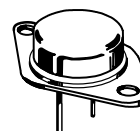


Figure 1. Power Derating

2N6056

ON Semiconductor Preferred Device

**DARLINGTON
8 AMPERE
SILICON
POWER TRANSISTOR
80 VOLTS
100 WATTS**



**CASE 1-07
TO-204AA
(TO-3)**

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

2N6056

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

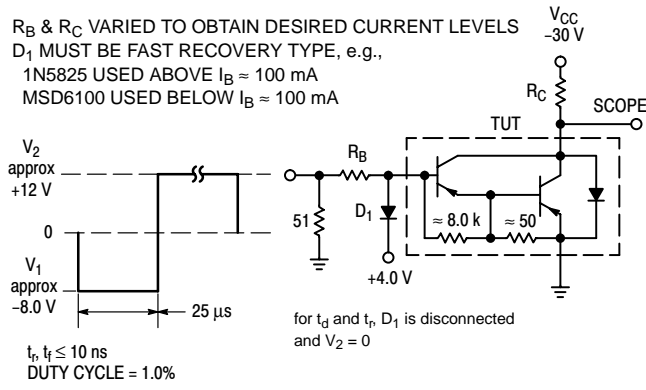
| Characteristic | Symbol | Min | Max | Unit |
|--|----------------|------------|------------|-------|
| OFF CHARACTERISTICS | | | | |
| Collector–Emitter Sustaining Voltage (2) ($I_C = 100\text{ mAdc}$, $I_B = 0$) | $V_{CEO(sus)}$ | 80 | — | Vdc |
| Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) | I_{CEO} | — | 0.5 | mA dc |
| Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 150^\circ\text{C}$) | I_{CEX} | — — | 0.5 5.0 | mA dc |
| Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$) | I_{EBO} | — | 2.0 | mA dc |
| ON CHARACTERISTICS (2) | | | | |
| DC Current Gain ($I_C = 4.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) ($I_C = 8.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) | h_{FE} | 750 100 | 18000 — | — |
| Collector–Emitter Saturation Voltage ($I_C = 4.0\text{ Adc}$, $I_B = 16\text{ mA dc}$) ($I_C = 8.0\text{ Adc}$, $I_B = 80\text{ mA dc}$) | $V_{CE(sat)}$ | — — | 2.0 3.0 | Vdc |
| Base–Emitter Saturation Voltage ($I_C = 8.0\text{ Adc}$, $I_B = 80\text{ mA dc}$) | $V_{BE(sat)}$ | — | 4.0 | Vdc |
| Base–Emitter On Voltage ($I_C = 4.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$) | $V_{BE(on)}$ | — | 2.8 | Vdc |
| DYNAMIC CHARACTERISTICS | | | | |
| Magnitude of Common Emitter Small–Signal Short Circuit Current Transfer Ratio ($I_C = 3.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$, $f = 1.0\text{ MHz}$) | $ h_{fe} $ | 4.0 | — | — |
| Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$) | C_{ob} | — | 200 | pF |
| Small–Signal Current Gain ($I_C = 3.0\text{ Adc}$, $V_{CE} = 3.0\text{ Vdc}$, $f = 1.0\text{ kHz}$) | h_{fe} | 300 | — | — |

*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2.0%

2N6056

R_B & R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
 D_1 MUST BE FAST RECOVERY TYPE, e.g.,
 1N5825 USED ABOVE $I_B \approx 100$ mA
 MSD6100 USED BELOW $I_B \approx 100$ mA



For NPN test circuit reverse diode, polarities and input pulses.

Figure 2. Switching Times Test Circuit

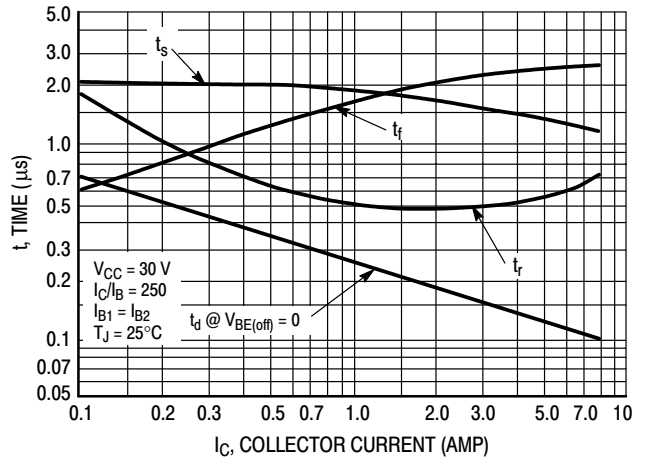


Figure 3. Switching Times

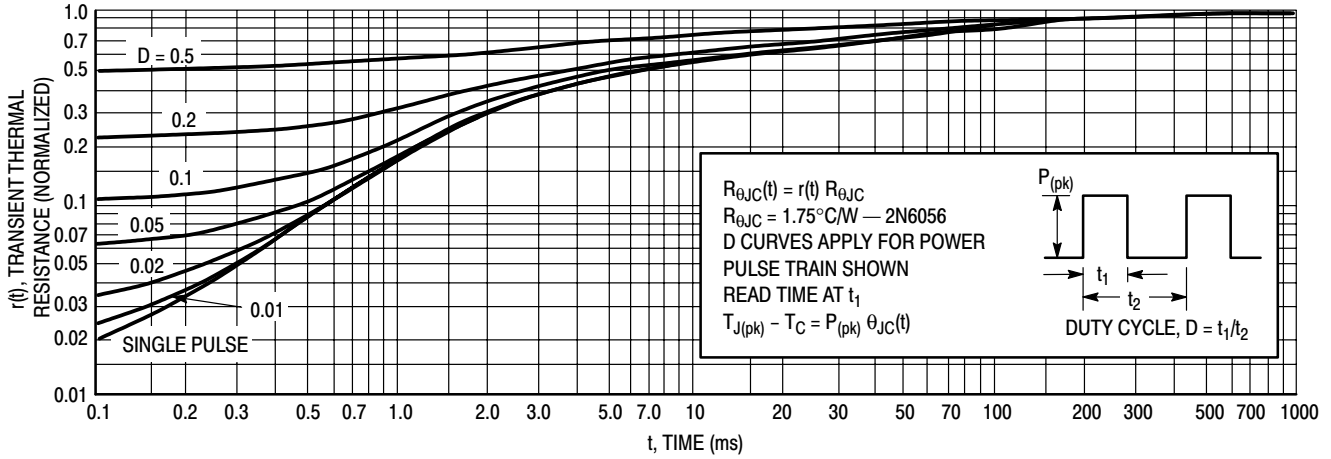


Figure 4. Thermal Response

ACTIVE-REGION SAFE OPERATING AREA

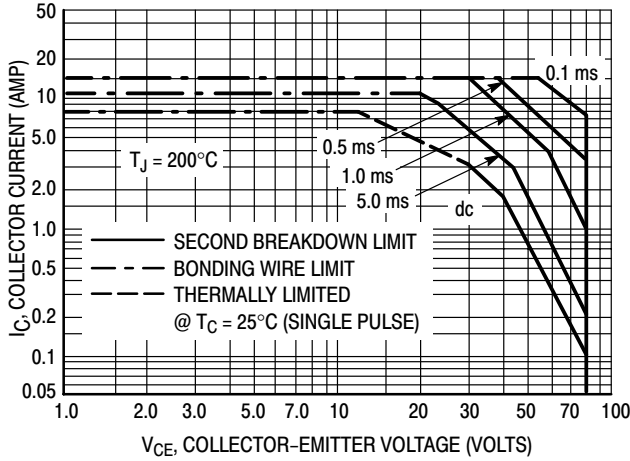


Figure 5. Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 200^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

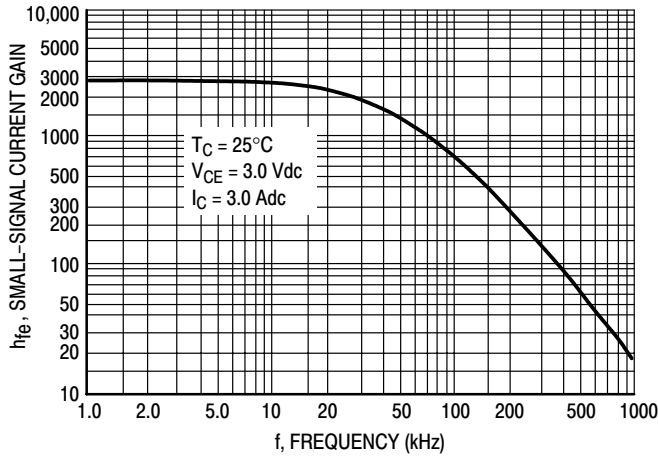


Figure 6. Small-Signal Current Gain

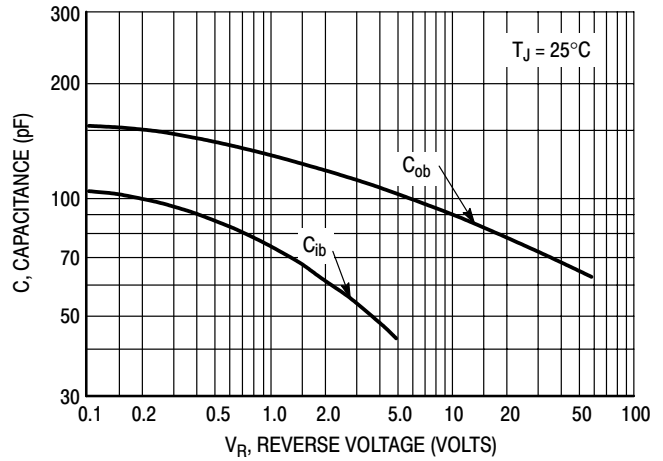


Figure 7. Capacitance

2N6056

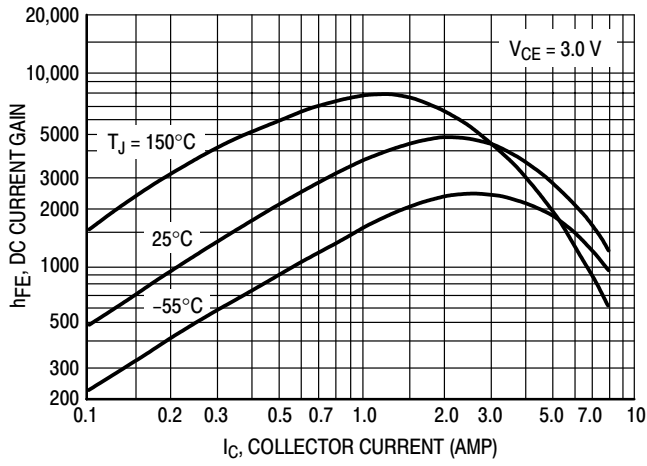


Figure 8. DC Current Gain

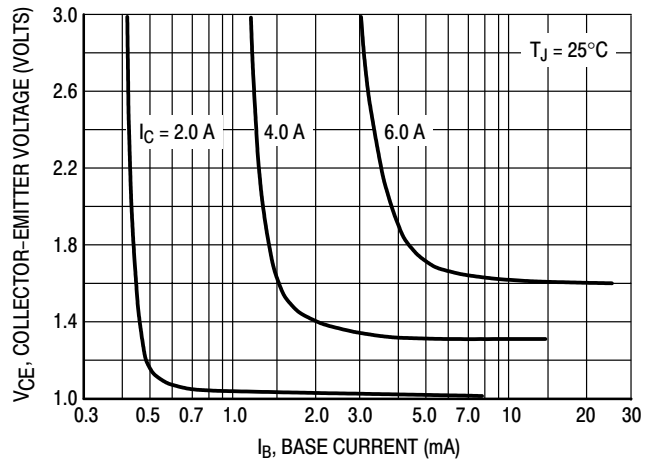


Figure 9. Collector Saturation Region

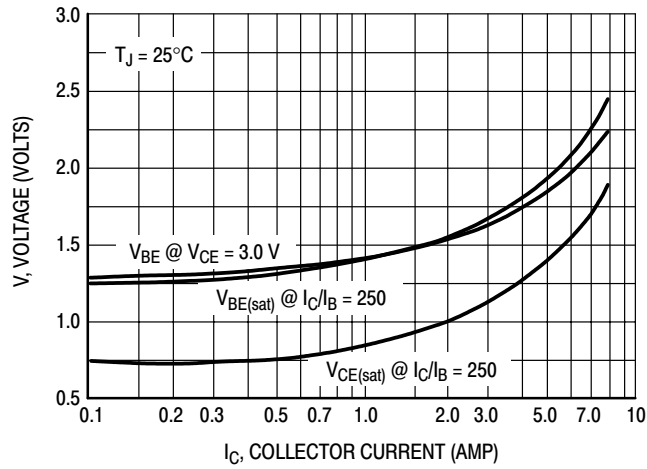
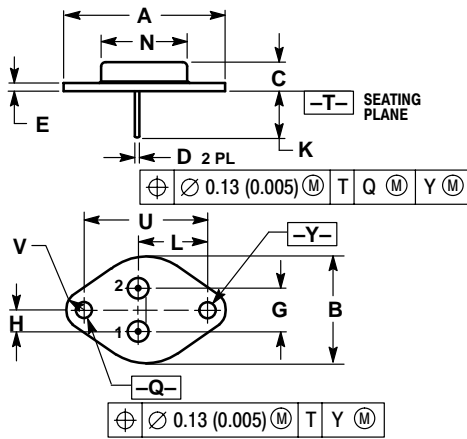


Figure 10. "On" Voltage

2N6056

PACKAGE DIMENSIONS

CASE 1-07 TO-204AA (TO-3) ISSUE Z



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.550 REF | | 39.37 REF | |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC | | 10.92 BSC | |
| H | 0.215 BSC | | 5.46 BSC | |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | 0.665 BSC | | 16.89 BSC | |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | | 30.15 BSC | |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

STYLE 1:

- PIN 1: BASE
- 2: EMITTER
- CASE: COLLECTOR

Notes

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