

2N6344A, 2N6348A, 2N6349A

Preferred Device

Triacs

Silicon Bidirectional Thyristors

Designed primarily for full-wave ac control applications, such as light dimmers, motor controls, heating controls and power supplies; or wherever full-wave silicon gate controlled solid-state devices are needed. Triac type thyristors switch from a blocking to a conducting state for either polarity of applied anode voltage with positive or negative gate triggering.

- Blocking Voltage to 800 Volts
- All Diffused and Glass Passivated Junctions for Greater Parameter Uniformity and Stability
- Small, Rugged, Thermowatt Construction for Low Thermal Resistance, High Heat Dissipation and Durability
- Gate Triggering Guaranteed in all Four Quadrants
- For 400 Hz Operation, Consult Factory
- 8 Ampere Devices Available as 2N6344 thru 2N6349
- Device Marking: Logo, Device Type, e.g., 2N6344A, Date Code

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
*Peak Repetitive Off-State Voltage(Note 1) (Gate Open, $T_J = -40$ to $+110^\circ\text{C}$, Sine Wave 50 to 60 Hz, Gate Open) 2N6344A, 2N6348A 2N6349A	V_{DRM} , V_{RRM}	600 800	Volts
*On-State RMS Current (Full Cycle Sine Wave 50 to 60 Hz) ($T_C = +80^\circ\text{C}$) ($T_C = +95^\circ\text{C}$)	$I_{\text{T(RMS)}}$	12 6.0	A
*Peak Non-repetitive Surge Current (One Full Cycle, 60 Hz, $T_C = +80^\circ\text{C}$) Preceded and followed by rated current	I_{TSM}	100	A
Circuit Fusing Consideration ($t = 8.3$ ms)	I^2t	59	A^2s
*Peak Gate Power ($T_C = +80^\circ\text{C}$, Pulse Width = 2.0 μs)	P_{GM}	20	Watts
*Average Gate Power ($T_C = +80^\circ\text{C}$, $t = 8.3$ ms)	$P_{\text{G(AV)}}$	0.5	Watt
*Peak Gate Current (Pulse Width = 2.0 μs ; $T_C = +80^\circ\text{C}$)	I_{GM}	2.0	A
*Peak Gate Voltage (Pulse Width = 2.0 μs ; $T_C = +80^\circ\text{C}$)	V_{GM}	± 10	Volts
*Operating Junction Temperature Range	T_J	-40 to $+125$	$^\circ\text{C}$
*Storage Temperature Range	T_{stg}	-40 to $+150$	$^\circ\text{C}$

*Indicates JEDEC Registered Data.

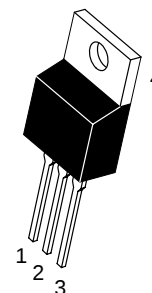
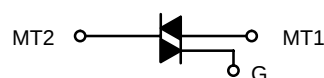
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



ON Semiconductor®

<http://onsemi.com>

TRIACS 12 AMPERES RMS 600 thru 800 VOLTS



TO-220AB
CASE 221A
STYLE 4

PIN ASSIGNMENT

	PIN ASSIGNMENT
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

ORDERING INFORMATION

Device	Package	Shipping
2N6344A	TO220AB	500/Box
2N6348A	TO220AB	500/Box
2N6349A	TO220AB	500/Box

Preferred devices are recommended choices for future use and best overall value.

2N6344A, 2N6348A, 2N6349A

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted; Electricals apply in either direction)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

*Peak Repetitive Blocking Current ($V_D = \text{Rated } V_{DRM}, V_{RRM}$; Gate Open)	I_{DRM}, I_{RRM}	—	—	10	μA
		—	—	2.0	mA

ON CHARACTERISTICS

*Peak On-State Voltage ($I_{TM} = \pm 17 \text{ A Peak}$; Pulse Width = 1 to 2 ms, Duty Cycle $\leq 2\%$)	V_{TM}	—	1.3	1.75	Volts
Gate Trigger Current (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 100 \text{ Ohms}$)	I_{GT}	—	6.0	50	mA
Quadrant I: MT2(+), G(+) All					
Quadrant II: MT2(+), G(−) 2N6348A and 2N6349A only					
Quadrant III: MT2(−), G(−) All					
Quadrant IV: MT2(−), G(+) 2N6348A and 2N6349A only					
*MT2(+), G(+); MT2(−), G(−) $T_C = -40^\circ\text{C}$					
*MT2(+), G(−); MT2(−), G(+) $T_C = -40^\circ\text{C}$					
Gate Trigger Voltage (Continuous dc) ($V_D = 12 \text{ Vdc}$, $R_L = 100 \text{ ohms}$)	V_{GT}	—	0.9	2.0	Volts
Quadrant I: MT2(+), G(+) All					
Quadrant II: MT2(+), G(−) 2N6348A and 2N6349A only					
Quadrant III: MT2(−), G(−) All					
Quadrant IV: MT2(−), G(+) 2N6348A and 2N6349A only					
*MT2(+), G(+); MT2(−), G(−) $T_C = -40^\circ\text{C}$					
*MT2(+), G(−); MT2(−), G(+) $T_C = -40^\circ\text{C}$					
Gate Non-Trigger Voltage ($V_D = \text{Rated } V_{DRM}$, $R_L = 10 \text{ k ohms}$, $T_J = 110^\circ\text{C}$)	V_{GD}	0.2	—	—	Volts
*MT2(+), G(+); MT2(−), G(−); MT2(+), G(−); MT2(−), G(+)					
Holding Current ($V_D = 12 \text{ Vdc}$, Gate Open)	I_H	—	6.0	40	mA
Initiating Current = $\pm 200 \text{ mA}$					
*Turn-On Time ($V_D = \text{Rated } V_{DRM}$, $I_{TM} = 17 \text{ A}$, $I_{GT} = 120 \text{ mA}$, Rise Time = $0.1 \mu\text{s}$, Pulse Width = $2 \mu\text{s}$)	t_{gt}	—	1.5	2.0	μs

DYNAMIC CHARACTERISTICS

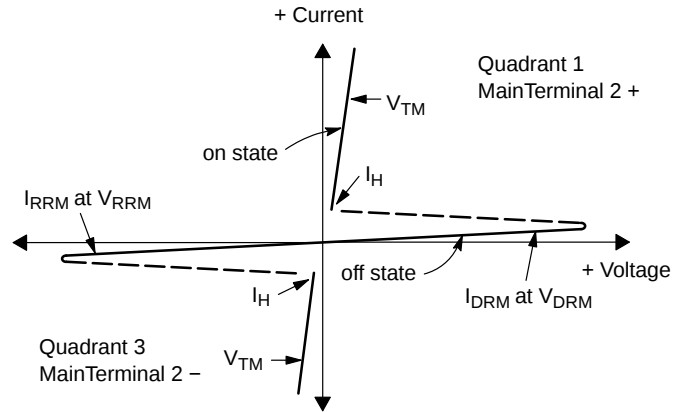
Critical Rate of Rise of Commutation Voltage ($V_D = \text{Rated } V_{DRM}$, $I_{TM} = 17 \text{ A}$, Commutating $di/dt = 6.1 \text{ A/ms}$, Gate Unenergized, $T_C = 80^\circ\text{C}$)	$dv/dt(c)$	—	5.0	—	V/ μs
--	------------	---	-----	---	------------------

*Indicates JEDEC Registered Data.

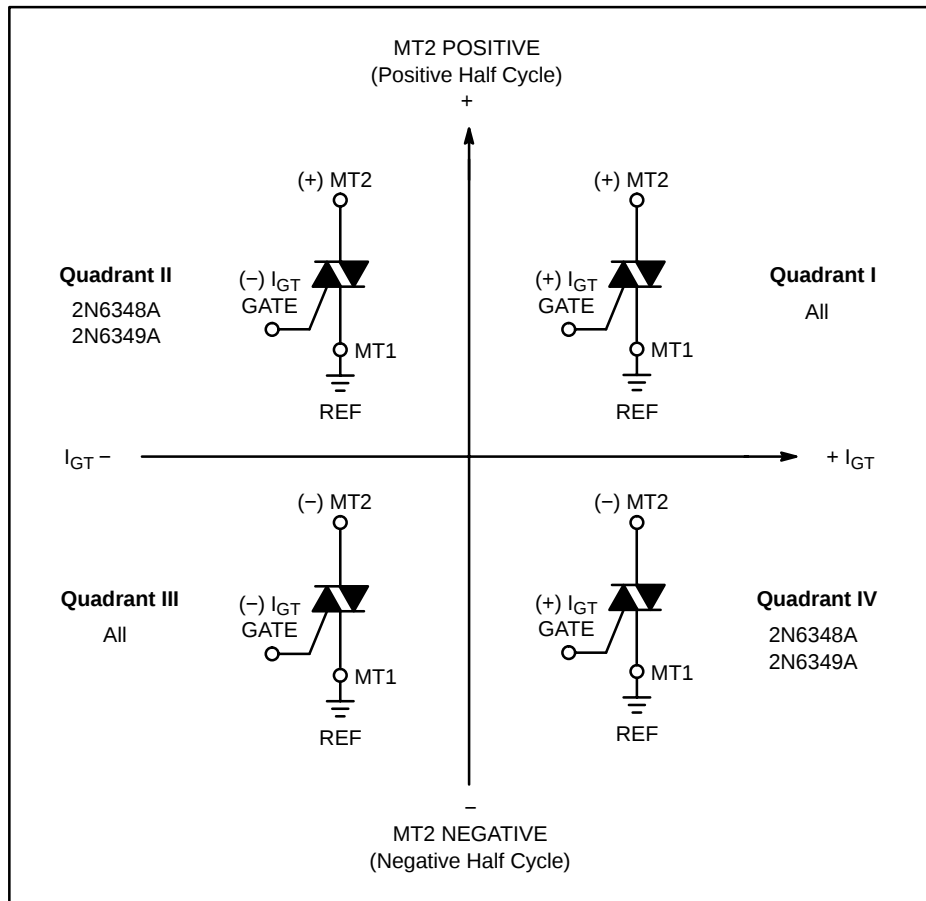
2N6344A, 2N6348A, 2N6349A

Voltage Current Characteristic of Triacs (Bidirectional Device)

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.

With in-phase signals (using standard AC lines) quadrants I and III are used.

2N6344A, 2N6348A, 2N6349A

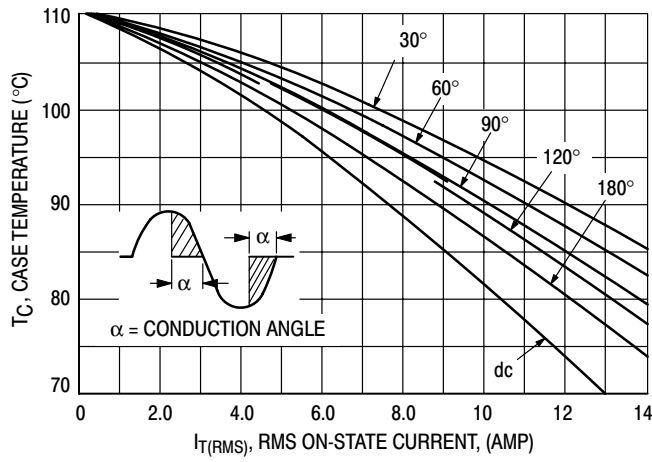


Figure 1. RMS Current Derating

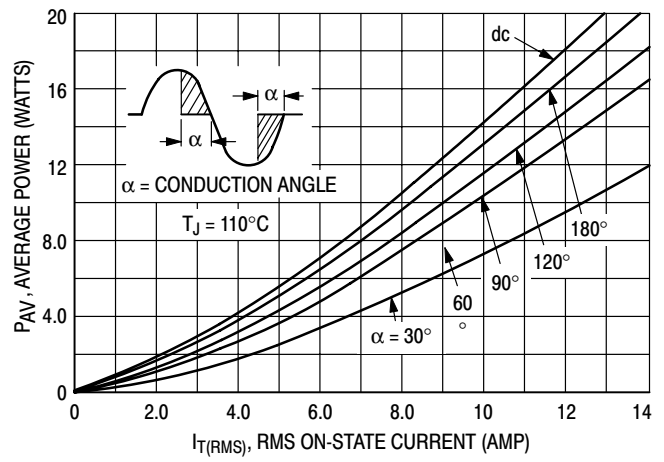


Figure 2. On-State Power Dissipation

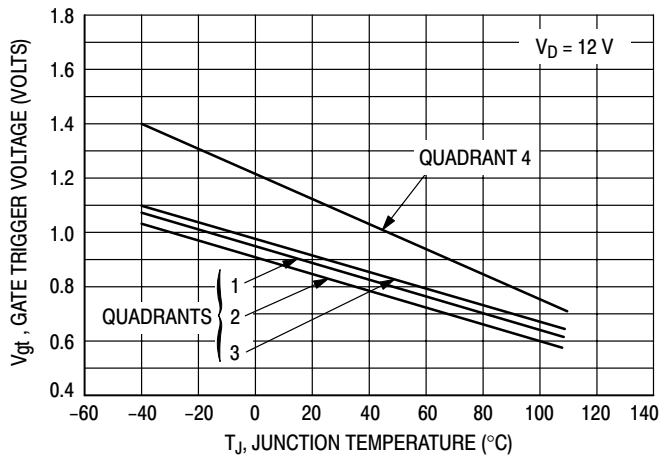


Figure 3. Typical Gate Trigger Voltage

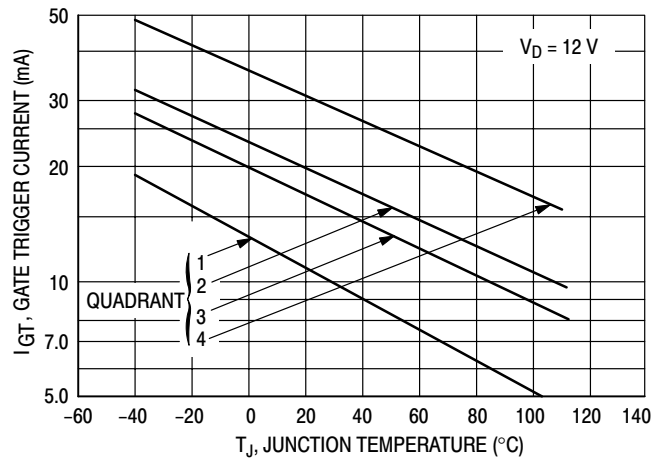


Figure 4. Typical Gate Trigger Current

2N6344A, 2N6348A, 2N6349A

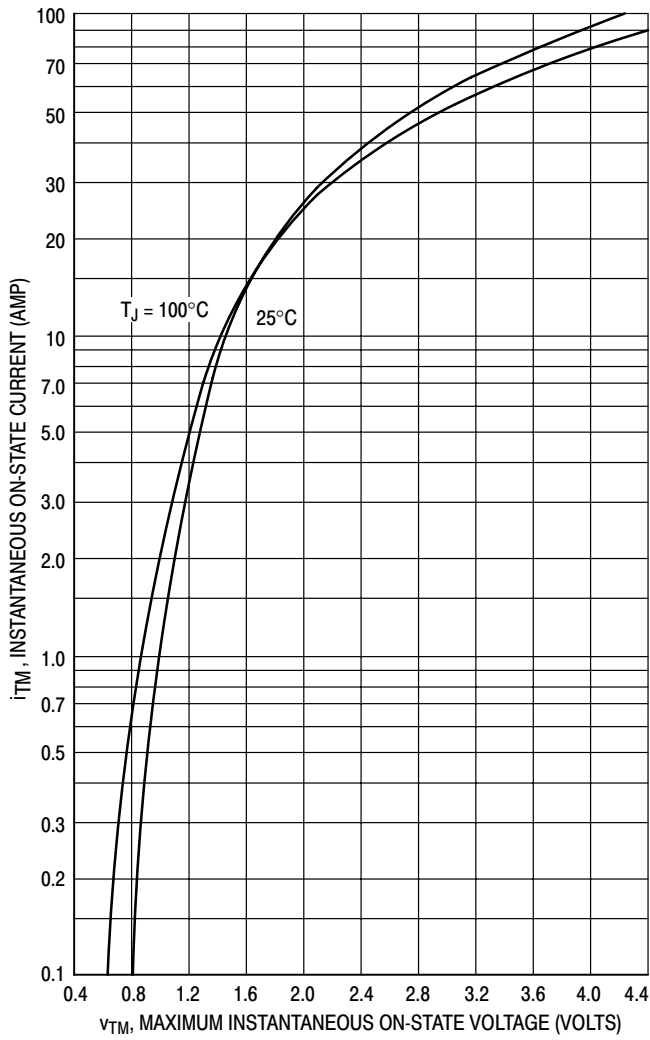


Figure 5. On-State Characteristics

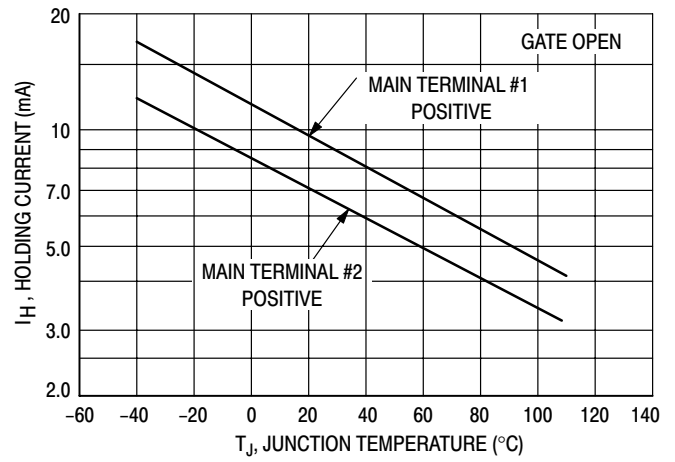


Figure 6. Typical Holding Current

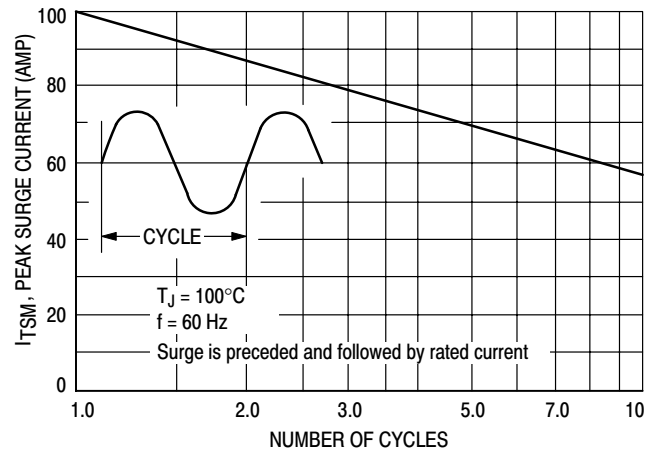


Figure 7. Maximum Non-Repetitive Surge Current

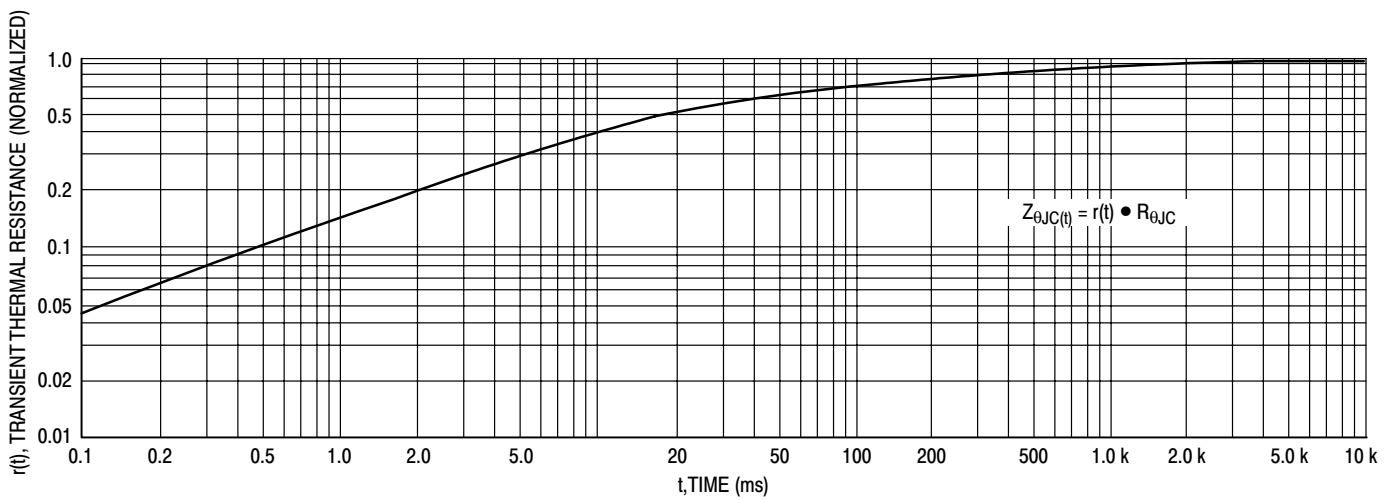
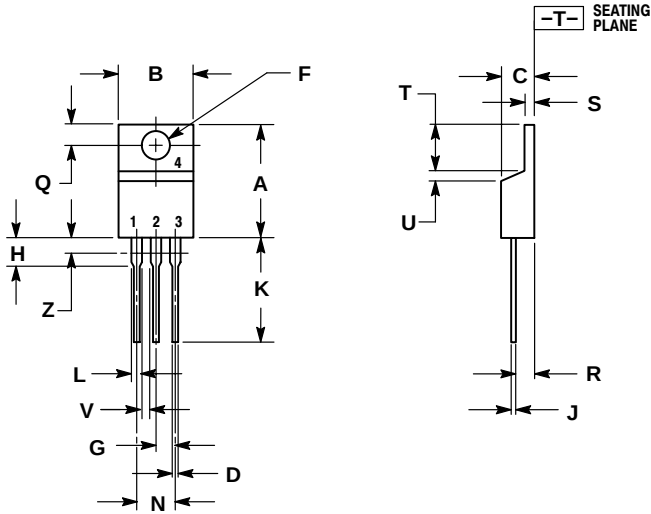


Figure 8. Typical Thermal Response

2N6344A, 2N6348A, 2N6349A

PACKAGE DIMENSIONS

TO-220AB
CASE 221A-07
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 4:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your
local Sales Representative.