

# SN74LS273

## Octal D Flip-Flop with Clear

The SN74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-Bit High Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

### GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.75	5.0	5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	0	25	70	°C
I <sub>OH</sub>	Output Current – High			–0.4	mA
I <sub>OL</sub>	Output Current – Low			8.0	mA

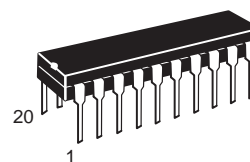


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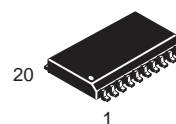
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**LOW  
POWER  
SCHOTTKY**



**PLASTIC  
N SUFFIX  
CASE 738**



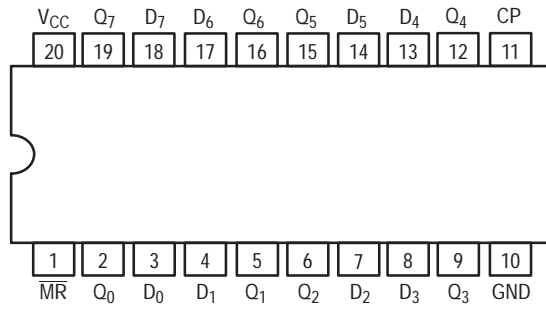
**SOIC  
DW SUFFIX  
CASE 751D**

### ORDERING INFORMATION

Device	Package	Shipping
SN74LS273N	16 Pin DIP	1440 Units/Box
SN74LS273DW	16 Pin	2500/Tape & Reel

# SN74LS273

## CONNECTION DIAGRAM DIP (TOP VIEW)



### PIN NAMES

CP	Clock (Active HIGH Going Edge) Input
D <sub>0</sub> – D <sub>7</sub>	Data Inputs
MR	Master Reset (Active LOW) Input
Q <sub>0</sub> – Q <sub>7</sub>	Register Outputs

### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 U.L.

### NOTES:

a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

## TRUTH TABLE

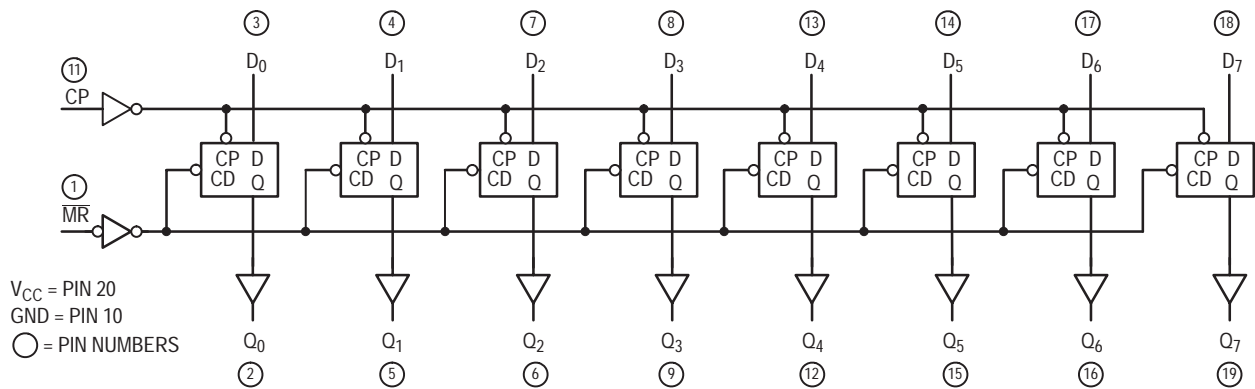
MR	CP	D <sub>x</sub>	Q <sub>x</sub>
L	X	X	L
H	⬆	H	H
H	⬆	L	L

H = HIGH Logic Level

L = LOW Logic Level

X = Immaterial

## LOGIC DIAGRAM



# SN74LS273

## FUNCTIONAL DESCRIPTION

The SN74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the  $\overline{MR}$  input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the

setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$V_{IH}$	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
$V_{IL}$	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{IK}$	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$ , $I_{IN} = -18 \text{ mA}$
$V_{OH}$	Output HIGH Voltage	2.7	3.5		V	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table
$V_{OL}$	Output LOW Voltage		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$
			0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
$I_{IH}$	Input HIGH Current			20	$\mu\text{A}$	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7 \text{ V}$
				0.1	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 7.0 \text{ V}$
$I_{IL}$	Input LOW Current			-0.4	mA	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.4 \text{ V}$
$I_{OS}$	Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$
$I_{CC}$	Power Supply Current			27	mA	$V_{CC} = \text{MAX}$

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

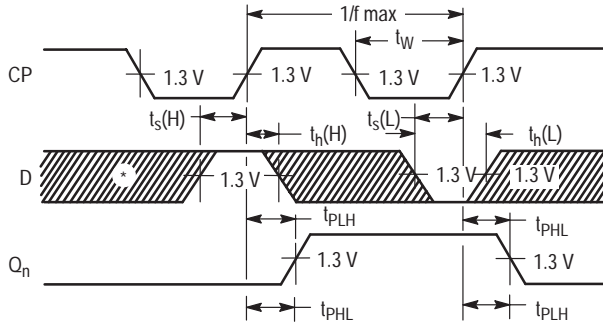
## AC CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$f_{MAX}$	Maximum Input Clock Frequency	30	40		MHz	Figure 1
$t_{PHL}$	Propagation Delay, $\overline{MR}$ to Q Output		18	27	ns	Figure 2
$t_{PLH}$ $t_{PHL}$	Propagation Delay, Clock to Output		17 18	27 27	ns	Figure 1

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
$t_w$	Pulse Width, Clock or Clear	20			ns	Figure 1
$t_s$	Data Setup Time	20			ns	Figure 1
$t_h$	Hold Time	5.0			ns	Figure 1
$t_{rec}$	Recovery Time	25			ns	Figure 2

AC WAVEFORMS



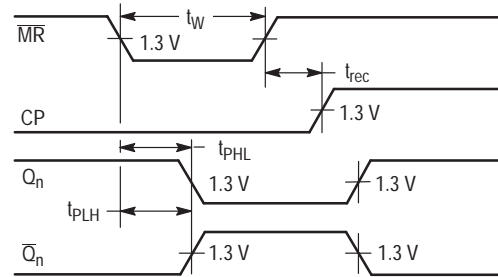
\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**

**DEFINITION OF TERMS**

**SETUP TIME ( $t_s$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_h$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

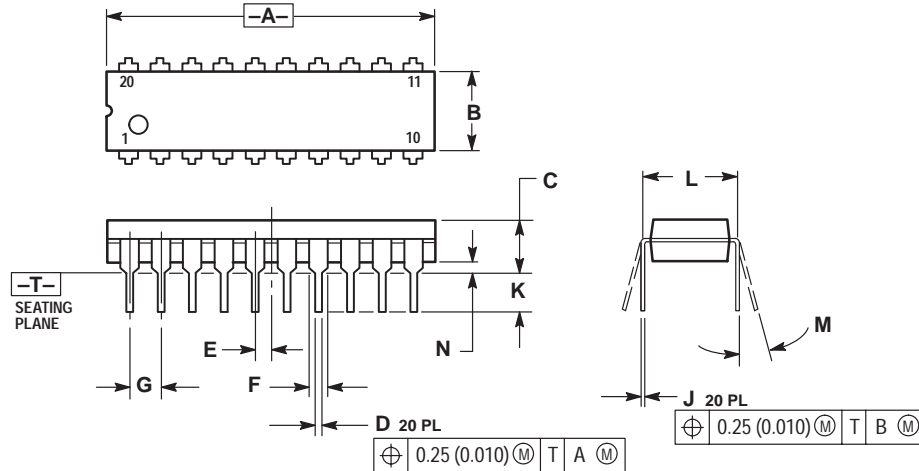
continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

# SN74LS273

## PACKAGE DIMENSIONS

**N SUFFIX**  
PLASTIC PACKAGE  
CASE 738-03  
ISSUE E



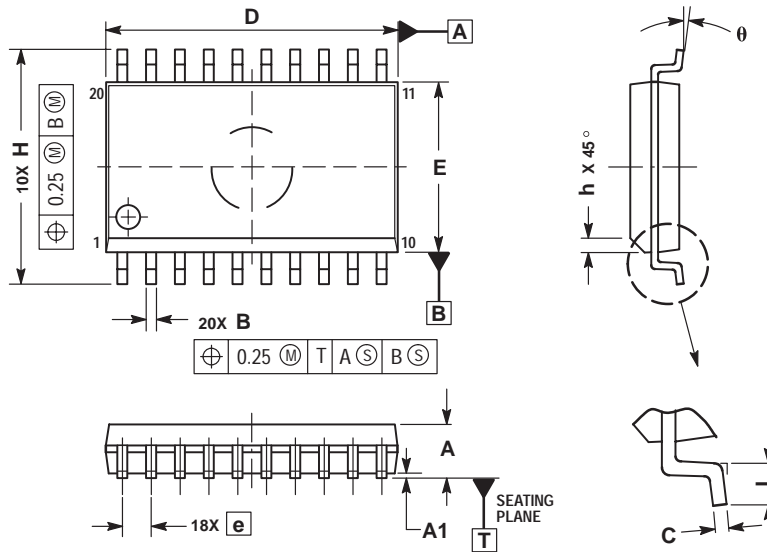
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

# SN74LS273

## D SUFFIX PLASTIC SOIC PACKAGE CASE 751D-05 ISSUE F



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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