BCP68T1

Preferred Device

NPN Silicon Epitaxial Transistor

This NPN Silicon Epitaxial Transistor is designed for use in low voltage, high current applications. The device is housed in the SOT−223−4 package, which is designed for medium power surface mount applications.

- High Current: I_C = 1.0 A
- The SOT−223−4 Package can be soldered using wave or reflow.
- SOT−223−4 package ensures level mounting, resulting in improved thermal conduction, and allows visual inspection of soldered joints. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.
- Available in 12 mm Tape and Reel
  Use BCP68T1 to order the 7 inch/1000 unit reel.
  Use BCP68T3 to order the 13 inch/4000 unit reel.
- The PNP Complement is BCP69T1
- Pb−Free Package May be Available. The G−Suffix Denotes a Pb−Free Lead Finish

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	20	Vdc
Collector−Base Voltage	V_{CBO}	25	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	1.0	Adc
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance − Junction−to−Ambient (Surface Mounted)	$R_{\theta JA}$	83.3	°C/W
Lead Temperature for Soldering, 0.0625 in from case Time in Solder Bath	T_L	260 10	°C Sec

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

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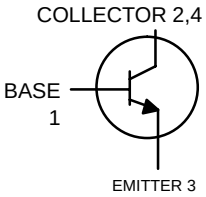
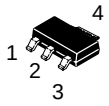
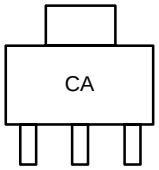
MEDIUM POWER NPN SILICON HIGH CURRENT TRANSISTOR SURFACE MOUNT





SOT−223−4 (TO−261)
CASE 318E
Style 1

MARKING DIAGRAM



CA = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
BCP68T1	SOT−223−4	1000 / Tape & Reel
BCP68T1G	SOT−223−4	1000 / Tape & Reel
BCP68T3	SOT−223−4	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CES}$	25	−	−	Vdc
Collector−Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	20	−	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	−	−	Vdc
Collector−Base Cutoff Current (V_{CB} = 25 Vdc, I_E = 0)	I_{CBO}	−	−	10	μAdc
Emitter−Base Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	−	10	μAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mAdc, V_{CE} = 10 Vdc) (I_C = 500 mAdc, V_{CE} = 1.0 Vdc) (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	h_{FE}	 50 85 60	 − − −	 − 375 −	−
Collector−Emitter Saturation Voltage (I_C = 1.0 Adc, I_B = 100 mAdc)	$V_{CE(sat)}$	−	−	0.5	Vdc
Base−Emitter On Voltage (I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	−	−	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	f_T	−	60	−	MHz

TYPICAL ELECTRICAL CHARACTERISTICS

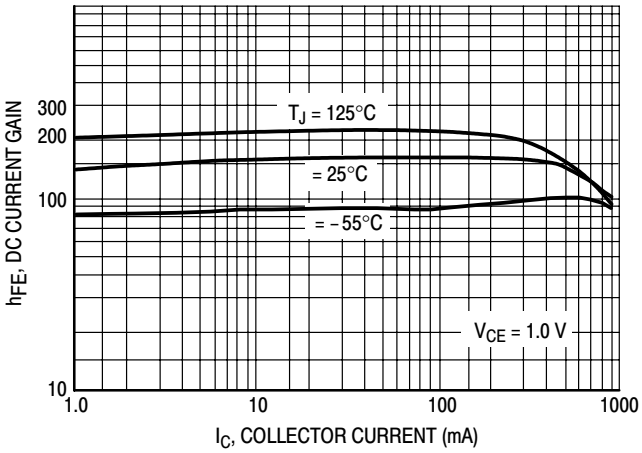


Figure 1. DC Current Gain

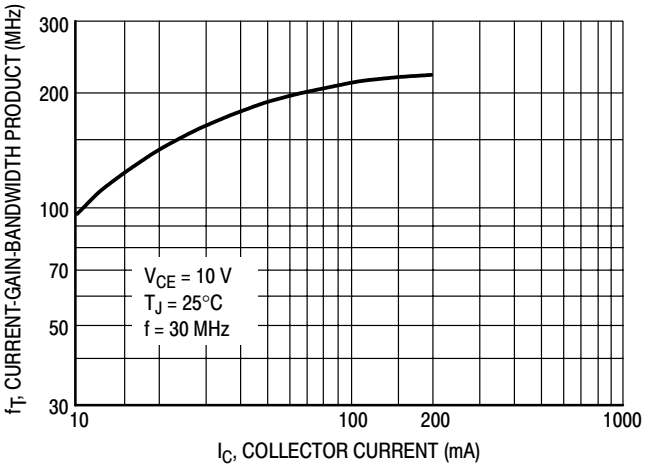


Figure 2. Current-Gain-Bandwidth Product

TYPICAL ELECTRICAL CHARACTERISTICS

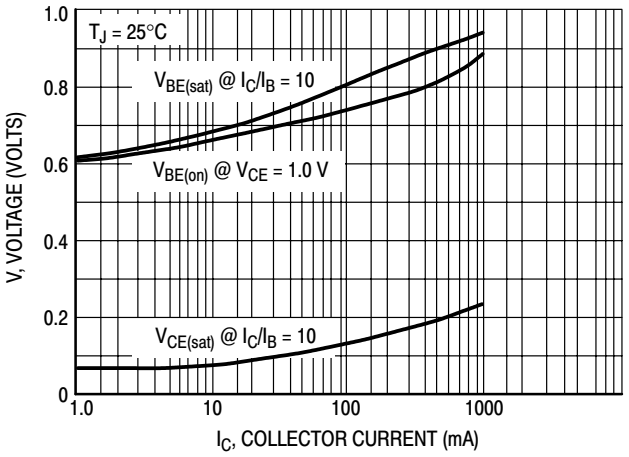


Figure 3. “On” Voltage

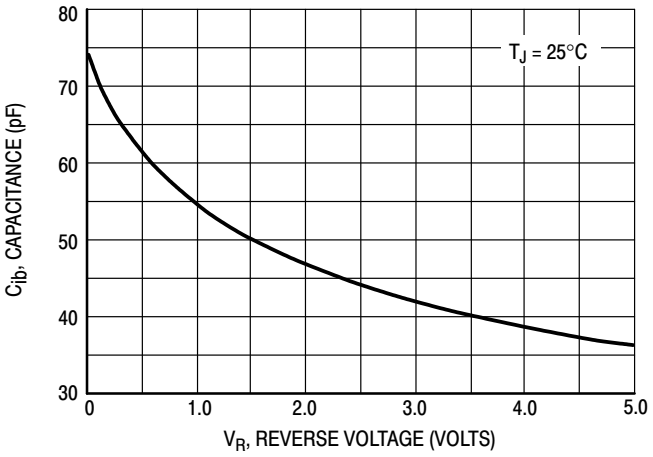


Figure 4. Capacitance

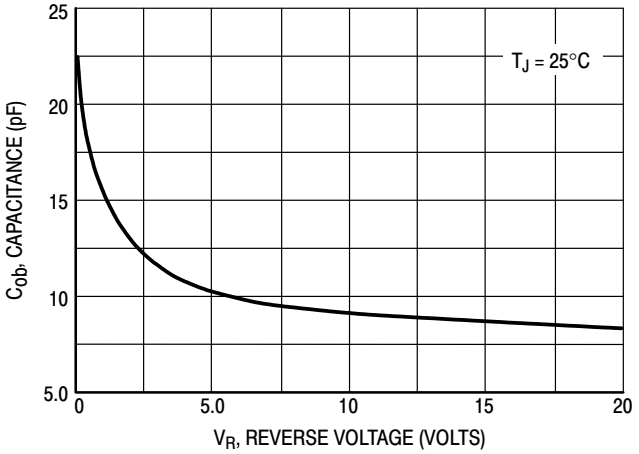


Figure 5. Capacitance

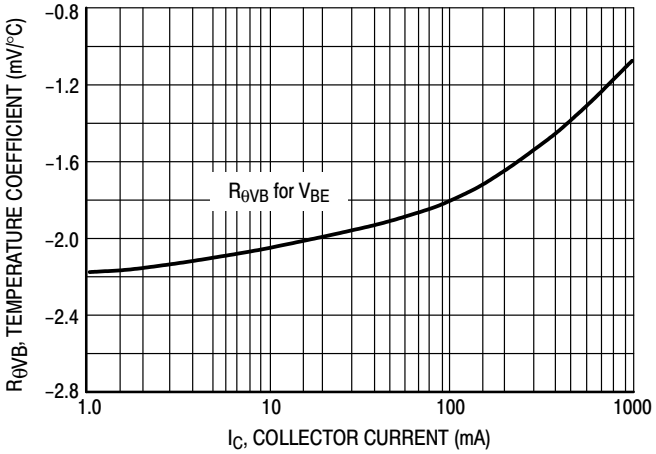


Figure 6. Base-Emitter Temperature Coefficient

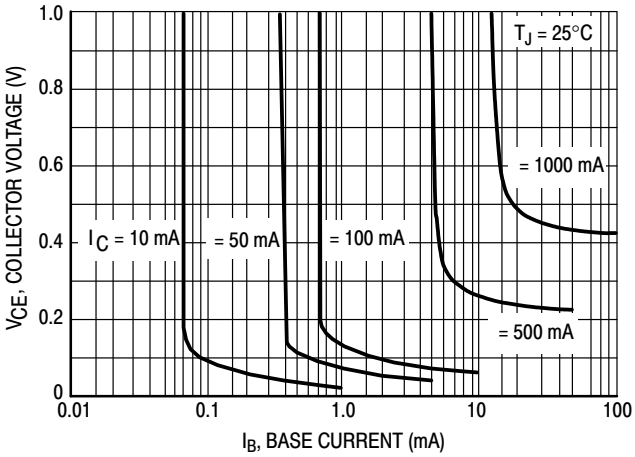
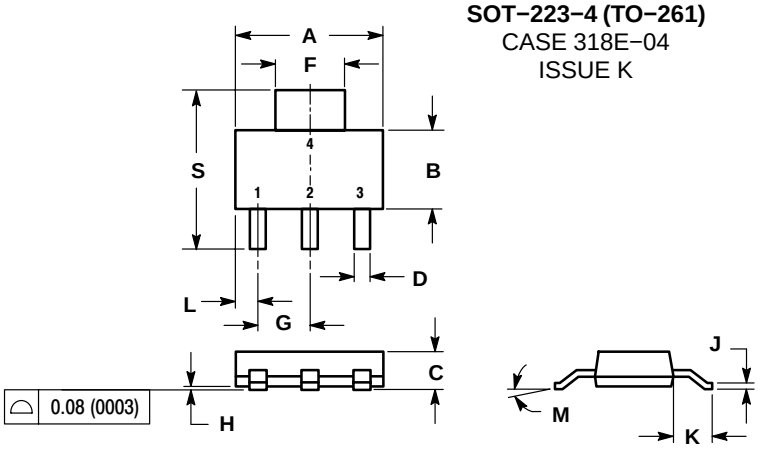


Figure 7. Saturation Region

PACKAGE DIMENSIONS

SOT−223−4 (TO−261)
CASE 318E−04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*

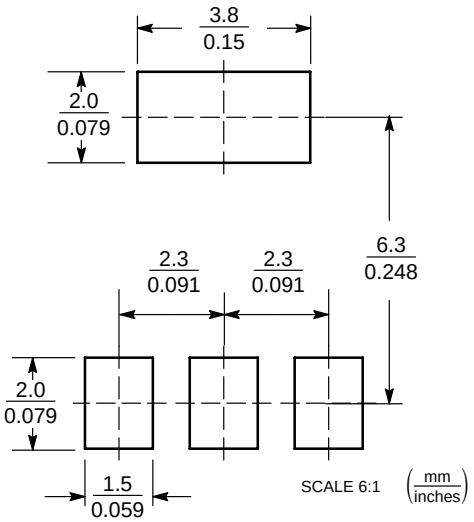


Figure 8. SOT−223

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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