

NPN Silicon Power Transistor

High Voltage SWITCHMODE™ Series

Designed for use in electronic ballast (light ballast) and in Switchmode Power supplies up to 50 Watts. Main features include:

- Improved Efficiency Due to:
 - Low Base Drive Requirements (High and Flat DC Current Gain h_{FE})
 - Low Power Losses (On-State and Switching Operations)
 - Fast Switching: $t_{fi} = 100$ ns (typ) and $t_{si} = 3.2$ μ s (typ)
 - @ $I_C = 2.0$ A, $I_{B1} = I_{B2} = 0.4$ A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot-to-Lot

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	V_{CEO}	400	Vdc
Collector-Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter-Base Voltage	V_{EBO}	9.0	Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	5.0 10	Adc
Base Current	I_B	2.0	Adc
Total Device Dissipation (T _C = 25°C) Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature	T _J , T _{stg}	– 65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.65 62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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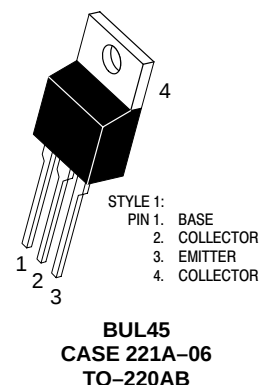
OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 100$ mA, $L = 25$ mH)	$V_{CEO(sus)}$	400	—	—	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}$, $I_B = 0$)	I_{CEO}	—	—	100	μ Adc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CES}$, $V_{EB} = 0$) (T _C = 125°C)	I_{CES}	—	—	10 100	μ Adc
Emitter Cutoff Current ($V_{EB} = 9.0$ Vdc, $I_C = 0$)	I_{EBO}	—	—	100	μ Adc

(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle $\leq$ 10%.

BUL45

POWER TRANSISTOR
5.0 AMPERES
700 VOLTS
35 and 75 WATTS



BUL45

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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ON CHARACTERISTICS

Base–Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 2.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$)	$V_{BE(\text{sat})}$	— —	0.84 0.89	1.2 1.25	Vdc
Collector–Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($T_C = 125^\circ\text{C}$)	$V_{CE(\text{sat})}$	— —	0.175 0.150	0.25 —	Vdc
Collector–Emitter Saturation Voltage ($I_C = 2.0\text{ Adc}$, $I_B = 0.4\text{ Adc}$) ($T_C = 125^\circ\text{C}$)	$V_{CE(\text{sat})}$	— —	0.25 0.275	0.4 —	Vdc
DC Current Gain ($I_C = 0.3\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($T_C = 125^\circ\text{C}$) ($I_C = 2.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$) ($T_C = 125^\circ\text{C}$) ($I_C = 10\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$) ($T_C = 125^\circ\text{C}$)	h_{FE}	14 — 7.0 5.0 10	— 32 14 12 22	34 — — — —	—

DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1.0\text{ MHz}$)				f_T	—	12	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)				C_{ob}	—	50	75	pF
Input Capacitance ($V_{EB} = 8.0\text{ Vdc}$)				C_{ib}	—	920	1200	pF
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I_{B1} reaches 90% of final I_{B1} (see Figure 18)	($I_C = 1.0\text{ Adc}$ $I_{B1} = 100\text{ mAdc}$ $V_{CC} = 300\text{ V}$)	1.0 μs	($T_C = 125^\circ\text{C}$)	V_{CE} (Dyn sat)	— —	1.75 4.4	— —	Vdc
		3.0 μs	($T_C = 125^\circ\text{C}$)		— —	0.5 1.0	— —	
	($I_C = 2.0\text{ Adc}$ $I_{B1} = 400\text{ mAdc}$ $V_{CC} = 300\text{ V}$)	1.0 μs	($T_C = 125^\circ\text{C}$)		— —	1.85 6.0	— —	
		3.0 μs	($T_C = 125^\circ\text{C}$)		— —	0.5 1.0	— —	

BUL45

SWITCHING CHARACTERISTICS: Resistive Load

Turn-On Time	(I _C = 2.0 Adc, I _{B1} = I _{B2} = 0.4 Adc Pulse Width = 20 μs, Duty Cycle < 20% V _{CC} = 300 V) (T _C = 125°C)	t _{on}	— —	75 120	110 —	ns
Turn-Off Time		t _{off}	— —	2.8 3.5	3.5 —	μs

SWITCHING CHARACTERISTICS: Inductive Load (V_{CC} = 15 Vdc, L_C = 200 μH, V_{clamp} = 300 Vdc)

Fall Time	(I _C = 2.0 Adc, I _{B1} = 0.4 Adc I _{B2} = 0.4 Adc) (T _C = 125°C)	t _{fi}	70 —	— 200	170 —	ns
Storage Time		t _{si}	2.6 —	— 4.2	3.8 —	μs
Crossover Time		t _c	— —	230 400	350 —	ns
Fall Time	(I _C = 1.0 Adc, I _{B1} = 100 mAdc I _{B2} = 0.5 Adc) (T _C = 125°C)	t _{fi}	— —	110 100	150 —	ns
Storage Time		t _{si}	— —	1.1 1.5	1.7 —	μs
Crossover Time		t _c	— —	170 170	250 —	ns
Fall Time	(I _C = 2.0 Adc, I _{B1} = 250 mAdc I _{B2} = 2.0 Adc) (T _C = 125°C)	t _{fi}	—	80	120	ns
Storage Time		t _{si}	—	0.6	0.9	μs
Crossover Time		t _c	—	175	300	ns

TYPICAL STATIC CHARACTERISTICS

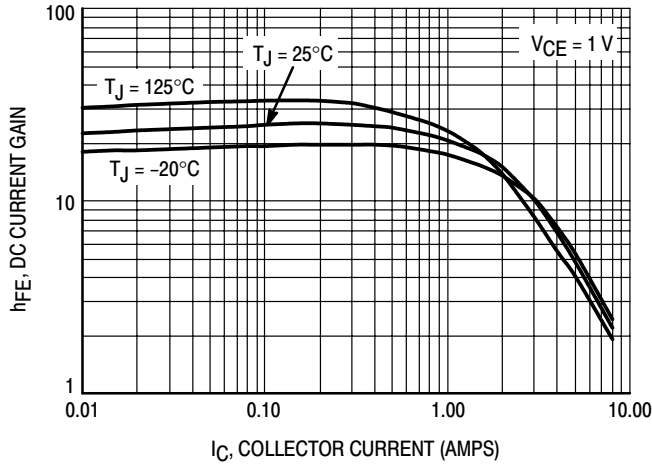


Figure 1. DC Current Gain @ 1 Volt

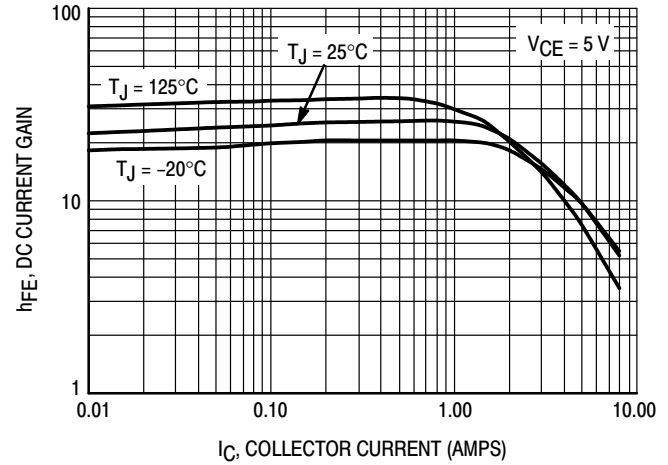


Figure 2. DC Current Gain at @ 5 Volts

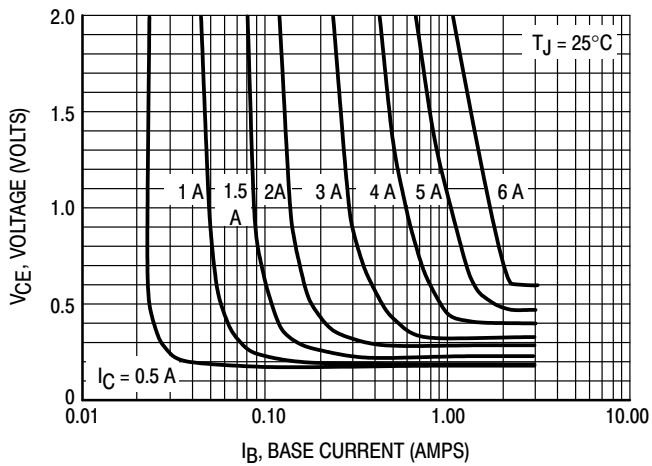


Figure 3. Collector-Emitter Saturation Region

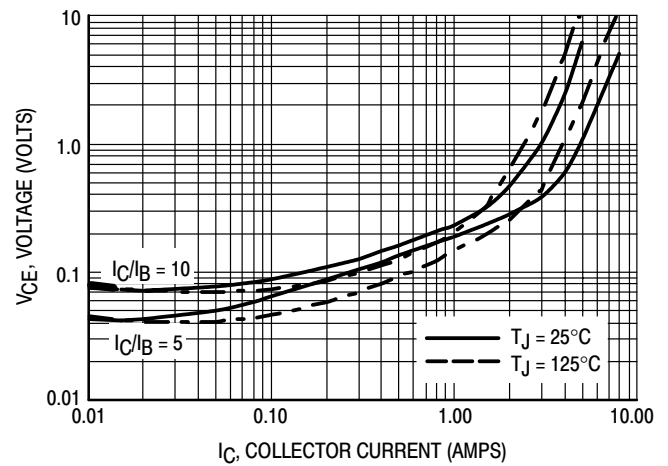


Figure 4. Collector-Emitter Saturation Voltage

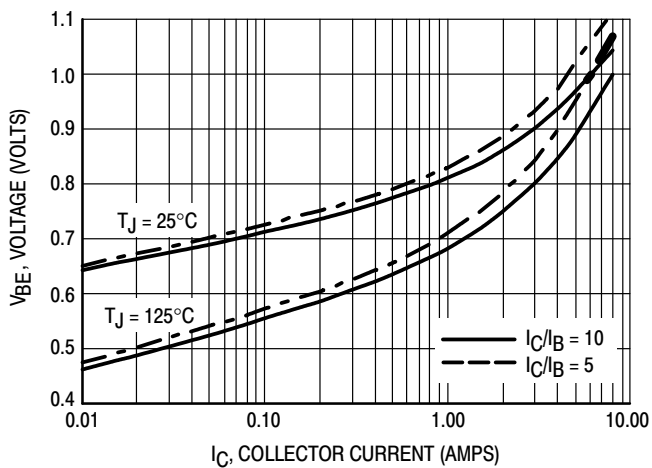


Figure 5. Base-Emitter Saturation Region

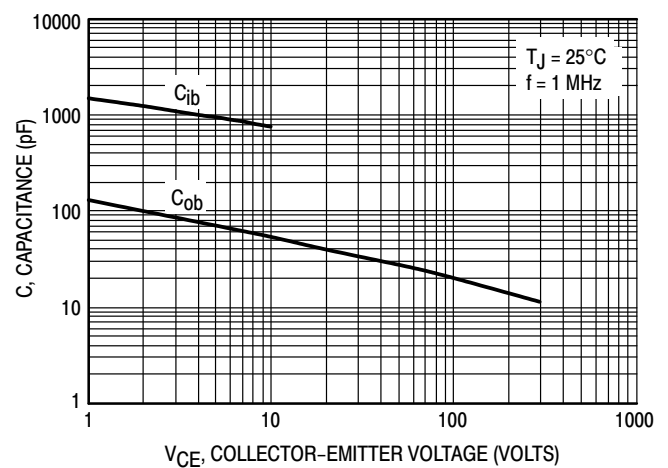


Figure 6. Capacitance

TYPICAL SWITCHING CHARACTERISTICS
($I_{B2} = I_C/2$ for all switching)

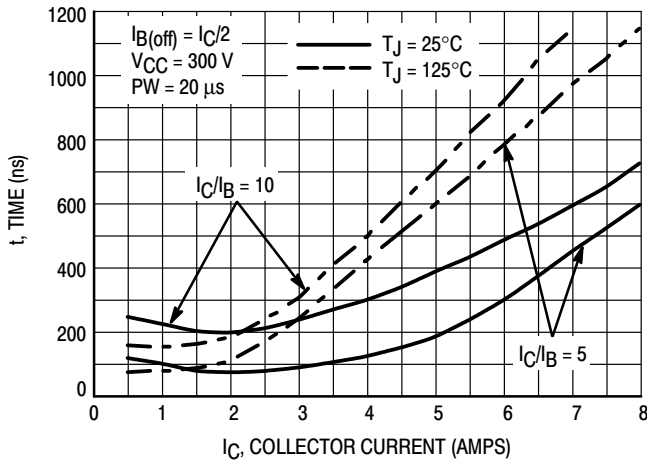


Figure 7. Resistive Switching, t_{on}

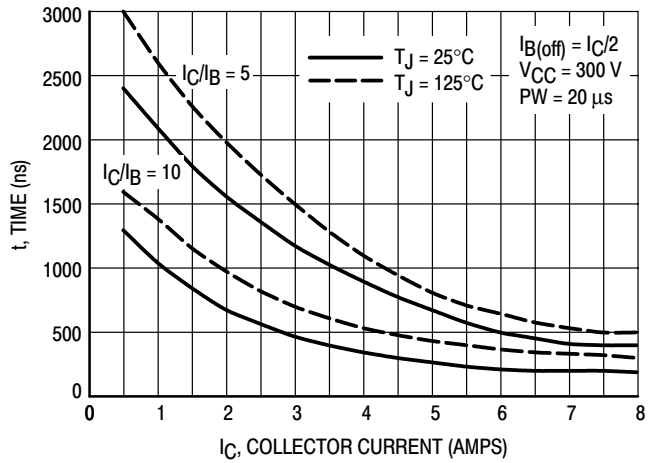


Figure 8. Resistive Switching, t_{off}

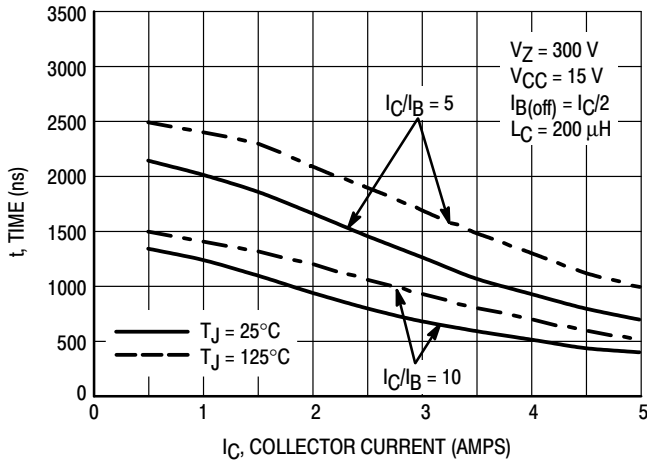


Figure 9. Inductive Storage Time, t_{si}

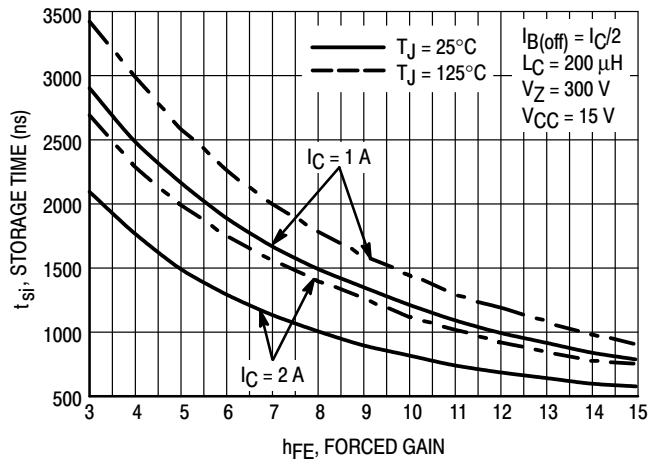


Figure 10. Inductive Storage Time, $t_{si}(h_{FE})$

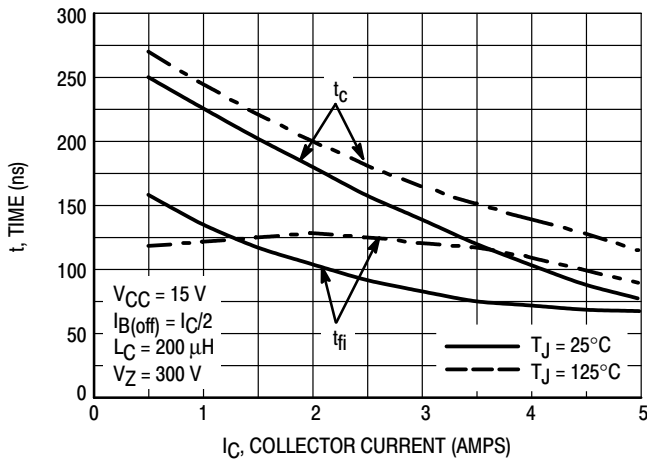


Figure 11. Inductive Switching, t_c & t_{fi} , $I_C/I_B = 5$

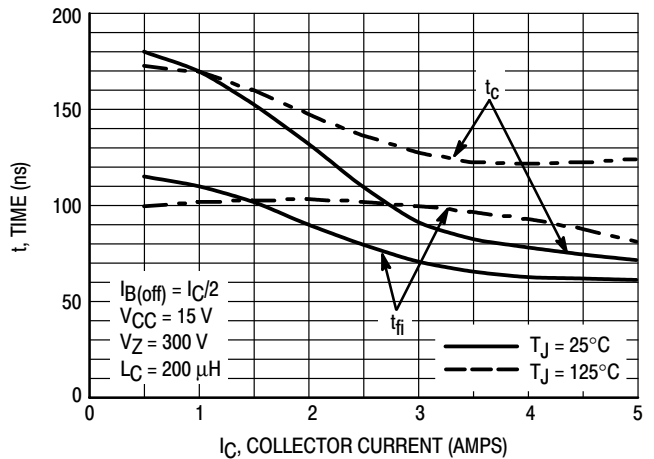


Figure 12. Inductive Switching, t_c & t_{fi} , $I_C/I_B = 10$

TYPICAL SWITCHING CHARACTERISTICS ($I_{B2} = I_C/2$ for all switching)

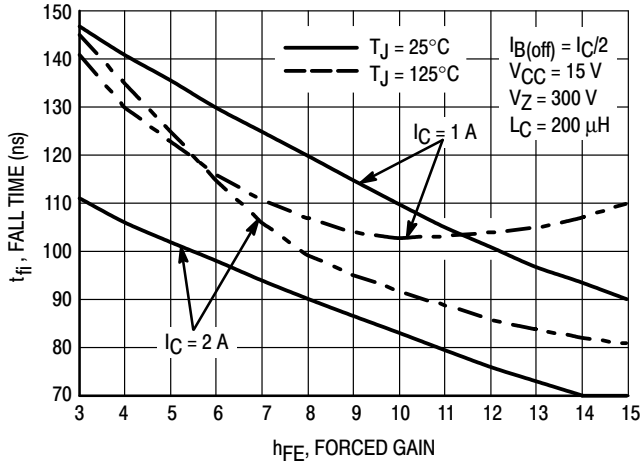
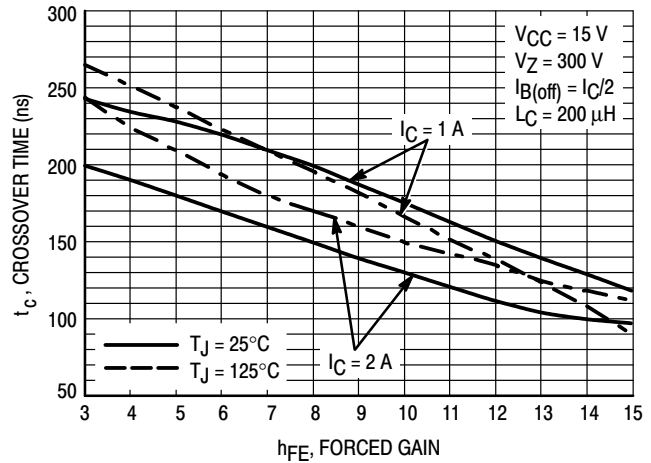
Figure 13. Inductive Fall Time, $t_{fi}(h_{FE})$ 

Figure 14. Crossover Time

GUARANTEED SAFE OPERATING AREA INFORMATION

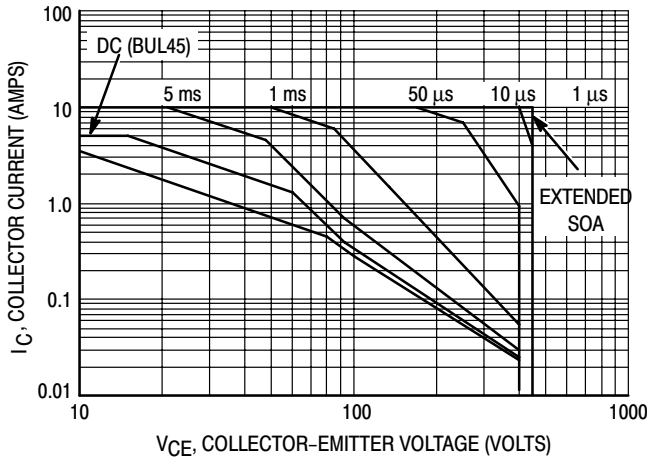


Figure 15. Forward Bias Safe Operating Area

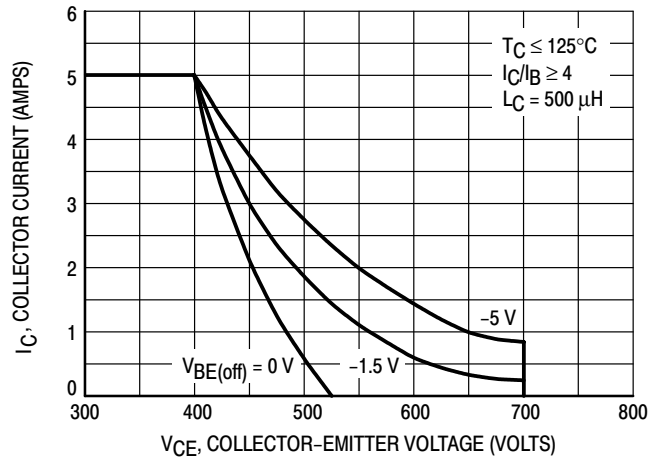


Figure 16. Reverse Bias Switching Safe Operating Area

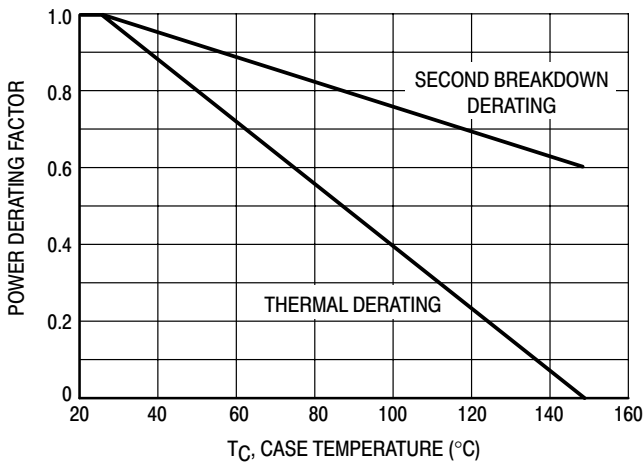


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17. $T_{J(pk)}$ may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

BUL45

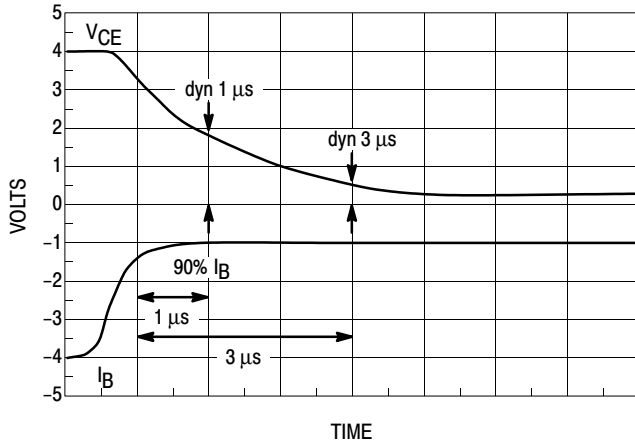


Figure 18. Dynamic Saturation Voltage Measurements

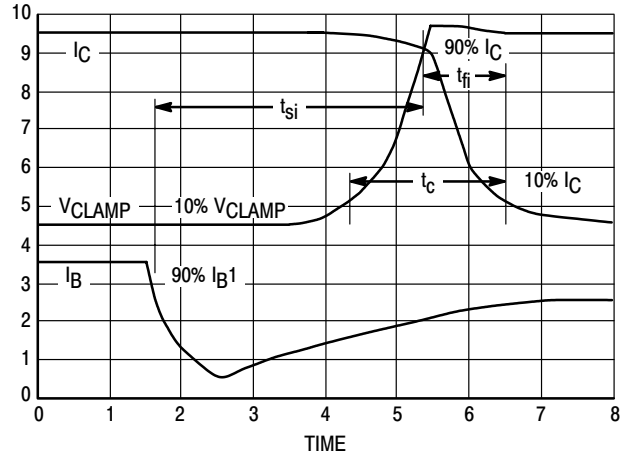
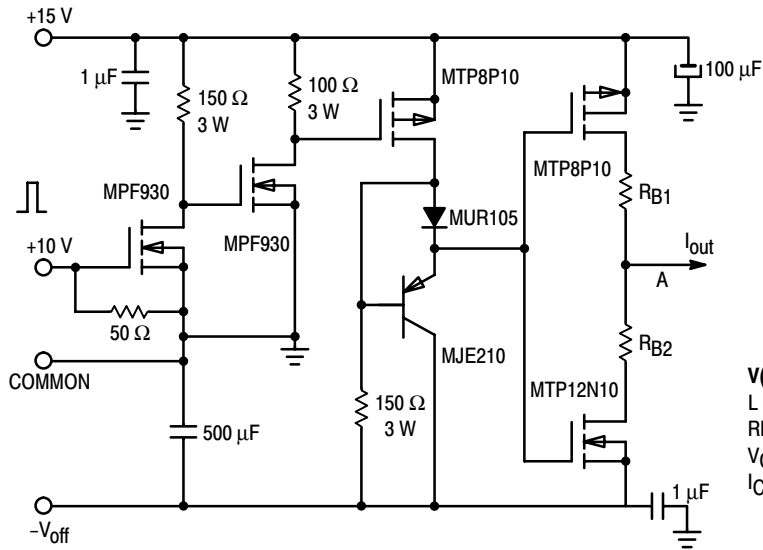


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)
 $L = 10 \text{ mH}$
 $RB2 = \infty$
 $V_{CC} = 20 \text{ VOLTS}$
 $I_C(\text{pk}) = 100 \text{ mA}$

INDUCTIVE SWITCHING
 $L = 200 \mu\text{H}$
 $RB2 = 0$
 $V_{CC} = 15 \text{ VOLTS}$
 $RB1 \text{ SELECTED FOR DESIRED } I_{B1}$

RBSOA
 $L = 500 \mu\text{H}$
 $RB2 = 0$
 $V_{CC} = 15 \text{ VOLTS}$
 $RB1 \text{ SELECTED FOR DESIRED } I_{B1}$

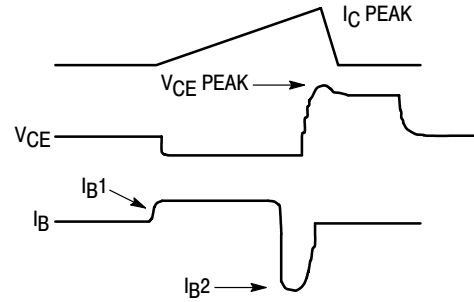


Table 1. Inductive Load Switching Drive Circuit

TYPICAL THERMAL RESPONSE

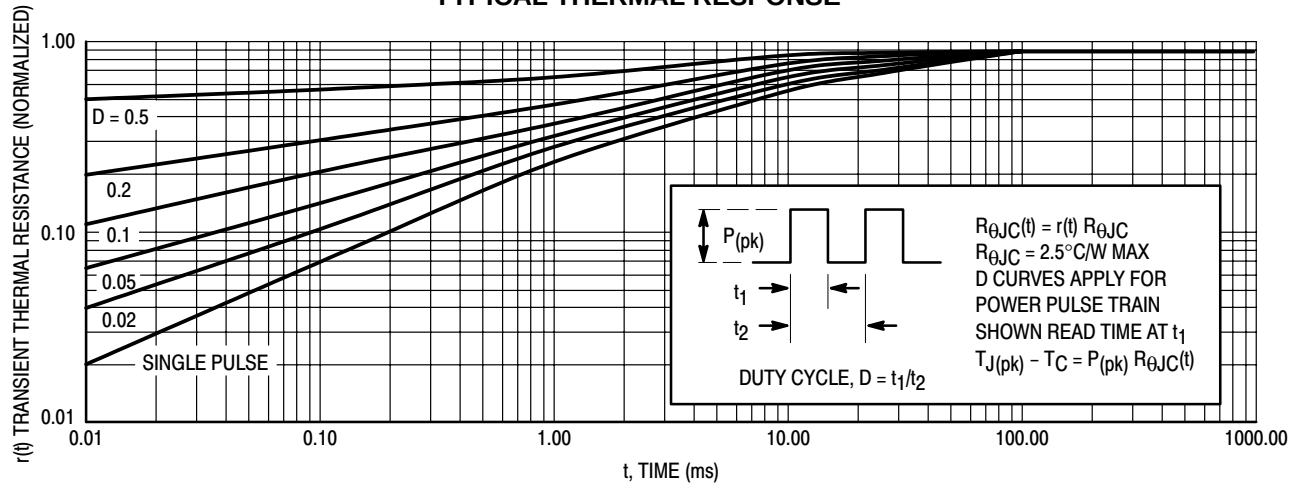
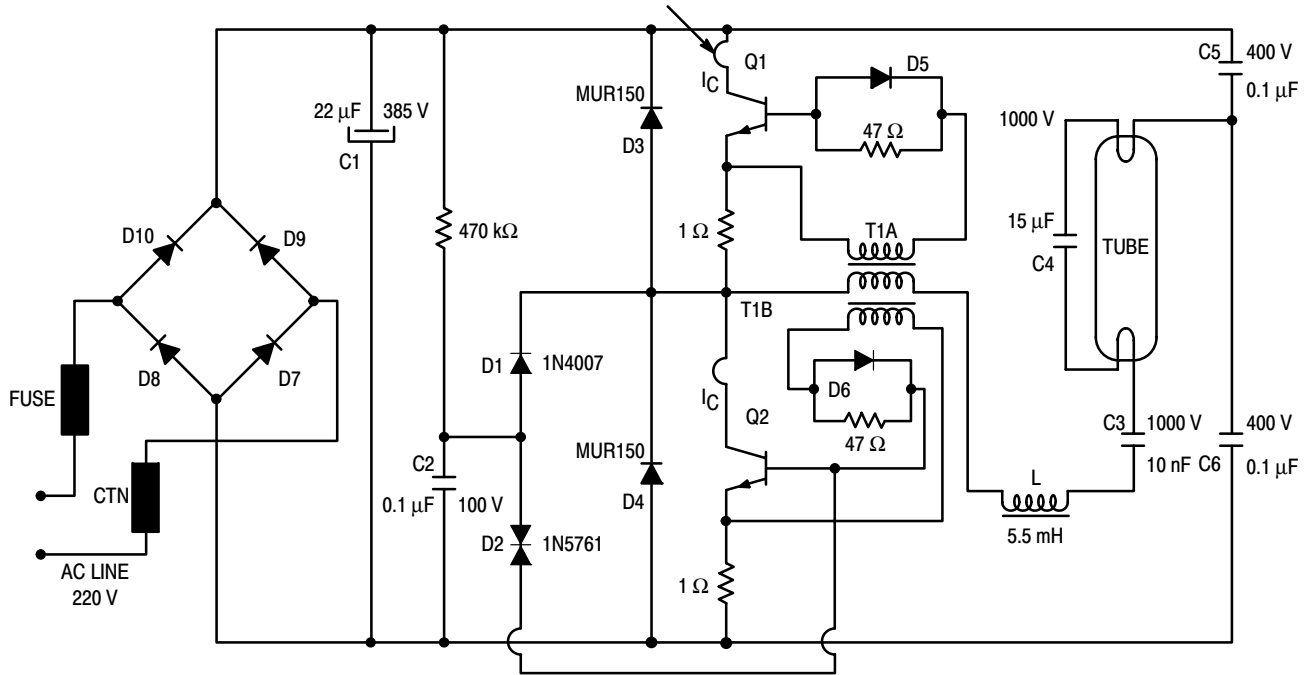


Figure 20. Typical Thermal Response ($Z_{\theta JC}(t)$) for BUL45

BUL45

The BUL45 Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by ON Semiconductor applications was built to

demonstrate how well these devices operate. The circuit and detailed component list are provided below.



Components Lists

Q1 = Q2 = BUL45 Transistor
 D1 = 1N4007 Rectifier
 D2 = 1N5761 Rectifier
 D3 = D4 = MUR150
 D5 = D6 = MUR105
 D7 = D8 = D9 = D10 = 1N400
 CTN = 47 Ω @ 25°C
 L = RM10 core, A1 = 400, B51 (LCC) 75 turns,
 wire $\varnothing$ = 0.6 mm
 T1 = FT10 toroid, T4A (LCC)
 Primary: 4 turns
 Secondaries: T1A: 4 turns
 T1B: 4 turns

All resistors are 1/4 Watt, $\pm 5\%$
 R1 = 470 k Ω
 R2 = R3 = 47 Ω
 R4 = R5 = 1 Ω (these resistors are optional, and
 might be replaced by a short circuit)
 C1 = 22 μ F/385 V
 C2 = 0.1 μ F
 C3 = 10 nF/1000 V
 C4 = 15 nF/1000 V
 C5 = C6 = 0.1 μ F/400 V

NOTES:

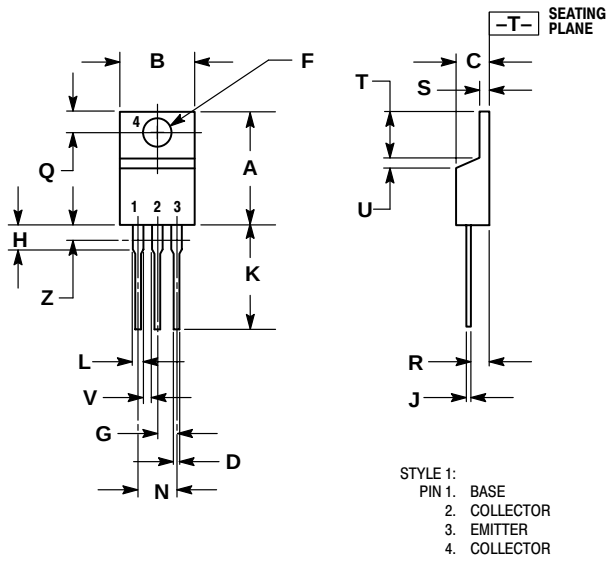
1. Since this design does not include the line input filter, it cannot be used "as-is" in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re-calculated with any other loads.

Figure 21. Application Example

BUL45

PACKAGE DIMENSIONS

TO-220AB CASE 221A-09 ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

Notes

Notes

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