

EMZ1DXV6T1, EMZ1DXV6T5

Product Preview Dual General Purpose Transistors

NPN/PNP Dual (Complimentary)

This transistor is designed for general purpose amplifier applications. It is housed in the SOT-563 which is designed for low power surface mount applications.

- Lead-Free Solder Plating
- Low $V_{CE(SAT)}$, < 0.5 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector – Emitter Voltage	V_{CEO}	-60	V
Collector – Base Voltage	V_{CBO}	-50	V
Emitter – Base Voltage	V_{EBO}	-6.0	V
Collector Current – Continuous	I_C	-100	mAdc

THERMAL CHARACTERISTICS

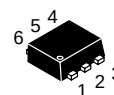
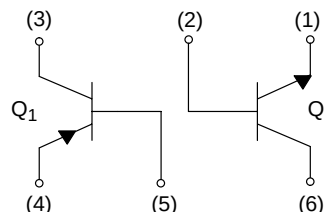
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C/W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C/W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.



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SOT-563
CASE 463A
PLASTIC

MARKING DIAGRAM



3Z = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
EMZ1DXV6T1	SOT-563	4 mm Pitch 4000/Tape & Reel
EMZ1DXV6T5	SOT-563	2 mm Pitch 8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

EMZ1DXV6T1, EMZ1DXV6T5

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Characteristic	Symbol	Min	Typ	Max	Unit
Q1: PNP					
Collector-Base Breakdown Voltage ($I_C = -50\ \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	-60	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = -1.0\ \text{mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	-50	-	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = -50\ \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	-6.0	-	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = -30\ \text{Vdc}$, $I_E = 0$)	I_{CBO}	-	-	-0.5	nA
Emitter-Base Cutoff Current ($V_{EB} = -5.0\ \text{Vdc}$, $I_B = 0$)	I_{EBO}	-	-	-0.5	μA
Collector-Emitter Saturation Voltage (Note 4) ($I_C = -50\ \text{mAdc}$, $I_B = -5.0\ \text{mAdc}$)	$V_{CE(sat)}$	-	-	-0.5	Vdc
DC Current Gain (Note 4) ($V_{CE} = -6.0\ \text{Vdc}$, $I_C = -1.0\ \text{mAdc}$)	h_{FE}	120	-	560	-
Transition Frequency ($V_{CE} = -12\ \text{Vdc}$, $I_C = -2.0\ \text{mAdc}$, $f = 30\ \text{MHz}$)	f_T	-	140	-	MHz
Output Capacitance ($V_{CB} = -12\ \text{Vdc}$, $I_E = 0\ \text{Adc}$, $f = 1\ \text{MHz}$)	C_{OB}	-	3.5	-	pF

Q2: NPN

Collector-Base Breakdown Voltage ($I_C = 50\ \mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	60	-	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = 1.0\ \text{mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	50	-	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = 50\ \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	7.0	-	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = 60\ \text{Vdc}$, $I_E = 0$)	I_{CBO}	-	-	0.5	μA
Emitter-Base Cutoff Current ($V_{EB} = 7.0\ \text{Vdc}$, $I_B = 0$)	I_{EBO}	-	-	0.5	μA
Collector-Emitter Saturation Voltage ⁽²⁾ ($I_C = 50\ \text{mAdc}$, $I_B = 5.0\ \text{mAdc}$)	$V_{CE(sat)}$	-	-	0.4	Vdc
DC Current Gain ⁽²⁾ ($V_{CE} = 6.0\ \text{Vdc}$, $I_C = 1.0\ \text{mAdc}$)	h_{FE}	120	-	560	-
Transition Frequency ($V_{CE} = 12\ \text{Vdc}$, $I_C = 2.0\ \text{mAdc}$, $f = 30\ \text{MHz}$)	f_T	-	180	-	MHz
Output Capacitance ($V_{CB} = 12\ \text{Vdc}$, $I_C = 0\ \text{Adc}$, $f = 1\ \text{MHz}$)	C_{OB}	-	2.0	-	pF

2. Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, D.C. $\leq 2\%$.

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, D.C. $\leq 2\%$.

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TYPICAL ELECTRICAL CHARACTERISTICS – Q1, PNP

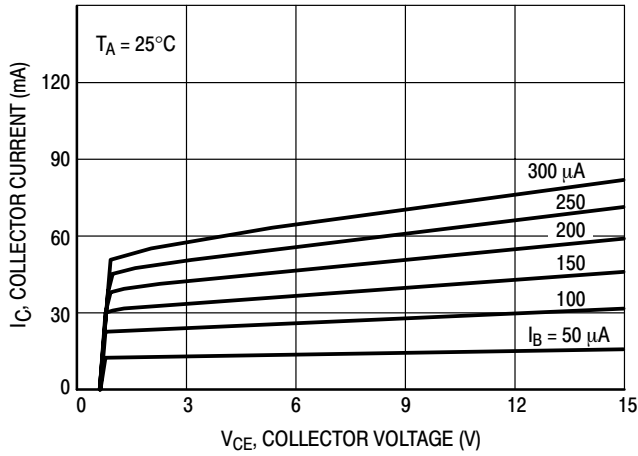


Figure 1. $I_C - V_{CE}$

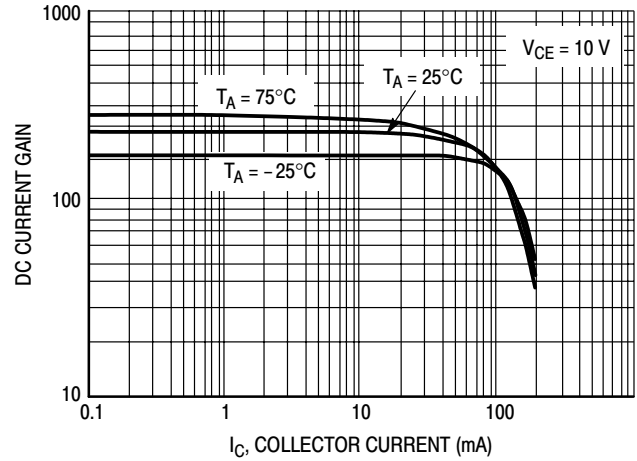


Figure 2. DC Current Gain

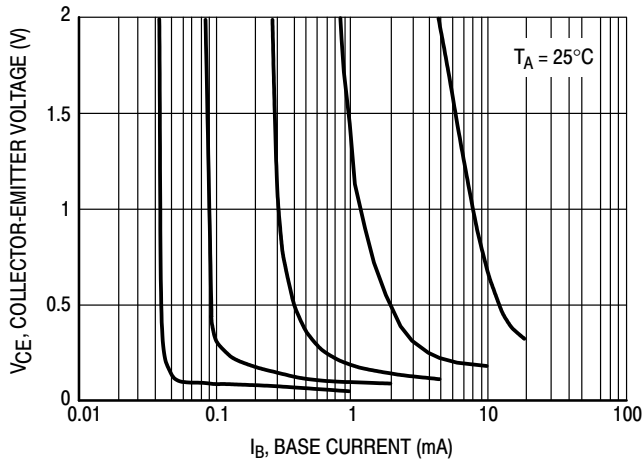


Figure 3. Collector Saturation Region

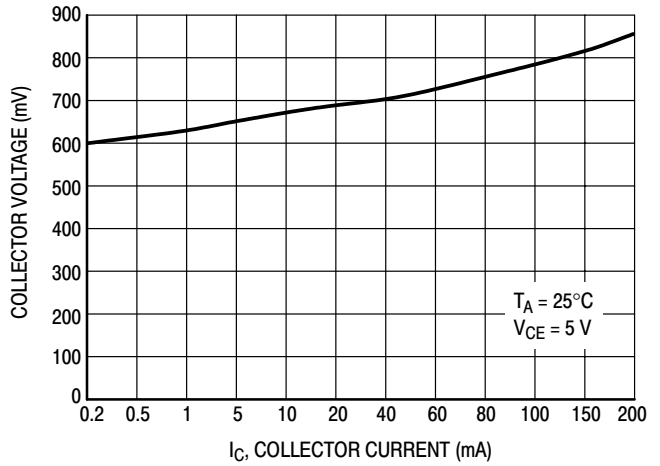


Figure 4. On Voltage

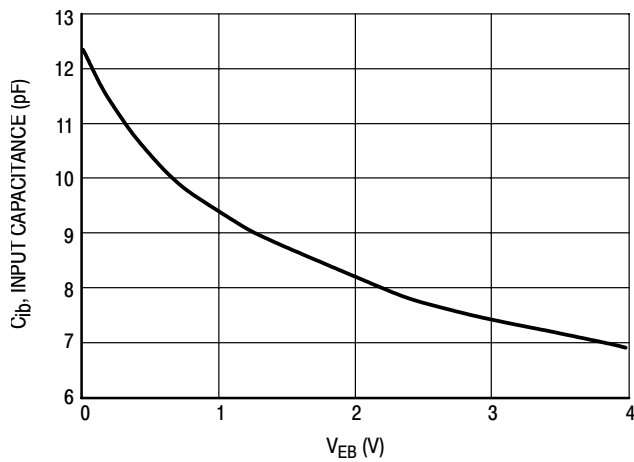


Figure 5. Capacitance

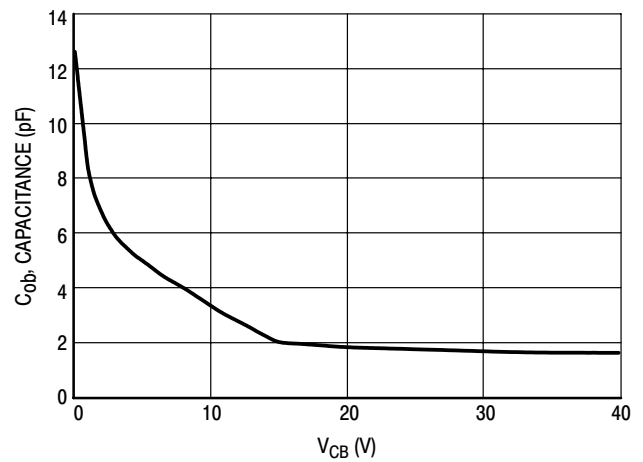


Figure 6. Capacitance

EMZ1DXV6T1, EMZ1DXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS – Q2, NPN

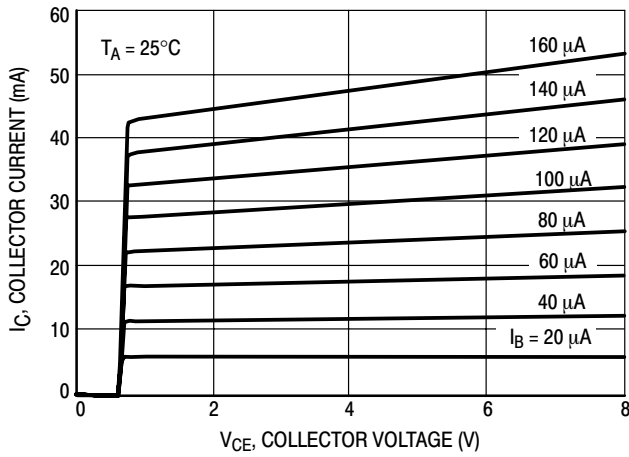


Figure 1. $I_C - V_{CE}$

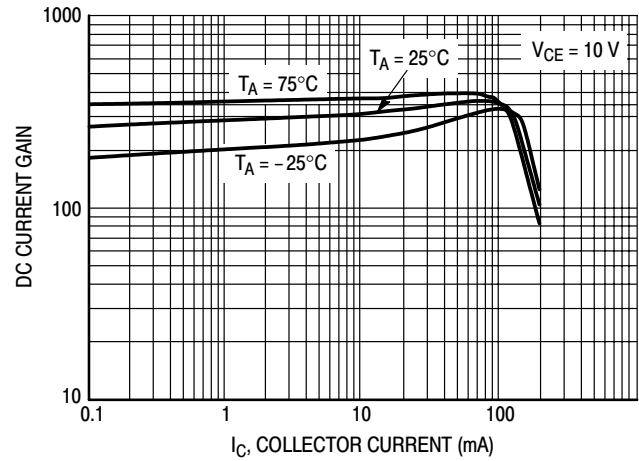


Figure 2. DC Current Gain

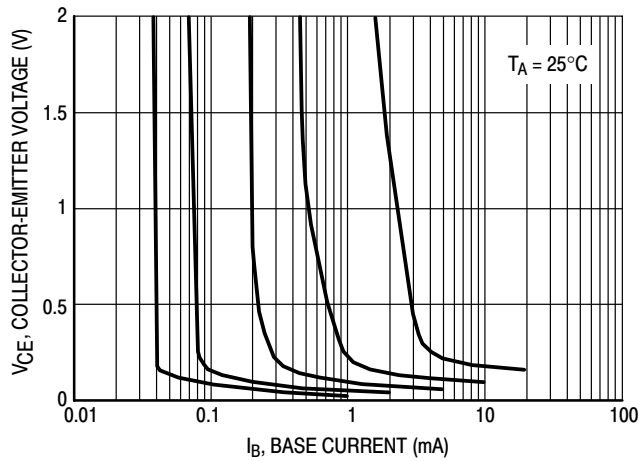


Figure 3. Collector Saturation Region

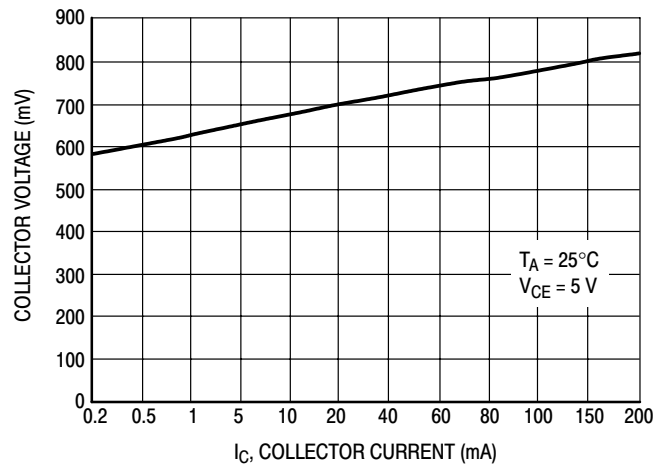


Figure 4. On Voltage

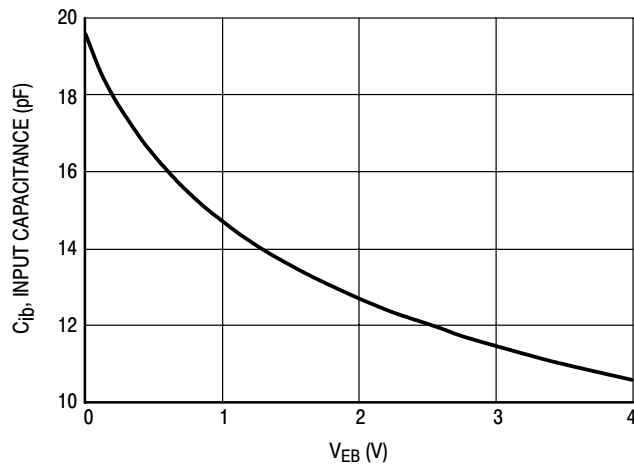


Figure 5. Capacitance

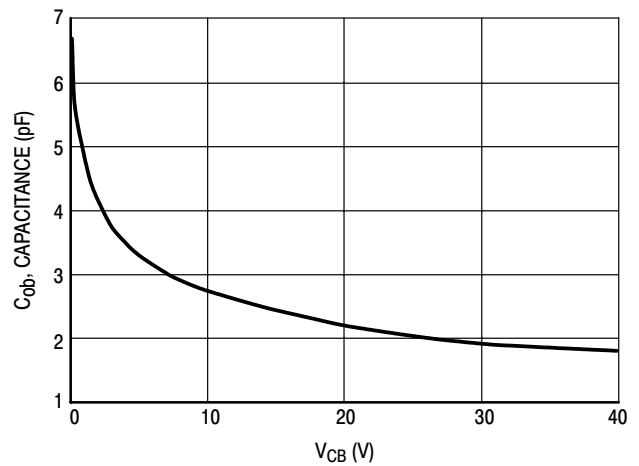
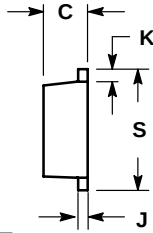
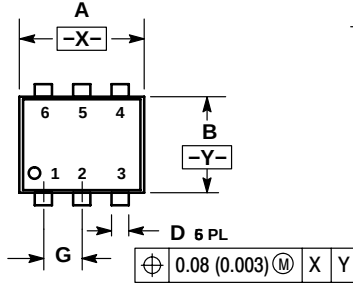


Figure 6. Capacitance

EMZ1DXV6T1, EMZ1DXV6T5

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE A



NOTES:

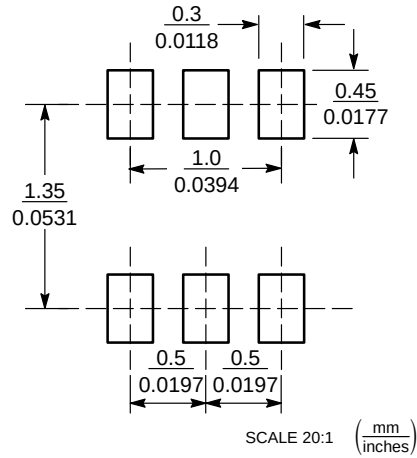
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:

- PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

SOLDER FOOTPRINT*



*For information on soldering specifications, please refer to our Soldering Reference Manual, SOLDERM/D.

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