# IRF830

# Power Field Effect Transistor

## N–Channel Enhancement Mode Silicon Gate TMOS

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

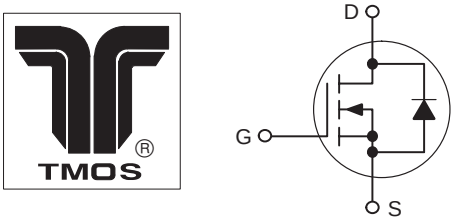
- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ to Minimize On–Losses, Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source–to–Drain Diode Characterized for Use with Inductive Loads

ON Semiconductor

http://onsemi.com

**TMOS POWER FET**
**4.5 AMPERES**
**500 VOLTS**
**$R_{DS(on)}$ = 1.5 Ω**

**N–Channel**

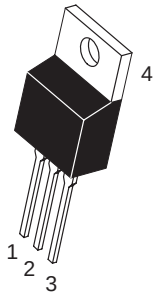



**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 500 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 500 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | ±20 | Vdc |
| Drain Current<br>Continuous, $T_C$ = 25°C<br>$T_C$ = 100°C<br>Peak, $T_C$ = 25°C | $I_D$ | <br>4.5<br>3.0<br>18 | Adc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 75<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |

**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance<br>— Junction–to–Case<br>— Junction–to–Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds | $T_L$ | 300 | °C |




**TO–220AB**
**CASE 221A**
**STYLE 5**

| PIN ASSIGNMENT | |
|---|---|
| 1 | Gate |
| 2 | Drain |
| 3 | Source |
| 4 | Drain |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| IRF830 | TO–220AB | 50 Units/Rail |

See the MTM4N45 Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP4N45 are applicable for this product.

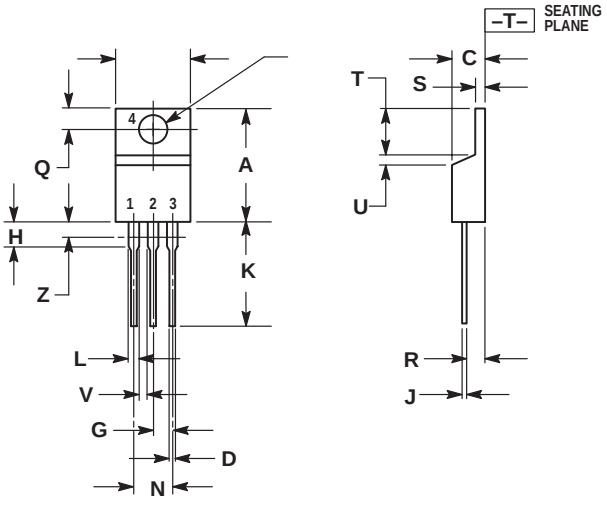
**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 500 | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 0.8 Rated $V_{DSS}$, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | —<br>— | 0.2<br>1.0 | mAdc |
| Gate–Body Leakage Current, Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS(f)}$ | — | 100 | nAdc |
| Gate–Body Leakage Current, Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS(r)}$ | — | 100 | nAdc |
| **ON CHARACTERISTICS** (1) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mA) | | $V_{GS(th)}$ | 2.0 | 4.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.5 Adc) | | $R_{DS(on)}$ | — | 1.5 | Ohm |
| On–State Drain Current ($V_{GS}$ = 10 V) ($V_{DS}$ ≥ 6.75 Vdc) | | $I_{D(on)}$ | 4.5 | — | Adc |
| Forward Transconductance ($V_{DS}$ ≥ 6.75 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | 2.5 | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | — | 800 | pF |
| Output Capacitance | | $C_{oss}$ | — | 200 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | — | 60 | |
| **SWITCHING CHARACTERISTICS** (1) | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 200 Vdc, $I_D$ = 2.5 Apk, $R_G$ = 15 Ω) | $t_{d(on)}$ | — | 30 | ns |
| Rise Time | | $t_r$ | — | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | — | 55 | |
| Fall Time | | $t_f$ | — | 30 | |
| Total Gate Charge | ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $V_{GS}$ = 10 Vdc, $I_D$ = Rated $I_D$) | $Q_g$ | 22 (Typ) | 30 | nC |
| Gate–Source Charge | | $Q_{gs}$ | 12 (Typ) | — | |
| Gate–Drain Charge | | $Q_{gd}$ | 10 (Typ) | — | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** (1) | | | | | |
| Forward On–Voltage | ($I_S$ = Rated $I_D$, $V_{GS}$ = 0) | $V_{SD}$ | 1.1 (Typ) | 1.6 | Vdc |
| Forward Turn–On Time | | $t_{on}$ | Limited by stray inductance | | |
| Reverse Recovery Time | | $t_{rr}$ | 450 (Typ) | — | ns |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from the contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>3.5 (Typ)<br>4.5 (Typ) | <br>—<br>— | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | 7.5 (Typ) | — | |

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## PACKAGE DIMENSIONS

**TO–220AB**
CASE 221A–09
ISSUE Z




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | — | 1.15 | — |
| Z | — | 0.080 | — | 2.04 |

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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