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# A DC to DC Converter for Notebook Computers Using HDTMOS and Synchronous Rectification

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One of the main issues for low output voltage power supplies is the power loss in the power semiconductors. This is especially true for portable notebook computers which require a highly efficient power supply to run their systems. The latest technology, HDTMOS is needed in order to meet the notebook power supply requirements.

As digital integrated circuit manufacturers work to implement more electrical functions and circuits onto a single silicon chip, the need for a low threshhold voltage MOSFET arises. They have presently standardized the supply voltage to a new logic level of 3.3 Volts. This new voltage standard has forced power supply design engineers to explore the possibility of using devices other than junction diodes for rectification. The Schottky and fast recovery diodes, however, have limited performance capabilities. Schottky barrier diodes are limited to a PIV generally below 100 V and fast recovery diodes have excessive reverse recovery times. The low on–resistance, power MOSFETs can break through these barriers and offer a high efficiency switchmode power supply.

## HDTMOS VERSUS CONVENTIONAL MOSFET

The advent of the power MOSFET, with its ease of drive and fast switching capability, has led to a substantial improvement in switchmode power supplies. High cell density TMOS (HDTMOS) is an advancement in power MOSFET technology that reduces power dissipation. This results in lower thermal generation and a reduction in the component's total part count.

HDTMOS provides a substantial improvement in current carrying capability by employing VLSI processing. The use of VLSI processing and new design techniques allow low–voltage MOSFETs to be manufactured with more parallel cells packed into a given die area. With 6 million cells per square inch, the yield is over 5 times greater than current conventional processing can achieve. This new technology provides a $R_{DS(on)}$ as low as 7 mohms, which is several times lower than a conventional power MOSFET.

The reduction in on–resistance achieved by employing HDTMOS technology makes it possible for power supply designers to increase the power supply output rating of a given package. They can even design the power supply for power MOSFETs without the need of a heatsink. Designers can also take advantage of its lower on–resistance to reduce junction temperature and improve system efficiency.

In addition to the low on–resistance, the reverse recovery characteristic of HDTMOS is another merit over conventional diodes. The soft recovery of the intrinsic diode allows it to be used in the output rectification circuit, thus eliminating the need for a parallel freewheeling diode in the output circuit. A typical buck converter is shown in Figure 1.

Figure 1 shows a converter that employs one power MOSFET and one Schottky rectifier for power conversion. The Schottky rectifier acts as a freewheeling diode when the MOSFET is turned off. Although the forward voltage drop of a Schottky rectifier is very low when compared to a conventional diode, these losses can be further reduced by using a MOSFET as the freewheeling diode. The resulting improvement is significant, especially in low output voltage converters.

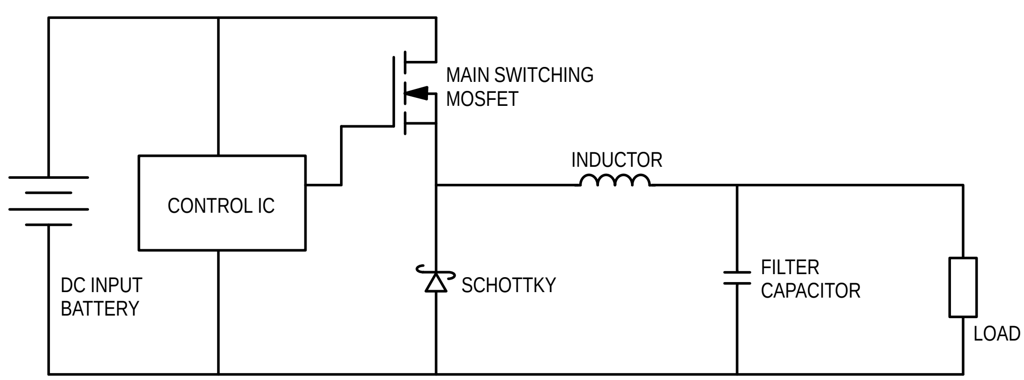


**Figure 1. Typical Buck Converter**

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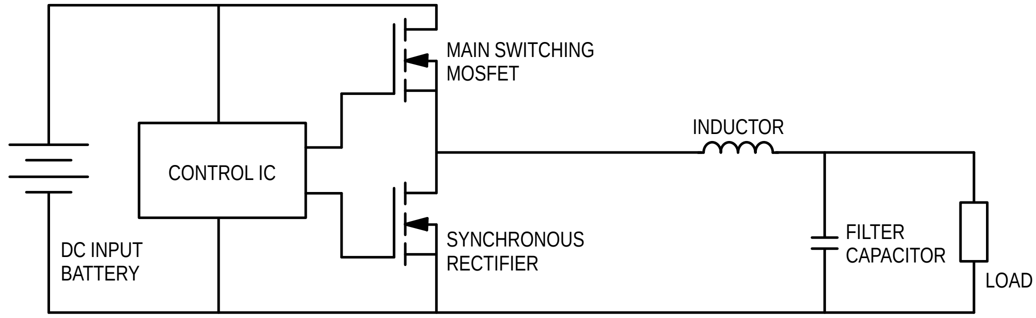



**Figure 2. Synchronous Rectification DC to DC Converter**

In order to achieve synchronous rectification during MOSFET switching, an alternate triggering control IC is needed to turn the two switching transistors on and off alternately. The buck converter includes the main switching device and the synchronous rectifier as shown in Figure 2. When the synchronous rectifier MOSFET turns on, the current will flow through the MOSFET instead of the Schottky diode. The low on–resistance of the synchronous MOSFET reduces the losses that would normally occur with a synchronous diode. Hence, the power dissipation of a diode is given by:

$$P_{diode} = I_{out} \times (1–d) \times V_f$$

Where $V_f$ = forward voltage drop of the diode
$I_{out}$ = power supply rated output current
D = duty cycle.

From the above, we know that the power dissipation of a diode is directly proportional to the diode's forward voltage drop. The power dissipation of the best Schottky diode with less than a 0.35 V forward voltage drop is still much higher than a synchronous rectifier transistor. The power dissipation of a synchronous rectifier is given by:

$$P_{MOSFET} = [I_D(1–D)]^2 \times R_{DS(on)}$$

Where $I_D$ = drain current of MOSFET
$P_{MOSFET}$ = power dissipation of the MOSFET

The $R_{DS(on)}$ of HDTMOS is only a few milliohms. The power loss in a synchronous rectifier HDTMOS is therefore much lower than the freewheeling diodes in power converter output circuits. The purpose of the Schottky freewheeling diode used in the synchronous rectification output circuit is to provide a continuous current path during the switch–over period of the two MOSFETs. Without the freewheeling diode, the current will flow through a parasitic diode of the low side MOSFET instead of the MOSFET itself. This will increase the power loss during the switching transition of the devices, whereby the parasitic diode of the MOSFET will perform like a fast recovery diode.

## THE BUCK CONVERTER

The buck converter is one of the most fundamental topologies of any switching power supply configuration. It is basically a forward–mode regulator and is also the basic building block of all the forward–mode topologies.

The basic circuit of a buck converter is shown in Figure 3. When the switch Q1 is turned on, the input voltage is applied to inductor L1, and power is then delivered to the output. Inductor current can also build up according to Faraday's Law as shown below:

$$V_L = L\ (di/dt)$$

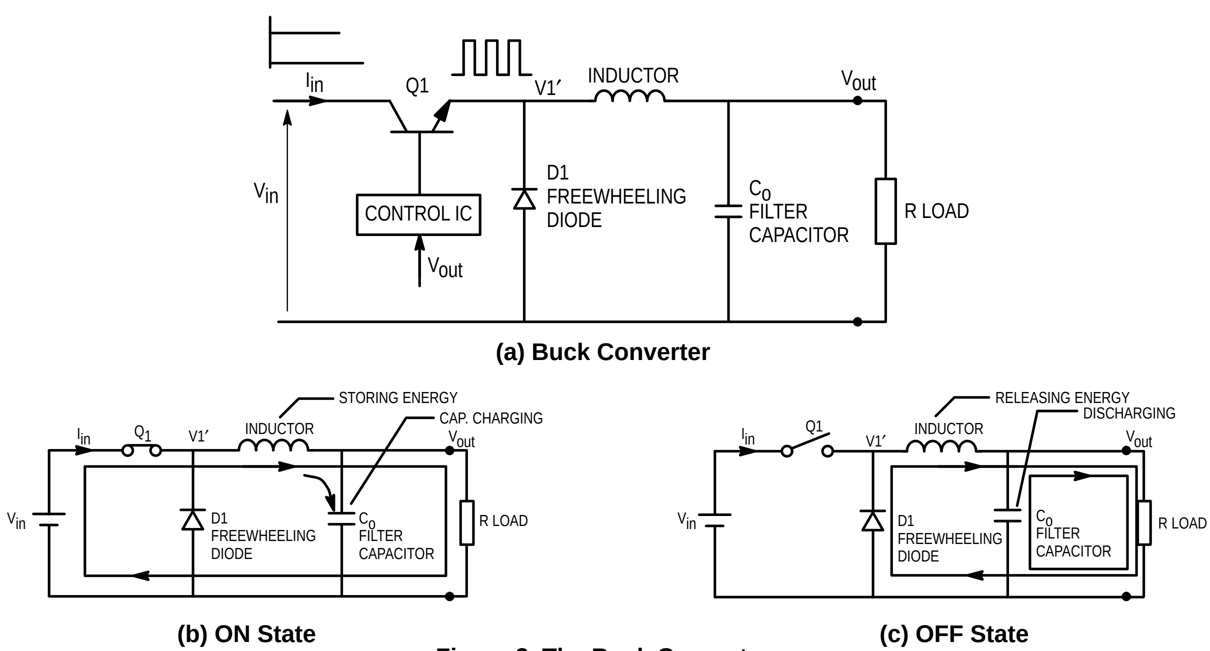



**Figure 3. The Buck Converter**

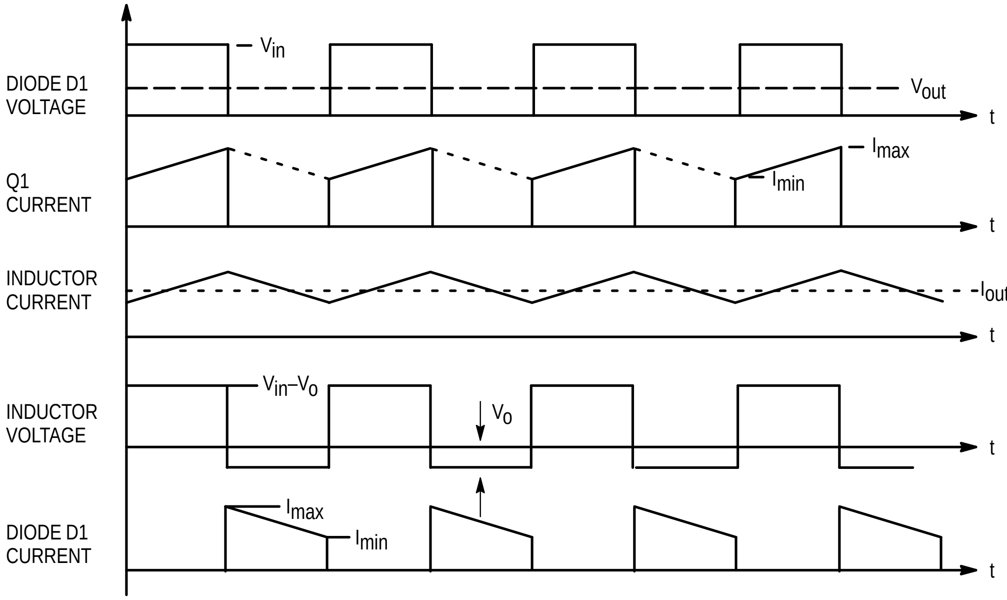



**Figure 4. Voltage and Current Waveform of a Buck Converter**

When the switch is turned off, the voltage across the inductor reverses and the free–wheeling diode D1 becomes forward biased. This allows the energy stored in the inductor to be delivered to the output where the continuous current is then smoothed by the output capacitor. Typical waveforms for a buck converter are shown in Figure 4.

The switching transistor Q1 is switched at high frequency (typically 20 kHz to 300 kHz) to produce a chopped output voltage V′. The LC filter has an arranging effect on the applied pulsating input producing a smooth dc output voltage and current. The output voltage flows to the load with only a small ripple and can be controlled by varying the Mark/space ratio of the V′.

Neglecting the circuit losses, the steady–state average voltage across the inductor is zero. The basic dc equation of the buck converter is given by:

$$V_{out}/V_{in} = D$$

Where D = transistor switching duty cycle, defined as the conduction time divided by the switching period. Usually expressed in the form of:

$$D = t_{on}/T$$

Where $T = t_{on} + t_{off}$

The buck converter is a step down type where output voltage is always lower than input. Output voltage regulation is obtained by varying the duty cycle of the switch. The buck converter is always operated in continuous mode. There are no major problems with the continuous mode buck.

When the transistor Q1 is turned on, the current flows through the inductor and the load (inductor energy is stored):

$$V_L = V_{in} – V_{out} = L \text{ x } (dI_L/dt)$$

Assume that $V_{in}$, $V_{out}$ and L are constant, and that there is no initial current (complete energy transfer).

Hence, the peak–to–peak current ripple is:

$$\Delta I_L = [(V_{in} – V_{out})/L] \text{ x } t_{on}$$

When the transistor is turned off, the inductor current flows through the free–wheeling diode and to the load, and the polarity of the voltage on L reverses (stored energy is released).

During turn–off,

$$V_L = 0 – V_{out} = L \text{ x } dI_L/dt$$

Therefore, $V_L = – V_{out}$

The current waveforms are shown in Figure 5.

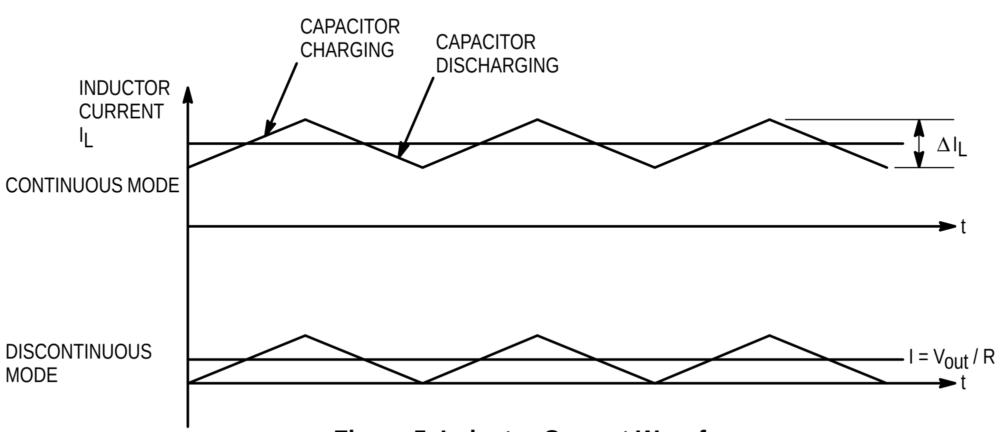



**Figure 5. Inductor Current Waveform**

Hence, the peak–to–peak current ripple is:

$$\Delta I_L = t_{on} \times [(V_{in} - V_{out})/L]$$
$$= D\ (1 - D)\ [(V_{in} \times T)/L]$$

which reaches maximum when D = 0.5

The maximum current is:

$$I_{Lmax} = V_{out}/R + \Delta I_L/2$$

The minimum current is:

$$I_{Lmin} = V_{out}/R - \Delta I_L/2$$

At the boundary condition between continuous and discontinuous modes of operation:

$$I = V_{out}/R = \Delta I_L/2$$

Hence,

$$\Delta I_L = [(V_{in} \times T)/L] \times D\ (1 - D)$$

Therefore,

$$\text{Inductor } L = [D(I - D)\ (V_{in} \times T)]/\Delta I_L \quad \text{where } \Delta I_L = 2V_{out}/R$$
$$= [D(I - D)\ (V_{in} \times T)R]/2V_{out}$$
$$= \{D(1 - D)\ [(T/t_{on})\ V_{out} \times T]R\}/2V_{out}$$
$$= [T\ (1 - D)R]/2$$

This is the minimum inductance value required for the inductor. At values lower than this, the converter will operate in discontinuous mode.

The output voltage ripple is obtained as follows:

The change in charge $\Delta Q$ of the output filter capacitor is represented by the shaded area in the diagram.

$$\Delta Q = 1/2 \times (\Delta I_L/2) \times (T/2)$$
$$= (T \times \Delta I_L)/8$$

Thus, output ripple $\Delta V_{out}$ is:

$$\Delta V_{out} = \Delta Q/C_{out}$$
$$= [T \times \Delta I_L] \times 8C_{out}$$
$$= \{[V_{out} \times T^2]\ (1 - D)D\}/8LC_{out}$$

where $C_{out}$ is the output filtering capacitor.

Thus, the minimum values of output filtering capacitor $C_{out}$ can be determined by the following:

$$C_{out} = [(V_{out} \times T^2)\ (1 - D)D]/(\Delta V_{out} \times 8 \times L)$$
$$= \Delta I/(8\ f\ \Delta V_{out})$$

To determine the $t_{on}$ & $t_{off}$ relationship, first consider the rate of change of inductor current:

$$\Delta I_L = (V/L) \times \Delta t$$

The voltage across the inductor is equal to $(V_{in} - V_{sat} - V_o)$, neglecting the voltage drop of the effective resistance of the inductor.

When Q1 is turned on,

$$\Delta I_L = [(V_{in} - V_{sat} - V_{out})/L] \times t_{on}$$

$V_{sat}$ – Q1 turned on saturation voltage

When Q1 is turned off,

$$\Delta I_L = [(V_{out} + V_f)/L] \times t_{off}$$

$V_f$ – forward voltage of diode

Since the rate of change of inductor current is equal for $t_{on}$ and $t_{off}$,

$$[(V_{in} - V_{sat} - V_{out})/L]\ t_{on} = [(V_{out} + V_f)/L]/t_{off}$$

Thus, $t_{on}/t_{off} = (V_{out} + V_f)/(V_{in} - V_{sat} - V_{out})$

Hence,

$$\text{Duty Cycle } D = t_{on}/(t_{on} + t_{off})$$
$$= (V_{out} + V_f)/(V_{in} - V_{sat} + V_f)$$

Again, a minimum value of inductor L can also be determined by using the above assumption.

Hence,

$$L = (V_L/\Delta I_L)\ \Delta t$$
$$L_{min} = [(V_{in} - V_{sat} - V_{out})/\Delta I_L]/t_{on}$$

The energy stored within the inductor during switching period is:

$$E_{store} = 1/2 \times L \times (i_{pk} - i_{min})^2$$

The input energy is stored by the flux contained within the core of the inductor L.

With the use of an appropriately chosen LC filter, the square–wave modulation could be eliminated and ripple–free DC voltages equal to the average of the duty–cycle–modulated DC input would result. By sensing the DC output and controlling the switching duty cycle in a negative feedback loop, the DC output could be regulated against input line and output load changes.

### Synchronous Rectifier

In order to reduce the free–wheeling diode drop as well as increase the converter efficiency, the Schottky diode can be replaced by an N–channel HDTMOS device to act as the main conducting device of the inductor current during the Q1 turn–off period.

When considering a converter operating with a 50% duty cycle and assuming the forward drop of the Schottky remains unchanged at 0.4 volts, it is obvious that when using a synchronous rectifier with a $R_{DS(on)}$ of 33 mohms (MTD20N03HD) or less at a current of 4 amps, the power loss is much lower than when using a free–wheeling diode.

Power = Voltage x Current or
= Current$^2$ x Resistance

### Effects of Parallel Schottky Diode

To further minimize the power loss during the dead time when switching between one HDTMOS and the other, a Schottky diode is added in parallel with the synchronous rectifier.

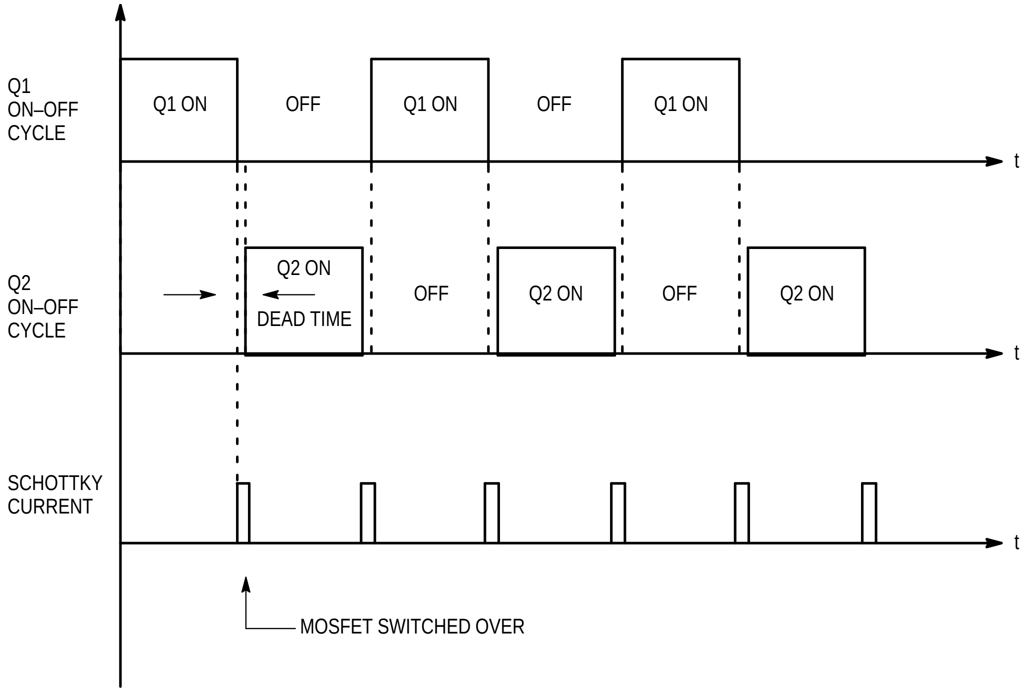



**Figure 6. Dead Time and Schottky Diode Waveforms**

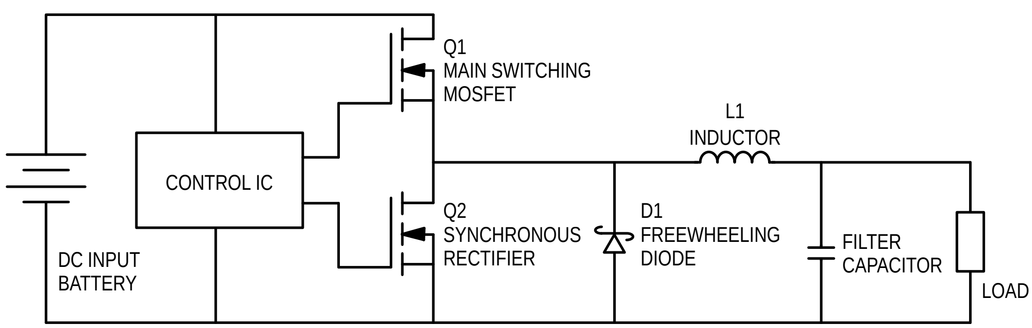



**Figure 7. Synchronous Rectifier with Parallel Schottky Diode**

When MOSFET Q1 is switched off before Q2 turns on, the free–wheeling diode D1 will provide a continuous path for either the current or the energy stored in inductor L1 to continue flowing through the diode. This waveform is shown in Figure 6. With the parallel Schottky diode D1 in place, the overall efficiency of the power supply is slightly improved. This circuit is shown in Figure 7. The comparison of efficiency between a synchronous rectifier with a parallel Schottky diode and that of a Schottky diode alone is shown in Figure 8.

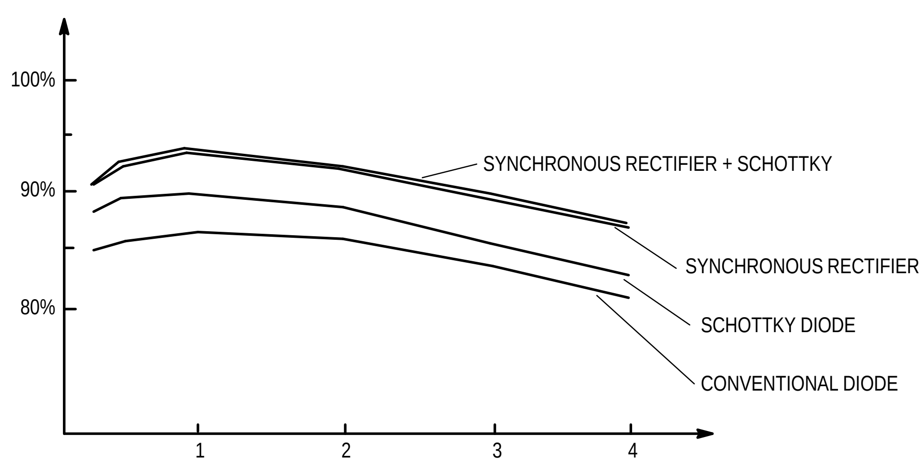



**Figure 8. The Improvement in Efficiency by Employing Synchronous Rectification**

### Further Improvements

The buck converter is one of the simplest and most fundamental configurations in switchmode power supply design. In order to further reduce the losses in the converter, either [1] increase the turn–on and turn–off switching speed of the MOSFETs' triggering gate pulses to reduce the switching loss during transition, [2] reduce the switching frequency of the converter, or [3] use low effective (internal) resistance components, i.e., inductors, input and output capacitors, low forward drop Schottkys, and low $R_{DS(on)}$ on switching MOSFETs. The switching loss of a MOSFET is shown in Figure 9.

## DC TO DC BUCK CONVERTER DESIGN

The buck converter is designed for the present market needs of notebook computers and other portable equipment where efficiency & size are important. The efficiency of the converter is an important consideration for all battery powered equipment since high efficiency prolongs the battery's operating life. Another important factor is the size of the power supply, as notebook computers and other portable products are space limited. Therefore, the outline of the power supply must be designed to be as small as possible. The design is shown in Figure 10.

### The Control IC

The choice of the control IC is extremely important. Select the one that provides the best performance in synchronous rectification. The Maxim 797 is chosen for the synchronous rectifier PWM control device. Its features include:

1. Switching frequency can go as high as 300 kHz (150 kHz/300 kHz fixed frequency PWM operation for Maxim 797)
2. Very low quiescent current. Typically 375 µA
3. High efficiency; can achieve as high as 96%
4. Adopted both high–side and low–side N–channel MOSFET for synchronous rectification operation. This will reduce losses by using P–channel for high side configuration.
5. High sink/source triggering current. Typically 1A
6. Small outline and low profile surface mount package. Ideal for notebook computers.

(Refer to the Maxim 797 data sheet for detailed information)

### Switching Frequency of Buck Regulator

The output voltage of the buck regulator $V_{out} = V_{in} (t_{on} / T)$ is independent of the value of period T. The question arises as to whether or not there is an optimum period and on what basis the period is selected. At first thought it might seem best to minimize the size of the filter components L & $C_{out}$ by going to a frequency that is as high as possible. While increasing the switching frequency will lead to an increase of AC losses in the circuit, the switching speed of the MOSFET remains constant at different operating frequencies. Therefore, the AC losses of the converter are inversely proportional to the switching period T.

The free–wheeling diode D1 can also contribute some losses during the reverse recovery period. This period is the time it takes for the diode to cease drawing reverse leakage current. The period is measured from the instant that the diode has been subjected to reverse voltage. The free–wheeling diode should therefore be specified as an ultra–fast recovery type or a Schottky, both of which have recovery times as low as 30 ns.

Even a fast recovery time diode can still dissipate significant power during the turn–off period and is also proportional to the switching frequency. While increasing the switching frequency does reduce the size of the filter elements L & $C_{out}$, it also adds to the total losses and contributes to the requirement for a larger heat sink for the switching devices (if HDTMOS devices are not used). To compromise, the switching frequency of the DC–DC buck converter discussed in this application note was selected at 300 kHz to minimize the inductor and capacitor size for notebook requirements.

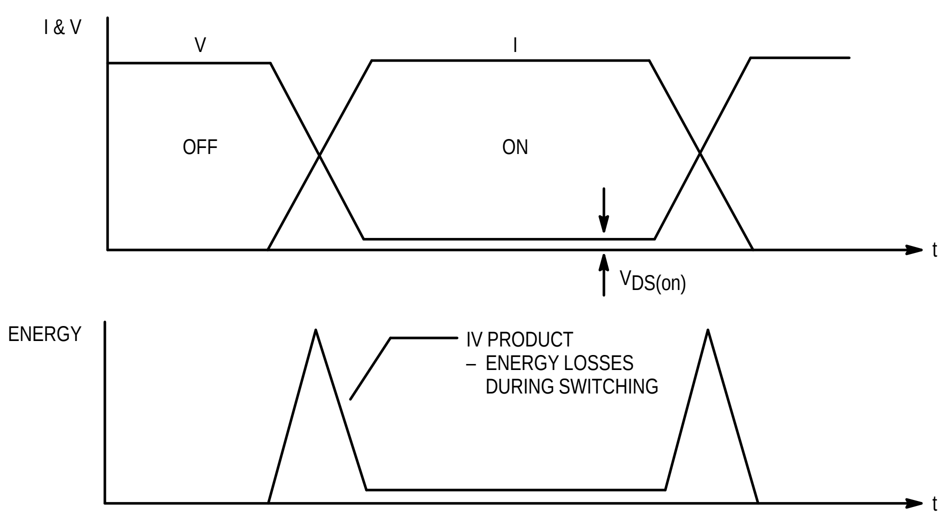



**Figure 9. Switching Loss of MOSFET**

**Output inductor**

The current waveform of the output inductor is shown in Figure 5. Its predominant characteristic is a ramping up and down waveshape during the charging and discharging cycle. It can also be noted that the current at the center of the ramp is equal to the DC output current $I_o$.

As the DC output current changes, the slope of the ramp remains constant as the voltage across L remains constant.

Where $V_L = V_{in} – V_{out}$ & $L = di/dt \times V_L$

but the current at the center of the ramp ($I_o$) decreases.

The value of the inductor is not fixed and can be adjusted freely in order to make tradeoffs among size, cost, and efficiency. Although lower inductor values will minimize size and cost, they will also reduce efficiency due to higher peak currents. To permit the use of the physically smallest inductor in the circuit, lower the inductance value until the circuit is operating at the border between continuous and discontinuous modes. Reducing the inductor values even further, below this crossover point, results in discontinuous–conduction operation even at full load. This helps reduce output filter capacitance requirements but causes the core energy storage requirements to increase again. On the other hand, higher inductor values will increase efficiency, but at some point the resistive losses due to the extra turns of wire will exceed the benefit gained from lower AC current levels. Also, high inductor values can affect the load–transient response of the converter.

Inductance L, $L_{min} = [(V_{in} – V_{sat} – V_{out})/\Delta I_L] \times t_{on}$

Consider maximum input voltage,

$V_{in}$ = 30 V
$V_{sat}$ = 1 V (for MTD20N03HD)
$V_{out}$ = 3.3 V
$\Delta I_L$ = 2A (assume 0.5 time of $I_{out}$)
$t_{on}$ = 0.66 µs (assuming D = 0.2,
f = 300 kHz)

Thus, $L_{min}$ = 8.5 µH

This is the minimum inductance requirement, below this value the converter will operate in discontinuous mode.

Hence, a 10 µH ferrite core inductor was chosen for the sample circuit.

The inductor's DC resistance is a key parameter for efficient performance and must be ruthlessly minimized, preferably to less than 25 mohms at $I_{out}$ = 3A. If a standard off–the–shelf inductor is not available, choose a core with an $LI^2$ rating greater than L x $Ipk^2$ to prevent saturation and wind it with the largest diameter wire that can fit the winding area.

In 300 kHz applications, ferrite core material is strongly preferred; for 150 kHz applications, Kool–mu (Aluminum alloy) and even iron powder is acceptable. For high current applications, shielded core geometries (such as toroidal or pot core) help keep noise and EMI to a minimum.

**Current–Sense Resistor**

The current–sense resistor values are calculated according to the worst–case, current–limit threshold voltage (between CSH & CSL pins of the Maxim control IC) and the peak inductor current. The continuous–mode peak inductor–current calculations that follow are also useful for sizing the switches and specifying the inductor–current saturation ratings.

Where $I_{peak} = (V_{out}/R) + (\Delta I/2)$
$= I_{load} + [(V_{in} – V_{sat} – V_{out})\ t_{on}]/2L$

Thus, $I_{peak} = 4 + [(30 – 1 – 3.3)\ 0.66\ \mu]/(2 \times 10\ \mu)$
= 4.9A

In order to simplify the calculation, the sense resistor $R_{sense}$ can be obtained as follows:

$R_{sense} = 100\ mV/I_{peak}$

Thus, = 100 mV/4.9
= 20.4 mohms

Hence, 15 mohms was used in the converter circuit to increase the current limit to 5.8A.

When selecting the sense resistor, low–inductance resistors, such as surface–mount metal film resistors, are preferred.

Note: The current–limit for the CSH & CSL is typically 100 mV.

**Input Capacitor Capacitance**

Place a small ceramic capacitor, C8 (0.1 µF) between V+ and GND close to the device in parallel with the bulk capacitors C1, C11, C22 and C23. This is to accommodate the high frequency components of the ripple current. Also, connect a low ESR bulk capacitor directly to the drain of the high–side MOSFET. Select the bulk input filter capacitor based on how much ripple the supply can tolerate on the dc input line. The less ripple expected, the larger the capacitor and the higher the surge current during the power–up period can be. In addition, the designer should consider replacing the single input bulk capacitor with two parallel units, each with half the capacitance value of the buck capacitor. This is to reduce the capacitor ESR to one half that of the single unit.

The value of the input bulk capacitor can be calculated by the following formula:

$$C_{in} = (I \times t)/\Delta V$$

Where $C_{in}$ = input capacitance, µF
I = input current, A = 3A (Assume 90% efficiency & 4A load)
t = time the capacitor spent supplying current, ms = $t_{on}$
1 ms = 2.666 µs (Assume duty cycle at 0.8)
$\Delta V$ = allowable peak–to–peak ripple, V = 0.2 V (Assume 0.2 V ripple)

Therefore, $C_{in} = (3 \times 2.66\ \mu)/0.2$
= 40 µF

However, four 22 µF capacitors were connected in parallel to reduce ESR and increase its capacitance for lesser input ripple.

### Output Filter Capacitor

The choice of the output filter capacitor depends upon the type of converter being used as well as the maximum operating current and switching frequency. Most of today's applications call for an electrolytic capacitor, preferably a low ESR type. The ESR of the filter capacitor has a direct effect on the output ripple and also the life of the capacitor itself. Since the ESR is a dissipative element, the power loss in the capacitor generates heat which, in turn, shortens the capacitor's life.

To ensure stability, the capacitor must meet both minimum capacitance and allowable maximum ESR values as given by:

$$V_{out} = (1/C_{out}) \int i\,dt$$

Thus, $$V_{out} = (\Delta I_L \times T)\ (4\ C_{out} \times 2)$$
$$= \Delta I/8\ f\ C_{out}$$

Rearranging the terms, the minimum output capacitance is:

$$C_{out} = \Delta I/8\ f\ \Delta V_{out}$$

$= 2/(8 \times 300K \times 0.03)$ Assume output ripple is 30 mV
$= 27\ \mu F$

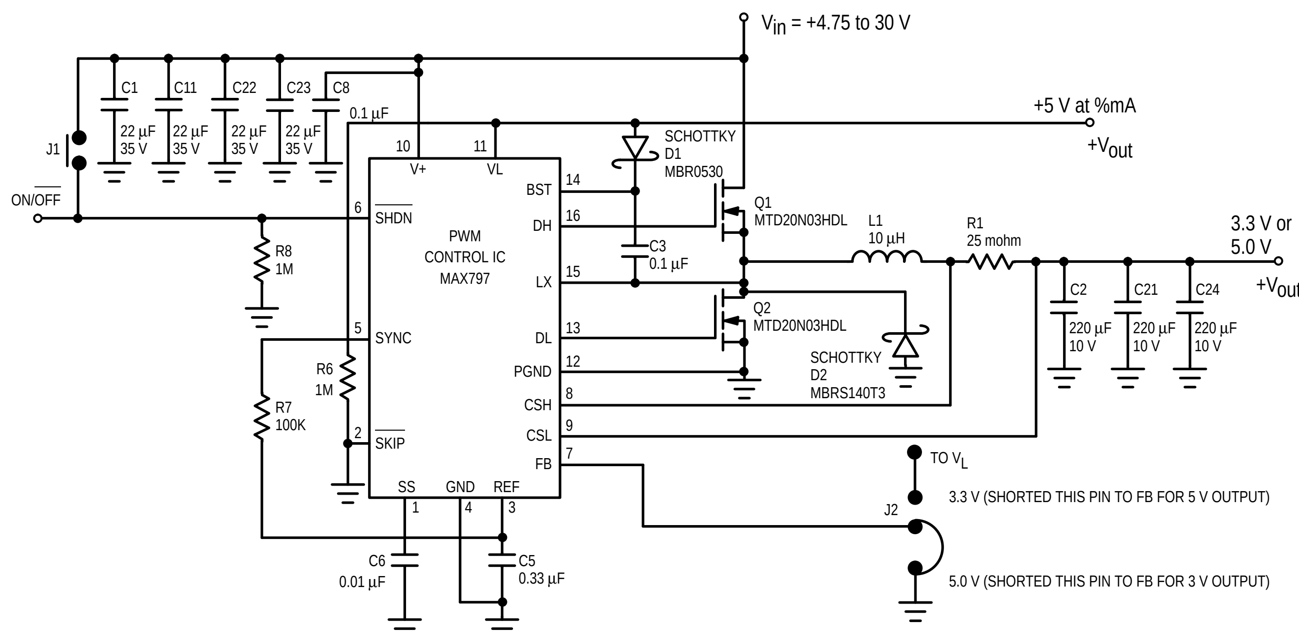
The sample board used three 220 µF capacitors connected in parallel to further reduce ESR and also to minimize output ripple.

In order to ensure minimum output ripple, the ESR of the capacitor may be calculated by the following relationship:

$$ESR_{max} = \Delta V_{out}/\Delta I_L$$

It is important to note that proper selection of the LC filter is essential since it will influence two important parameters in the performance of the switching power supply.

First, the LC filter combination has a very strong influence on the overall stability of the switching system. Second, a small L and large C will result in a low surge impedance of the output filter. This means that the power supply will have a good transient response due to load step changes.



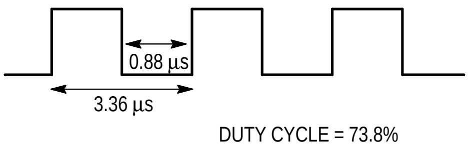

The power supply is 3.3 V or 5 V selectable.

**Figure 10. A 5 VDC to 3.3 VDC, 4 Amp Synchronous Step–Down Power Supply Controller Using N–Channel MOSFETs and Schottky Diodes** (Component List is in Table)

**Test Results**

Figures 11a and 11b show the measured waveform of the gate triggering voltage of the high side switching transistor.

11a) At $V_{in}$ = 8 V
$I_{out}$ = 4A
$V_{out}$ = 5 V




11b) At $V_{in}$ = 30 V
$I_{out}$ = 4A
$V_{out}$ = 5 V

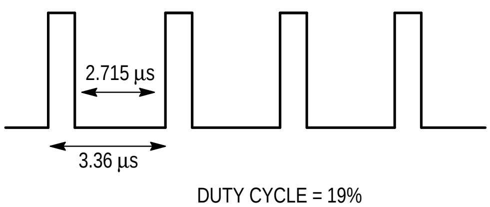



**Figure 11.**

Figure 12 shows the inductor current waveform at full load (4A) with maximum $V_{in}$ and 5 V output.

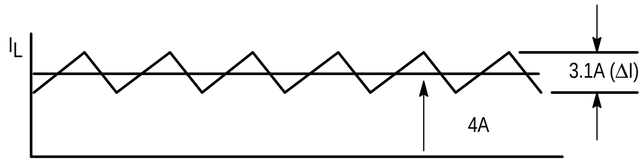



**Figure 12. Inductor Current Waveform**

Where $I_O$ = 4A, ΔI = 3.1A

The output voltage ripple measured was 30 mVp–p at full load. The transient response subject to a load change that switched from 1A to 4A at the rate of 500 Hz, was 42 mV.

The circuit was first tested on a breadboard using wires for all connections. The results are rather poor in all aspects. The system was unstable, noisy and also unable to supply full load. The current limit was low due to high noise present at the $R_{sense}$ resistor caused by the connecting wires.

The following data was obtained by using a double sided PCB with all of the appropriate components in place. This synchronous rectifier yields results that reach 92% efficiency, whereby the Schottky diode converter only attains 89% efficiency.

Efficiency data was also taken under three different line voltage conditions (minimum, nominal, and maximum) using synchronous rectification. The results show that there is little variation in the efficiency at low line conditions. At high line voltage, however, there is a significant dip in efficiency due to high losses in the inductor. The results, which were best at low line, are listed in Table 1 and also plotted in graphic form in Figure 13.

| $I_O$ (A) | $V_{in}$ = 4.75 V | | | | $V_{in}$ = 6 V | | | | $V_{in}$ = 30 V | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Eff | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Eff | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Eff |
| 0.25 | 0.2 | 4.75 | 3.33 | 88.7 | 0.16 | 6 | 3.33 | 86.7 | 0.039 | 30 | 3.34 | 72 |
| 0.5 | 0.39 | 4.72 | 3.32 | 90.6 | 0.31 | 5.99 | 3.32 | 89.3 | 0.076 | 30 | 3.33 | 73.5 |
| 1 | 0.75 | 4.69 | 3.28 | 93.2 | 0.6 | 5.97 | 3.29 | 91.8 | 0.141 | 30 | 3.31 | 78.2 |
| 2 | 1.53 | 4.63 | 3.26 | 92 | 1.2 | 5.92 | 3.27 | 92 | 0.27 | 30 | 3.3 | 81.4 |
| 3 | 2.37 | 4.57 | 3.25 | 90 | 1.866 | 5.87 | 3.25 | 89 | 0.404 | 30 | 3.29 | 81.4 |
| 4 | 3.27 | 4.5 | 3.23 | 87.8 | 2.54 | 5.82 | 3.24 | 87.7 | 0.54 | 30 | 3.28 | 81.1 |

**Table 1. Efficiency Data Under Various Input Voltage Conditions**

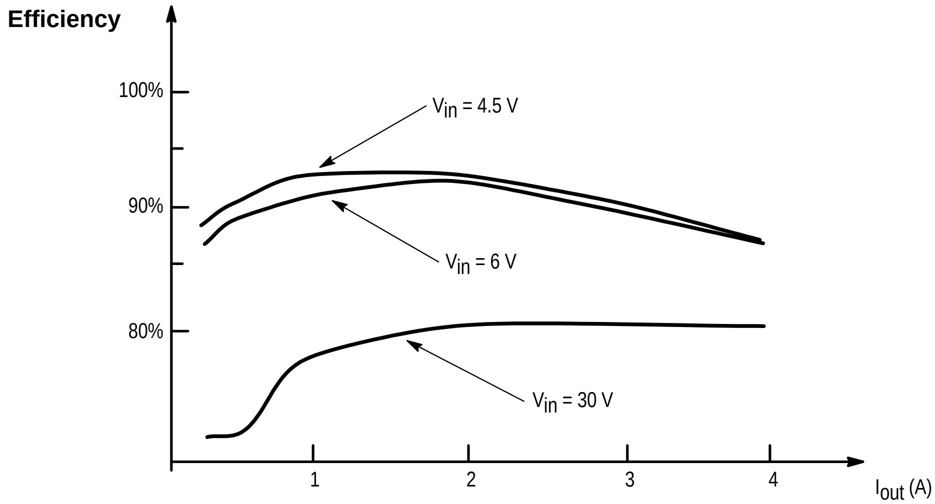



**Figure 13. Comparison of Efficiency at Different Line Input Voltage**

The efficiency comparisons between a synchronous rectifier, a Schottky diode and an ultra fast diode each used as the free–wheeling device are shown in Tables 2a and 2b.

The overcurrent protection tested was shutdown at 5.8A. It can be varied by simply changing the value of $R_{sense}$.

The major losses of the converter were mainly due to the following components:

1. $I^2R$ losses (these include inductor DC losses, $R_{DS(on)}$ of MOSFET, $R_{sense}$ and copper loss of PCB).
2. Gate–charge losses.
3. Diode conduction losses.
4. Switching losses or transition losses of power MOSFET.
5. Capacitor ESR losses.
6. PWM Control IC losses.

| | Synchronous Rectifier + Schottky | | | | Synchronous Rectifier | | | |
|---|---|---|---|---|---|---|---|---|
| $I_O$ (A) | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Efficiency | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Efficiency |
| 0.25 | 0.157 | 6.02 | 3.35 | 88.6 | 0.159 | 6.02 | 3.34 | 87.2 |
| 0.5 | 0.3 | 6 | 3.33 | 92.6 | 0.305 | 6 | 3.33 | 91 |
| 1 | 0.597 | 5.98 | 3.3 | 92.4 | 0.6 | 5.98 | 3.29 | 91.7 |
| 2 | 1.2 | 5.94 | 3.28 | 92 | 1.202 | 5.94 | 3.29 | 91.5 |
| 3 | 0.843 | 5.89 | 3.26 | 90 | 1.848 | 5.89 | 3.26 | 89.8 |
| 4 | 2.526 | 5.83 | 3.25 | 88.2 | 2.537 | 5.83 | 3.25 | 87.8 |

**Table 2a. Efficiency Comparison**

| | Schottky | | | | Diode | | | |
|---|---|---|---|---|---|---|---|---|
| $I_O$ (A) | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Efficiency | $I_{in}$ (A) | $V_{in}$ (V) | $V_O$ (V) | Efficiency |
| 0.25 | 0.161 | 6.01 | 3.34 | 86.3 | 0.165 | 6.02 | 3.34 | 84.06 |
| 0.5 | 0.32 | 6 | 3.33 | 86.7 | 0.33 | 6 | 3.33 | 84.09 |
| 1 | 0.616 | 5.98 | 3.29 | 89.3 | 0.646 | 5.98 | 3.28 | 84.9 |
| 2 | 1.25 | 5.93 | 3.27 | 88.2 | 1.3 | 5.93 | 3.27 | 84.83 |
| 3 | 1.94 | 5.88 | 3.26 | 85.7 | 2 | 5.87 | 3.25 | 83 |
| 4 | 2.67 | 5.82 | 3.24 | 83.4 | 2.73 | 5.82 | 3.24 | 81.56 |

**Table 2b. Efficiency Comparison**

| Designation | Qty | Description |
|---|---|---|
| C1, C11, C22, C23 | 4 | 22 µF, 35 V low ESR capacitor |
| | | AVX 22 µF 35 V tantalum capacitor |
| | | Sprague 22 µF 35 V tantalum capacitor |
| C2, C21, C24 | 3 | 220 µF, 10 V low ESR capacitor |
| | | AVX 220 µF 10 V tantalum capacitor |
| | | Sprague 220 µF 10 V tantalum capacitor |
| C3, C8 | 2 | 0.1 µF ceramic capacitor |
| C4 | 1 | 4.7 µF, 16 V tantalum capacitor |
| | | AVX 4.7 µF 16 V tantalum capacitor |
| | | Sprague 4.7 µF 16 V tantalum capacitor |
| C5 | 1 | 0.33 µF ceramic capacitor |
| C6 | 1 | 0.01 µF ceramic capacitor |
| D1 | 1 | Schottky diode<br>Motorola MBR0530 |
| D2 | 1 | Schottky diode<br>Motorola MBRS140T3 |
| | | Motorola MBRS340T3 |
| J1, J2 | 2 | 2–pin header |
| L1 | 1 | 10 µh, 2A inductor |
| | | Coilcraft DO3316–103 |
| Q1, Q2 | 2 | N–channel MOSFET<br>Motorola MTD20N03HDL |
| R1 | 1 | 0.025 Ω Sense resistor<br>Dale WSL–2010–R025–F |
| R6, R8 | 2 | 1 M Ω, 5% resistor |
| R7 | 1 | 100 K Ω, 5% resistor |
| U1 | 1 | Maxim MAX797 |

**Table 3. Component List for DC–DC Converter**

## CONCLUSIONS

Synchronous Rectification is possible with all commonly used converter topologies. It is achieved by simply replacing the free–wheeling diode with a MOSFET utilizing an additional gate drive circuit. As a result of this replacement, the efficiency will improve significantly.

Efficiency of 92% and higher can be achieved by using very low on–resistance MOSFETs at a lower frequency if size is not a constraint to the design. At a higher switching frequency, a fast switching gate drive and low gate charge MOSFET is required to reduce losses. To further increase the efficiency, use a low ESR capacitor for input and output filtering. In addition, reduce $I^2R$ losses by using a low dc losses inductor and increasing the PCB copper track width on the high current path.

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