HDTMOS Power MOSFETs Excel in Synchronous Rectifier Applications

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APPLICATION NOTE

INTRODUCTION

A new technology, HDTMOS™, was recently introduced which addresses the needs of today's power transistor users. This development couples VLSI techniques with the ruggedness of vertical power structures to obtain an increased cell density and provide devices that exhibit lower overall $R_{DS(on)}$. As an added benefit, the reverse recovery characteristic of the parasitic body diode was observed to be faster than MOSFETs constructed with standard technologies [1], therefore, making HDTMOS a logical choice for a number of applications, including synchronous rectifier power converters. The following is an investigation of the advantages of employing HDTMOS transistors as synchronous rectifiers in a high power buck converter and a 5 Vdc to 3.3 Vdc buck converter in order to increase circuit performance and efficiency while possibly reducing parts count.

Using HDTMOS Transistors in Synchronous Rectifier Applications

The low $R_{DS(on)}$ and intrinsic diode recovery characteristics of HDTMOS transistors are useful attributes for synchronous rectifier applications. Because of the reduced $R_{DS(on)}$, HDTMOS transistors can lower conduction losses resulting in improved efficiency over Schottky diodes. The soft recovery of the intrinsic diode allows it to also be used in the rectification process eliminating the need for a parallel Schottky diode in some cases.

Two transistors are required in a typical converter employing synchronous rectification. These include the main switch transistor (Q2) and the synchronous rectifier transistor (Q1) as shown in Figure 1. Figure 2 shows the effects a Schottky has on power loss and output voltage while Figure 3 shows the advantage of reducing the conduction loss by using a synchronous rectifier transistor in place of a Schottky. Because conduction power loss for a Schottky is a function of the average forward current while the conduction loss for a synchronous rectifier transistor is a function of the RMS current squared, a Schottky can be more advantageous at high current levels while a synchronous rectifier transistor exhibiting low $R_{DS(on)}$ can be advantageous at reduced current levels. The 0.3 volt forward drop of a typical Schottky becomes even more significant in 3.3 volt output converters when compared with the source-to-drain drop of an HDTMOS transistor which is:

$V_{SD} = R_{DS(on)} \bullet I_{drain}$.

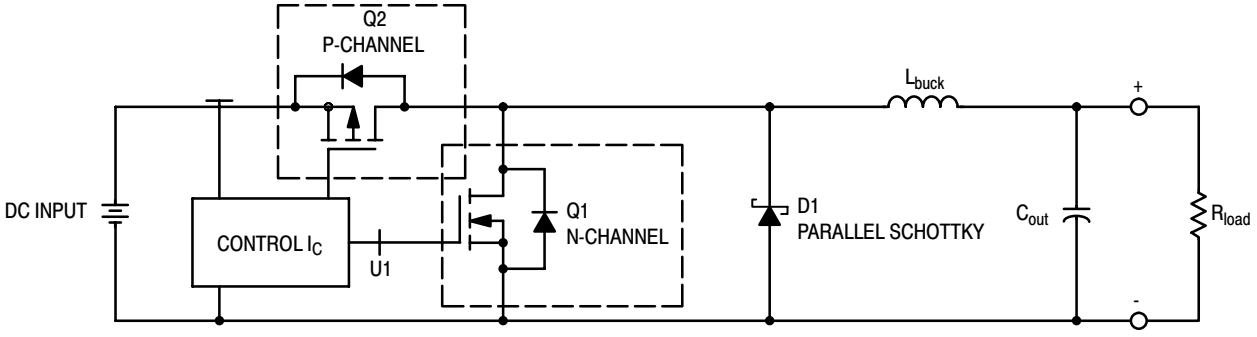

Figure 1. Typical Buck Regulator Employing a Synchronous Rectifier

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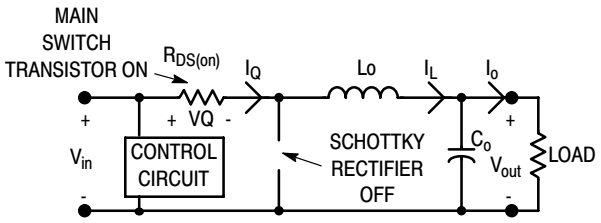
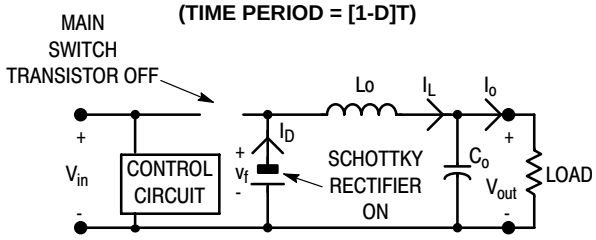
MAIN SWITCH TRANSISTOR ON
V_{IN} APPLIED
(TIME PERIOD = DT)



- **POWER TRANSISTOR PASSES CURRENT**
- **TRANSISTOR VOLTAGE DROP = I_Q x $R_{DS(on)}$**
- **TRANSISTOR POWER LOSS = I_{Qrms}^2 x $R_{DS(on)}$**

MAIN SWITCH TRANSISTOR OFF
INDUCTOR FORCES DIODE TO COMMUTATE
(TIME PERIOD = [1-D]T)



- **RECTIFIER DIODE PASSES CURRENT**
- **DIODE FORWARD VOLTAGE DROP = v_f**
- **DIODE POWER LOSS = $I_{D(avg)}$ x v_f**

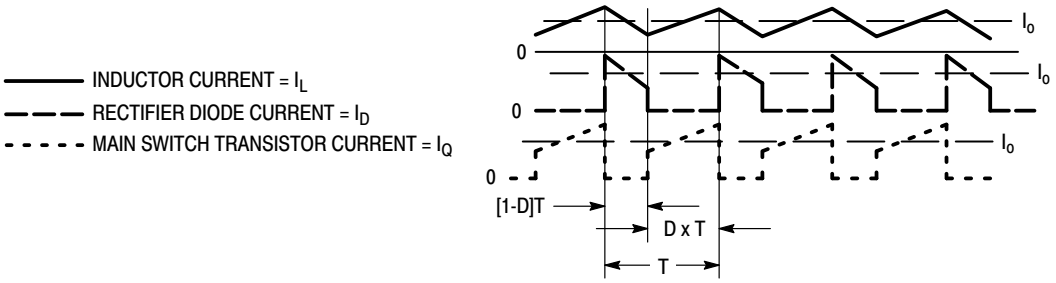
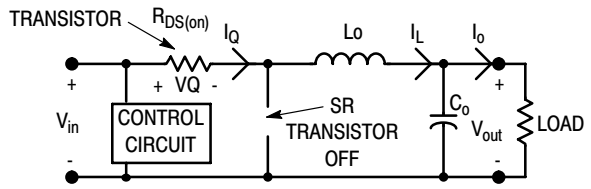


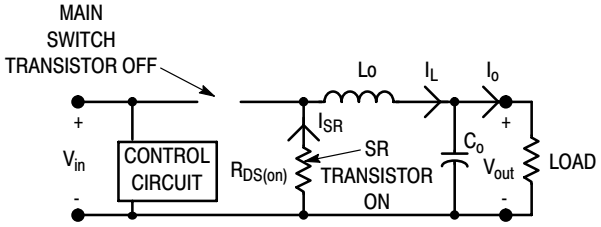
Figure 2. Buck Regulator Semiconductor Losses with a Schottky Rectifier

MAIN SWITCH TRANSISTOR ON
V_{IN} APPLIED
(TIME PERIOD = DT)



- **POWER TRANSISTOR PASSES CURRENT**
- **TRANSISTOR VOLTAGE DROP = I_Q x $R_{DS(on)}$**
- **TRANSISTOR POWER LOSS = I_{Qrms}^2 x $R_{DS(on)}$**

MAIN SWITCH TRANSISTOR OFF
SYNCHRONOUS RECTIFIER (SR) TRANSISTOR ON
(TIME PERIOD = [1-D]T)



- **SR TRANSISTOR OPERATES IN THIRD QUADRANT**
- **SR VOLTAGE DROP = I_{SR} x $R_{DS(on)}$**
- **SR POWER LOSS = I_{SRrms}^2 x $R_{DS(on)}$**

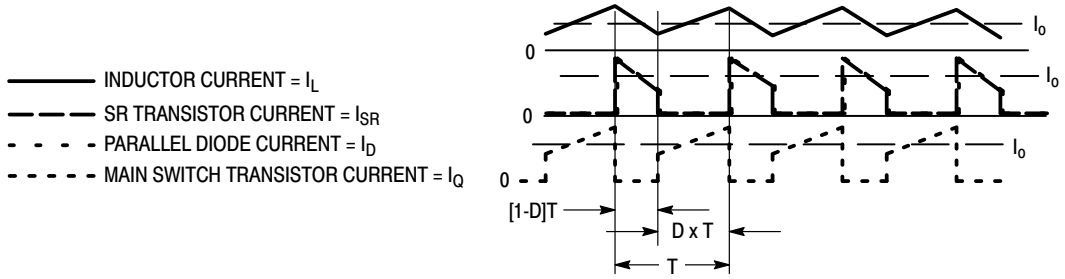


Figure 3. Buck Regulator Semiconductor Losses with a Synchronous Rectifier Transistor

A comparison of the power losses between HDTMOS transistors and Schottky diodes as used in the buck converter applications is shown by the following two equations:

$$P_{Schottky} = v_f \times I_o \times \frac{(1 - D)}{T}$$

and

$$P_{N\text{-}Channel} = (I_o \quad \sqrt{(1 - D)})2 \quad \times R_{DS(on)},$$

where

v_f = forward drop of the Schottky diode,

I_o = output current,

T = period (1/f), and

D = duty cycle.

Figures 4a and 4b show the conduction power loss advantages for transistors with 100 mΩ and 10 mΩ $R_{DS(on)}$ respectively when considering a converter operating with a 50% duty cycle and assuming the forward drop of the Schottky remains fixed at 0.3 V. It is obvious in Figure 4a that using a synchronous rectifier transistor with an $R_{DS(on)}$ of 100 mΩ at currents of less than 3 A improves conduction power loss. Similarly, Figure 4b shows the current can increase to 30 A when $R_{DS(on)}$ is 10 mΩ.

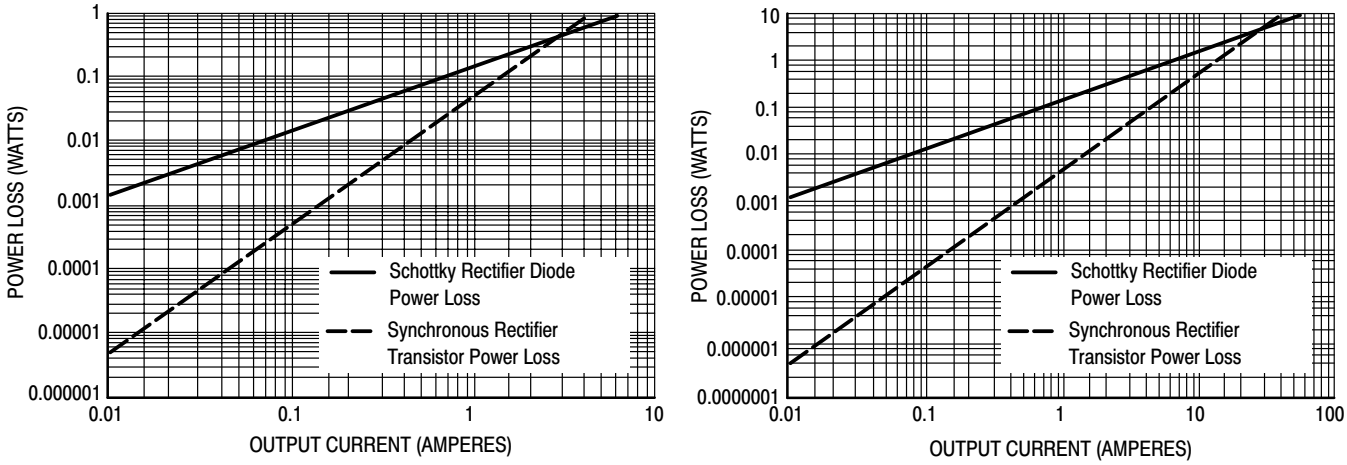


Figure 4. Buck Regulator Rectifier Conduction Power Loss Comparison versus Current
(a) $R_{DS(on)}$ = 100 mΩ (b) $R_{DS(on)}$ = 10 mΩ

In order for the N-Channel to act as a synchronous rectifier by replacing the free wheeling diode as the main conducting device during the downslope of the inductor current, the device must be oriented such that the intrinsic body diode blocks voltage. This orientation requires the device to be operated in the third quadrant. Operation in the first quadrant is typical and refers to the graph of "On-Region Characteristics" that is found on a power MOSFET transistor data sheet where the abscissa is V_{DS} and the ordinate is I_D. Operation in the third quadrant results when the drain current, I_D flows from source to drain and due to Ohm's law, the V_{DS} is also of a negative convention as shown in Figure 5. Note how the various curves relate to the gate-to-source voltage, V_{GS}, of the logic level device and how the body diode knee curve appears for V_{GS} values of 0 V and 1 V. This provides insight into operating the device properly as a synchronous rectifier. Two considerations that surface are: (1) The level of the gate-to-source voltage must be sufficiently high enough to keep the intrinsic body diode below 0.5 V to keep it from turning on, and (2) the current through the drain could be high enough for the channel impedance to drop in excess of 0.5 V. As shown in Table 1, $R_{DS(on)}$ actually improves when the device is operated in the third quadrant for certain levels of gate-to-source voltage.

Table 1. Summary of $R_{DS(on)}$ Values Measured in Figure 5 for an MTP75N03HDL Logic Level, N-Channel Device

V_{GS}	$R_{DS(on)}$ Quadrant #1	$R_{DS(on)}$ Quadrant #3	Percent Improvement
1 V	—	—	—
2 V	—	—	—
3 V	—	10.3 mΩ	—
4 V	9.1 mΩ	7.7 mΩ	15.0%
5 V	7.4 mΩ	6.7 mΩ	9.3%
6 V	6.7 mΩ	6.2 mΩ	8.5%
7 V	6.3 mΩ	6.1 mΩ	4.2%

For high current applications, N-Channel transistors are used for both the main switching transistor and the synchronous rectifier transistor because N-Channel transistors have lower $R_{DS(on)}$ than equivalent die sized P-Channel transistors and the selection of P-Channel devices is limited. However, high side switching of N-Channel devices requires additional circuitry even with today's sophisticated synchronous rectifier IC's. The HDTMOS technology has been applied to a line of P-Channel devices as well as N-Channel devices. Like N-Channel devices, the HDTMOS technology provides P-Channel devices with lower $R_{DS(on)}$ when compared to devices constructed using earlier technologies.

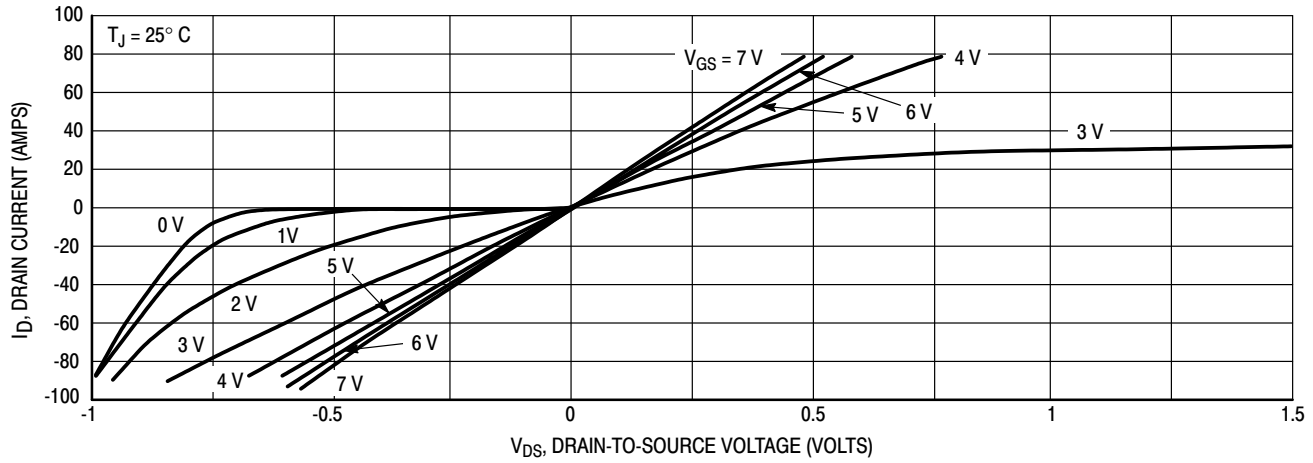


Figure 5. On Region Characteristics of an MTP75N03HDL Logic Level, N-Channel Device for Both the First and Third Quadrant

Another benefit of HDTMOS technology is the soft recovery exhibited by the parasitic body diode. Figure 6 illustrates the reverse recovery current of the MTP75N05HD device as compared to devices designed with standard technologies. The softer diode recovers quicker and has a reduced peak recovery current value. The circuits investigated here explore the use of this diode versus a parallel Schottky for operation during synchronous rectifier transistor "dead times." Dead times are time periods where neither switch conducts to prevent shoot through and are a feature of the newer integrated circuits that are designed specifically for synchronous rectification.

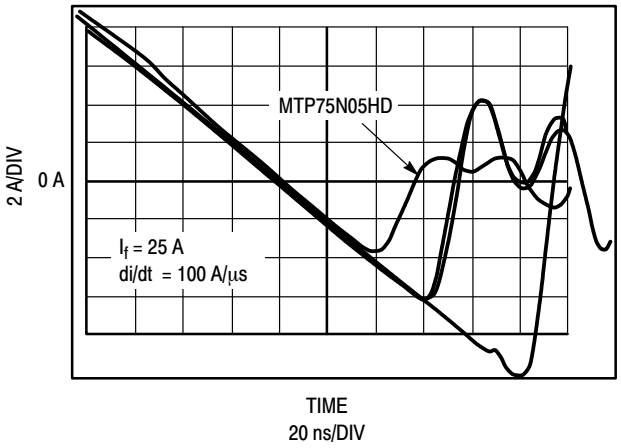


Figure 6. Comparison of Reverse Recovery Performance Between HDTMOS Transistors and Devices Built with Standard Processes

The benefits of increased efficiency and the requirement for lower logic voltage levels has heightened interest in synchronous rectifiers. In addition, the recent advances in integrated circuits has greatly reduced the complexity of implementing synchronous rectification in nonisolated applications. Applications that require transformer isolation are becoming more popular and recent work has focused in this area [7].

5 Vdc to 3.3 Vdc Buck Converter

In order to investigate the benefits of HDTMOS transistors as synchronous rectifiers, an application was sought that required the use of highly efficient power converters. Recent demand for 3.3 V logic levels in computer applications ranging from off-line to battery powered techniques provided an excellent testbed for the HDTMOS products offered in the SO-8 package known as the MiniMOS™ line.

The entire basis for using 3.3 V logic IC's is to reduce power dissipation while increasing switching speed in the logic circuitry and particularly, the CMOS transistors. This has its basis in the following equation:

$$i = C_{iss} \frac{dv_{GS}}{dt}$$

where

C_{iss} = MOSFET input capacitance, and dv_{GS}. = the transition of the MOSFETs gate-to-source voltage.

For a given value of C_{iss} and i, a faster dt can be achieved with a reduced voltage transition dv_{GS}. Similarly, gate charge losses in a MOSFET can be summarized as follows:

$$p_{gate} = (C_{iss} \times v_{gs}^2) \times f/2$$

where f is the switching frequency of the converter.

By lowering the logic level applied to the gate from 5 V to 3.3 V, devices do not dissipate as much power due to the relation of the power to the gate voltage squared. The increased use of a 3.3 volt logic level has required power converters that convert existing logic 5 Vdc busses to 3.3 Vdc. Without the ability to design an efficient conversion process, the use of 3.3 volt logic levels does not make sense for many applications due to the fact that any efficiency gains realized by saving gate charge losses in the IC's could be nullified by using an inefficient converter. It

is for these reasons that designers are seeking highly efficient, 5 Vdc to 3.3 Vdc power converters.

Designs with efficiencies in excess of 95% have been realized using various combinations of HDTMOS transistors as synchronous rectifiers in 5 Vdc to 3.3 Vdc buck converters. Figure 7 shows the schematic of a synchronous rectifier, DC to DC, buck converter using HDTMOS transistors. The boxed components were interchanged for assessing the efficiency effects of using various combinations of HDTMOS transistors and Schottky diodes.

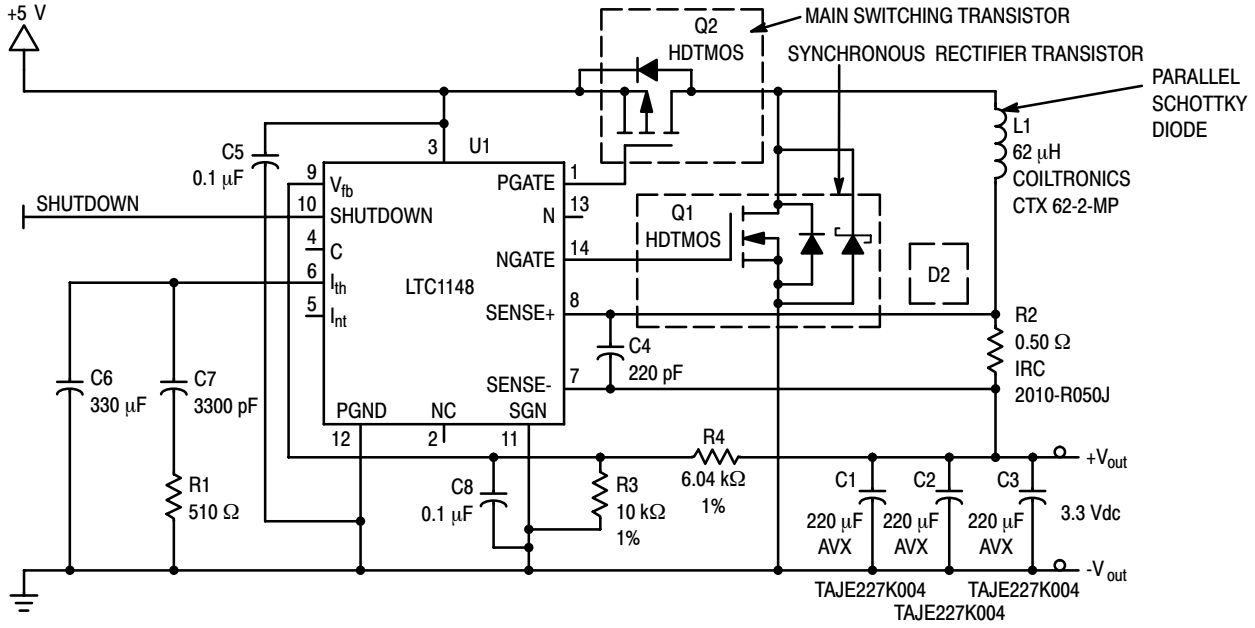


Figure 7. Schematic of a 5 Vdc to 3.3 Vdc Buck Converter Employing a Synchronous Rectifier (part sources listed under References)

Measured Effects of a Schottky Rectifier

In order to verify the effectiveness of a synchronous rectifier compared to a standard Schottky, the efficiency of the testbed was measured using each circuit arrangement as illustrated in Figure 8. Over the chosen output current range, the use of a synchronous rectifier provides at least 10% better efficiency than the Schottky diode does. Note that the minimum current for regulation in this particular application is 0.5 A. This is do to a phenomenon known as Burst Mode™ that is described below.

Measured data indicates the parallel Schottky's role in overall efficiency is dependent upon the operating level of the circuit's output current as shown in Figure 8. Referring to Figure 8 it can be seen that at output current levels of less than 0.5 A, the efficiency measured is better *with* the parallel Schottky diode across the synchronous rectifier transistor. This is due to the operation of the LTC1148 integrated circuit that transfers from Burst Mode to full ON at an output current of 0.5 A. Burst Mode is a way of cycling the integrated circuit at lower output currents so that the power loss due to the drive circuitry is reduced and the efficiency is increased. For more information, the reader is referred to reference [2]. During Burst Mode, the parallel diode conducts more often and therefore, the converter is more efficient with a Schottky diode than using the intrinsic body diode of the HDTMOS N-Channel transistor due to the Schottky's lower forward voltage drop. However, for currents of greater than 0.5 A, the use of a parallel Schottky with the N-Channel synchronous rectifier does not result in significant gains in efficiency. With the results presented, the designer is capable of designing an efficient converter based on required efficiency and available space.

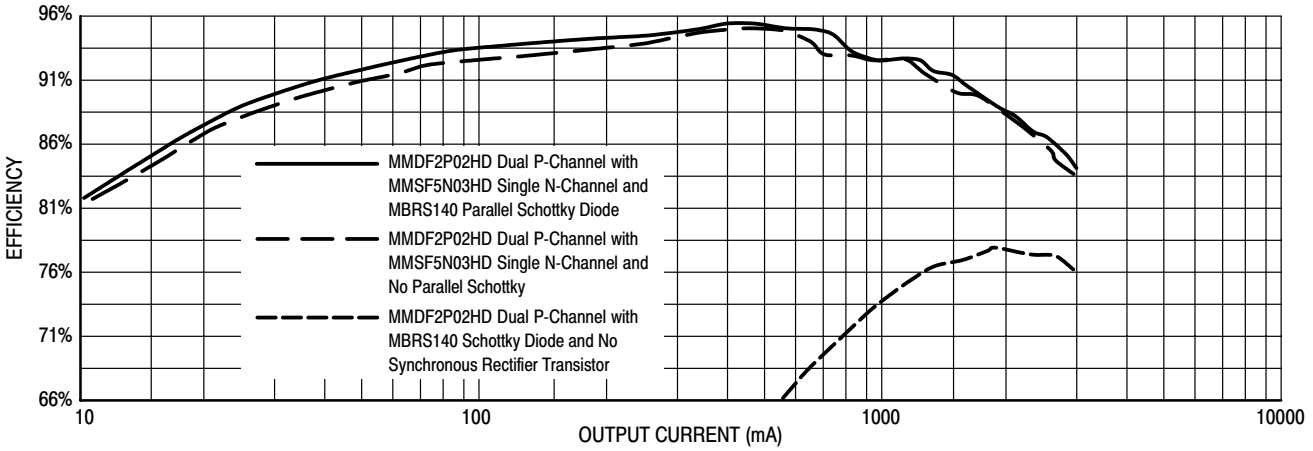


Figure 8. Comparison of Efficiencies Between a Schottky Rectifier and a Synchronous Rectifier

Power Loss Analysis

Loss contributions by the various components with the buck regulator, which employs synchronous rectification, are summarized in Figure 9. This figure is a summary of the power loss contributions of combination 1 in Table 3. The shape of the curve is indicative of the various loss contributions over output current.

The first part of the overall loss curve of Figure 9 has an abrupt downslope. In this area of the curve, low level control currents which power the control and gate drive circuitry are significant when compared to the output current. It is here that the benefits of using HDTMOS transistors (which exhibit low gate capacitance values) result in better overall converter efficiency. Note that at extremely low current levels, the switching losses and control circuitry power losses associated with using a synchronous rectifier transistor will be more than the overall losses of a Schottky diode. These losses are insignificant at higher output currents; however, the current drawn to support control functions becomes more of a factor when the load current is reduced to a comparable level.

The second part of the curve has an increasing slope that indicates increased power loss with increased output current. This is due to power losses of parasitic resistances and the RMS currents traveling through them. These losses tend to dominate with higher currents due to the power relation to the RMS current squared. The resulting effect is lower efficiency.

The three additional curves in Figure 9 show the effect that the parasitic resistances have on efficiency. Note that the $R_{DS(on)}$ of the HDTMOS transistors accounts for a similar amount of loss to those observed in the inductor DCR and series sense resistor (R2 in Figure 7). The added benefit of using low $R_{DS(on)}$, HDTMOS transistors is obvious. Also observe how at the higher currents, almost all of the power loss is due to parasitic resistance.

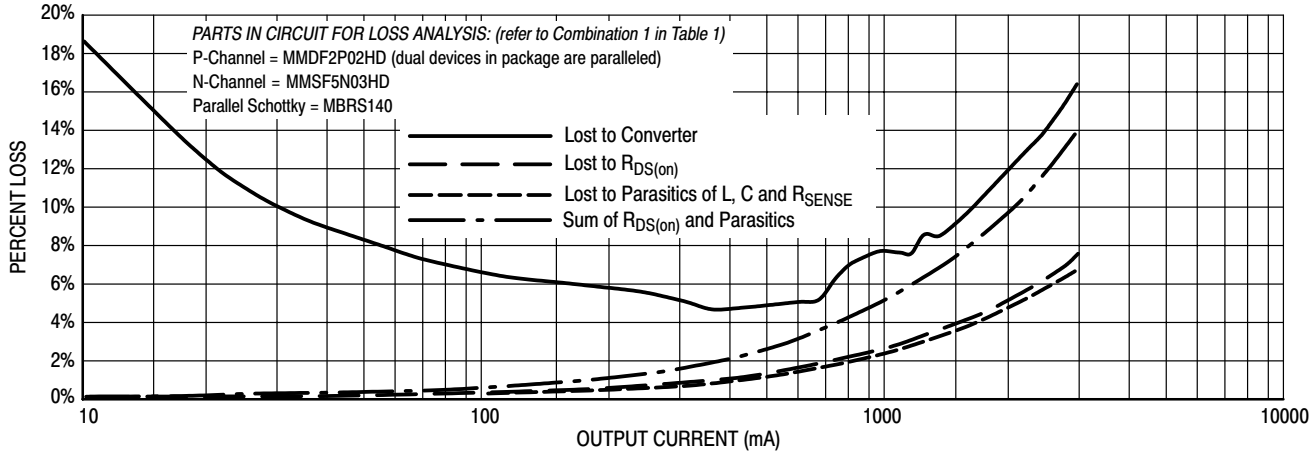


Figure 9. Power Loss Analysis of Main Power Path

Figure 10 is a good example of several factors that occur when using a synchronous rectifier transistor. The curve shows the current through the synchronous rectifier transistor and parallel Schottky. The “dead times” observed are actually created by the LTC1148 integrated circuit in order to avoid shoot through currents that result when both the main switch transistor and the synchronous rectifier transistor are in transition. The LTC1148 tests the gate drive pin states to provide total synchronization.

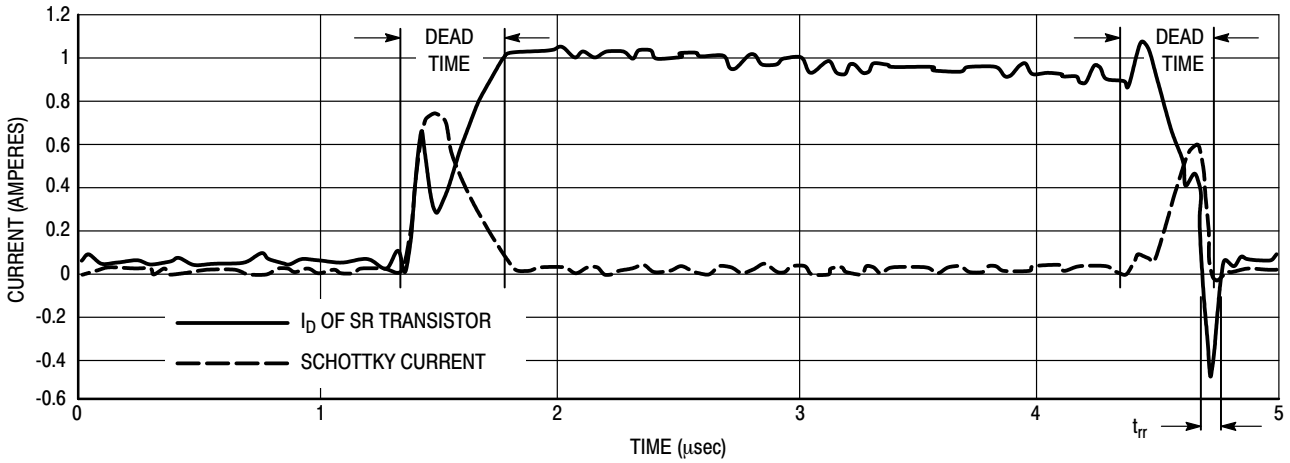


Figure 10. Waveforms of Synchronous Rectifier Transistor Drain Current and Parallel Schottky Current (I_{out} = 1 Amp)

Notice that during the dead times, the Schottky seems to share the current with the body diode of the synchronous rectifier transistor. This is due in part to the parasitics resulting from mounting the Schottky external to the transistor. By doing so, extra parasitic impedances slow the Schottky's ability to turn on and conduct current.

Figure 11 illustrates the reverse recovery times (t_{rr}) of the various combinations of MMSF5N03HD synchronous rectifier transistors and MBRS140 Schottkys for a 1 ampere load. Table 2 summarizes the results obtained in Figure 11. The largest peak current and recovery time occurs when the synchronous rectifier transistor body diode recovers without the presence of the external Schottky. The Schottky alone exhibits the best recovery time characteristic. The Schottky in parallel with the synchronous rectifier transistor helps to quell some of the current peaking and reverse recovery time. A smaller current peak will result in reduced EMI noise.

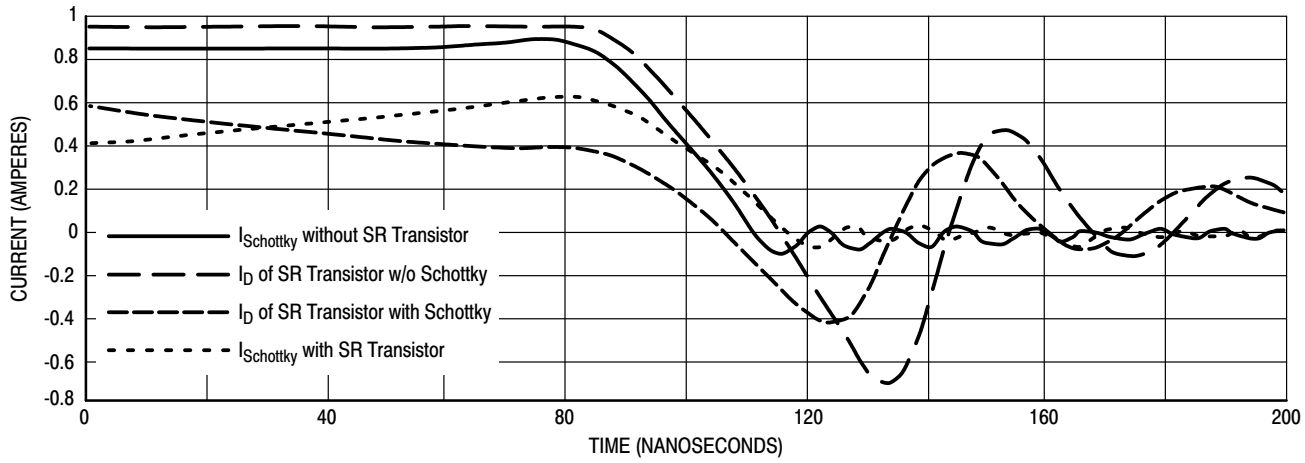


Figure 11. Comparison of t_{rr} Times for Various Arrangements of a Synchronous Rectifier Transistor and Schottky Diode (I_{out} = 1 Amp)

Table 2. Summary of Transistor Arrangements for Figure 10 Efficiency Graph

Rectifier Configuration	t_a	t_b	t_{rr}	Maximum Peak Recovery Current
MBRS140 Schottky Only	4.4 ns	4.8 ns	9.2 ns	128 mA
MMSF5N03HD Transistor Only	18.0 ns	10.8 ns	28.8 ns	734 mA
MMSF5N03HD Transistor (in Parallel with MBRS140 Schottky)	18.0 ns	11.0 ns	29.0 ns	438 mA
MBRS140 Schottky (in Parallel with MMSF5N03HD Transistor)	6.4 ns	1.6 ns	8.0 ns	94 mA

Versatility of the HDTMOS MiniMOS™ Portfolio

The findings resulting from observing the efficiency effects and waveforms with and without the parallel Schottky formed a basis for the configuration of the transistors and rectifier diode combinations used in the analysis of using HDTMOS transistors in the 5 Vdc to 3.3 Vdc buck converter. As a result of these findings, the remainder of this analysis was performed without the parallel Schottky diode. Several combinations of P-Channel and N-Channel HDTMOS devices were inserted into the test circuit and the efficiency was measured. The devices compared offer the designer several solutions to applying the wide portfolio of HDTMOS transistors. Figure 12 shows the resulting efficiency measurements of the various transistor combinations that are illustrated in Table 2.

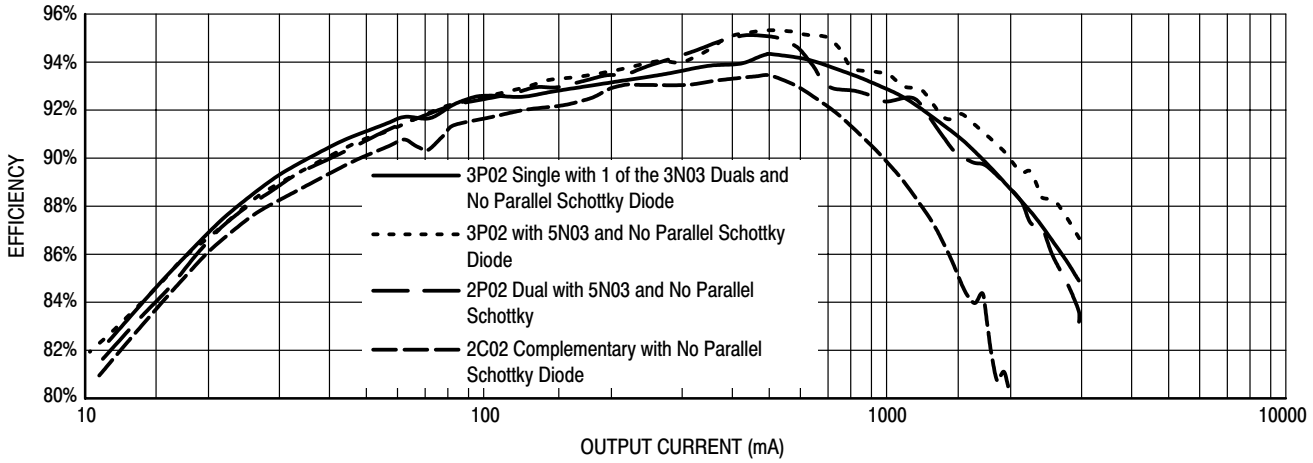


Figure 12. Comparison of Overall Efficiencies of Several Combinations of HDTMOS Transistors in a 5 Vdc to 3.3 Vdc Buck Converter Employing Synchronous Rectifiers

Table 3. Summary of Transistor Arrangements for Figure 10 Efficiency Graph

Combination Number	P-Channel Part Number	N-Channel Part Number	Maximum Measured Efficiency
1	MMDF2P02HD (two devices in package placed in parallel) $R_{DS(on)}$ = 0.18 (per Device)	MMSF5N03HD $R_{DS(on)}$ = 0.04	95.1%
2	MMSF3P02HD $R_{DS(on)}$ = 0.085	MMSF5N03HD $R_{DS(on)}$ = 0.04	95.4%
3	MMSF3P02HD $R_{DS(on)}$ = 0.085	MMDF3N03HD (only one of the two devices in this package were used) $R_{DS(on)}$ = 0.09	94.4%
4	MMDF2C02E (P-Channel Device of Complementary Pair in a Single Package) $R_{DS(on)}$ = 0.18	MMDF2C02E (N-Channel Device of Complementary Pair in a Single Package) $R_{DS(on)}$ = 0.18	93.6%

When observing the curves provided in Figure 12, it is apparent that the combinations differ slightly in measured efficiency. However, efficiency is sometimes sacrificed to accommodate space, cost, reliability and other factors. The following assessment of the curves in Figure 12 and the findings in Table 3 provides some insight into the benefits of the configuration of the various devices into four combinations.

Combination 1: Combination 1 makes use of the MMDF2P02HD transistor that features two P-Channel devices in one SO-8 package. Combining the MMDF2P02HD with the MMSF5N03HD N-Channel device provides for the second lowest combination of $R_{DS(on)}$ values of all four combinations. The resulting maximum efficiency measured is 95.1%. Two observations can be made which make this a favorable combination. First, driving two P-Channel gates versus one does not significantly degrade efficiency at the lower output currents where gate drive effects are greatest (Figure 12). Second, the RMS current carried by each transistor is 0.93 A that is 45.5% of the 2 amp maximum rated average forward current making this combination more reliable and attractive than combination 2 for designs with stringent derating criteria.

Combination 2: Combination 2 replaces the dual P-Channel device (each rated at 2 A) with a single device; the MMSF3P02HD that has a continuous current rating of 3 A. The N-Channel device used remains the same as combination 1. This combination has the best peak and overall measured efficiency. This is due to its lowest overall combined $R_{DS(on)}$ values.

Combination 3: Combination 3 is similar to combination 2 with the exception of the N-Channel device used. The MMSF5N03HD has been replaced with a MMDF3N03HD. The current rating is lower than the previous rating and as is typical of MOSFET transistors, the $R_{DS(on)}$ is slightly greater at 0.04 Ω. However, the MMDF3N03HD has two devices in one package (note that D in the part number stands for dual) and only one device was used leaving the other available for use in other ways. The efficiency measured in combination 3 is not significantly lower than in combination 2 yet the designer has an extra device available for use without using additional board space. This arrangement has many advantages including using the extra device for power management or driving shutdown circuitry.

Combination 4: At first glance, the combination 4 curve appears to exhibit a considerably lower efficiency than the other combinations. In addition, the data appears to indicate the converter ceases to operate at a lower output current. Closer inspection of the part combination reveals the answer. The transistor arrangement is combination 4 in Table 2 and consists of the MMDF2C02E that is a combination P-Channel and N-Channel device *in one package*! The C in the part number denotes complementary devices reside in the package. Combination 4 can provide in excess of 90% efficiency at output currents of nearly 1 amp while eliminating one package form the board.

The comparisons made thus far have concentrated on parts with V_{DSS} ratings of 20 and 30 V. While the higher voltage parts have the advantage of providing efficient 5 Vdc to 3.3 Vdc conversion, they also are useful for providing a 3.3 volt output from existing wall transformer levels of up to 24 V. The inclusion of HDTMOS devices with 12 volt V_{DSS} allows the designer versatility at a minor sacrifice in efficiency as shown in Figure 13. The 12 volt rating for these parts makes them an excellent choice for 5 Vdc to 3.3 Vdc converters.

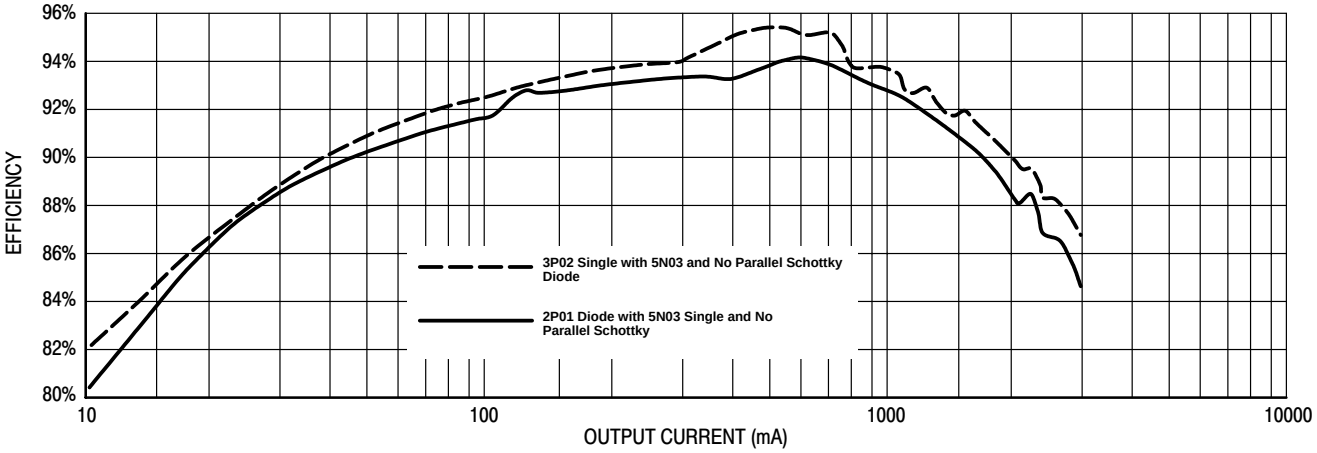


Figure 13. Comparison of Overall Efficiencies of Combination 1 to a Second Measurement Using an HDTMOS Transistors Rated at 12 V V_{DSS}

High Power, 12 Vdc Output Buck Converter

The nonisolated buck regulator employing synchronous rectifiers can be used to provide high power, regulated DC voltages in addition to lower power 3.3 Vdc outputs. Typically higher power converters employ an N-Channel device as the main switching transistor due to the lower $R_{DS(on)}$ exhibited by N-Channel devices when compared to P-Channel devices. Although drive circuitry becomes a little more complex, the gains in efficiency are worth the effort.

A converter capable of 300 watts was tested for efficiency using HDTMOS transistors. Figure 14 shows the schematic of the nonisolated buck converter which provides a 12 Vdc output and accepts inputs of 20 - 30 Vdc.

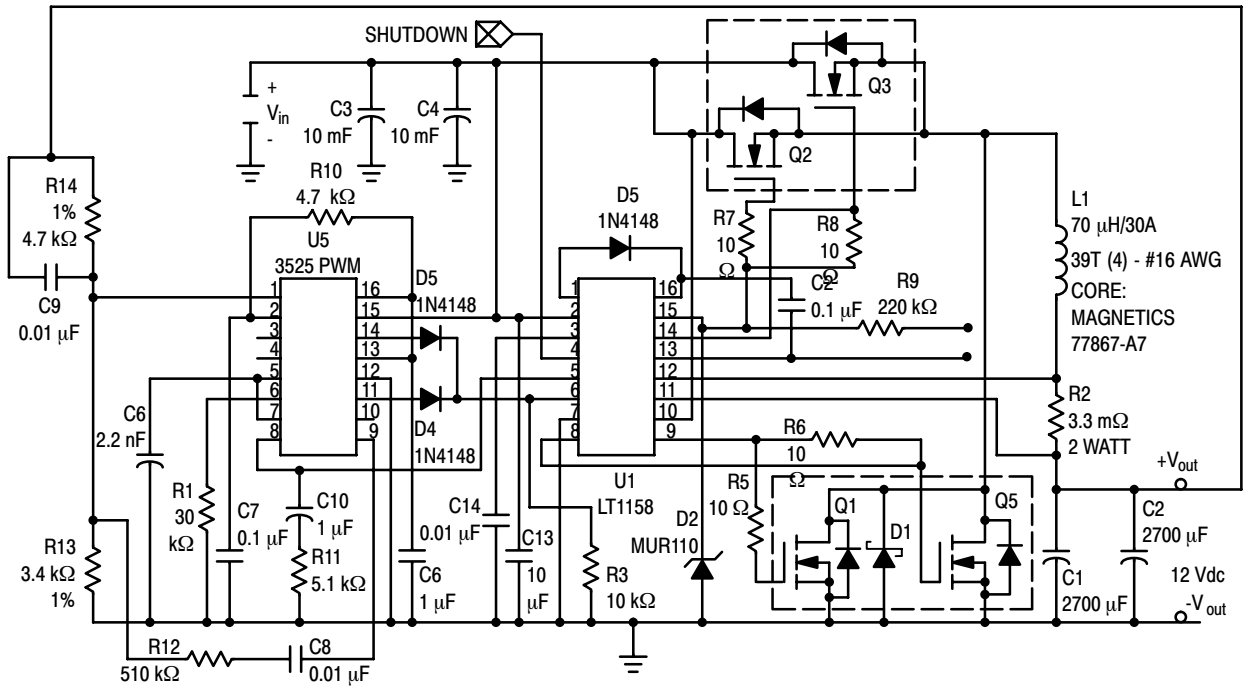


Figure 14. Schematic of a High Power 12 Vdc Output Buck Converter Employing a Synchronous Rectifier

The boxed devices in Figure 14 were interchanged and the overall converter efficiency was measured. Initially the board had two IRFZ44 devices in parallel for both the main switch (Q2 and Q3) and synchronous rectifier transistor (Q1 and Q4). In addition, a MBR745 Schottky diode was in parallel across the synchronous rectifier transistors. Each of the transistors had an $R_{DS(on)}$ value of 28 mΩ. The efficiencies for this arrangement are shown in Figure 15 for a 20 Vdc input and Figure 16 for a 24 Vdc input for outputs up to 120 watts.

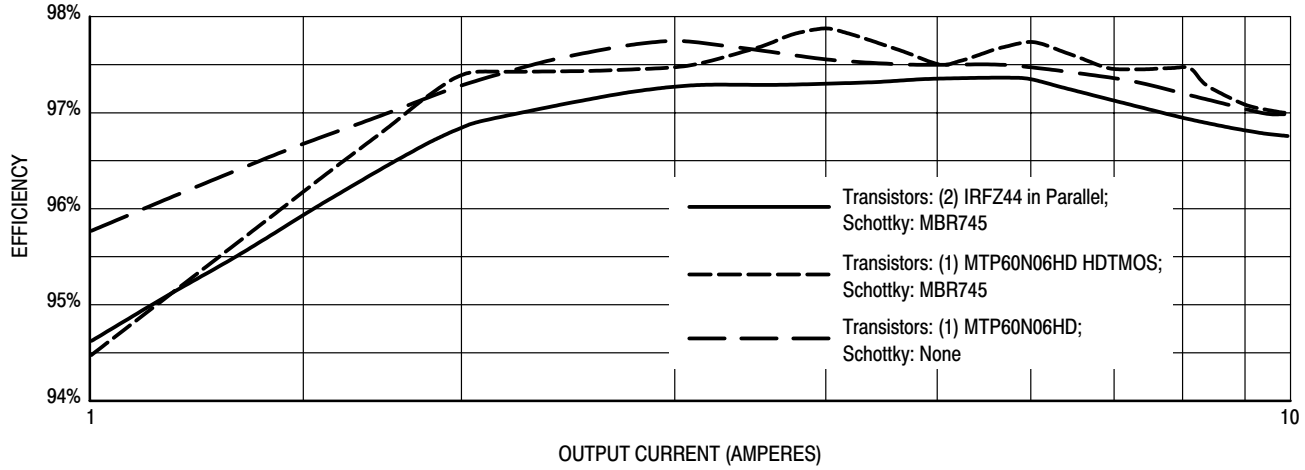


Figure 15. Efficiency of a 120 Watt, 12 Vdc Output Buck Converter (V_{in} = 20 Vdc)

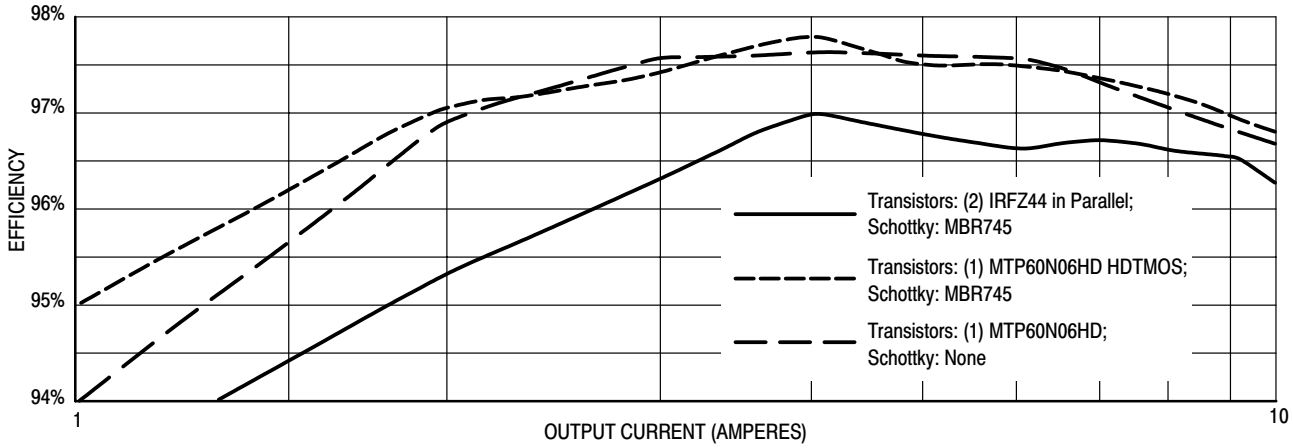


Figure 16. Efficiency of a 120 Watt, 12 Vdc Output Buck Converter (V_{in} = 24 Vdc)

To investigate the performance of HDTMOS transistors, a *single* MTP60N06HD device with a maximum $R_{DS(on)}$ of 14 mΩ was inserted in place of the two IRFZ44 devices in parallel for both the main switch transistor and synchronous rectifier transistor. The MTP60N06HD current and voltage rating closely match those of the IRF44Z. Efficiencies were then measured with and without the MBR745 Schottky in parallel.

As can be seen in Figures 14 and 15, one HDTMOS part can replace an older technology device and an increase in efficiency is realized. Also, as shown before, the favorable body diode characteristics allow the Schottky to be removed without significantly degrading the efficiency. The net result is a reduction in parts count and an increase in overall efficiency and reliability.

Conclusion

The benefit of using HDTMOS transistors in a synchronous rectifier application has been demonstrated. This application makes good use of the low $R_{DS(on)}$ and soft body diode characteristics that are particularly useful in creating efficient 5 Vdc to 3.3 Vdc converters. In addition, HDTMOS transistors are available in a wide portfolio making them useful in meeting demands such as space saving and increased reliability. The result is a reduced part count and a more cost effective solution for providing efficient power conversion at minimal power loss.

Acknowledgments

The work presented here was supported by Linear Technology who provided test boards and demonstration boards for designs based on the LTC1148 and LT1158 synchronous rectifier IC's. The support of the field and applications engineers at LTC was greatly appreciated.

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Appendix 1
LTC1148 Simplified Schematic [9]

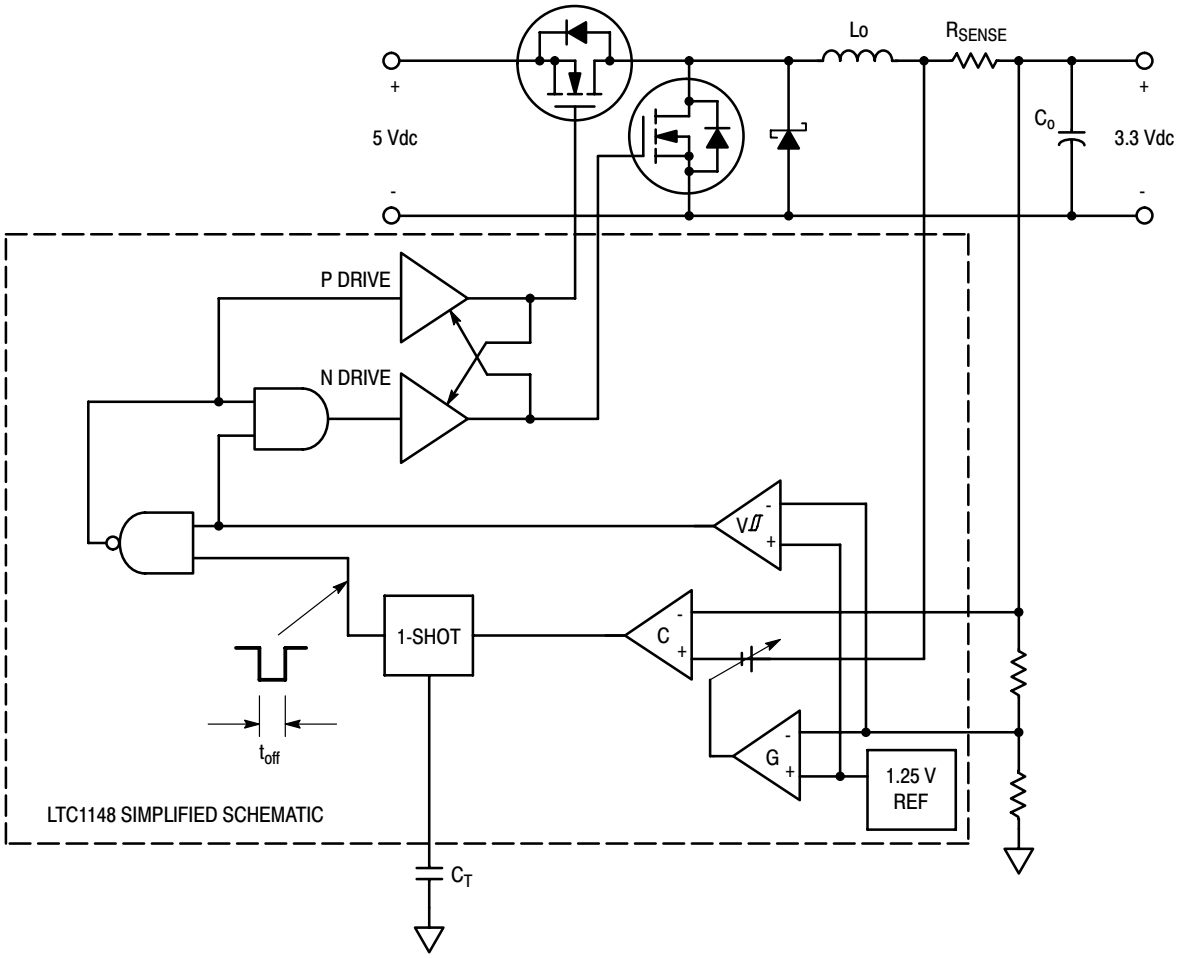

Figure A-1. 5 Vdc to 3.3 Vdc Buck Regulator with LTC1148 Simplified Schematic

Appendix 2
Diode Reverse Recovery Analysis [10]

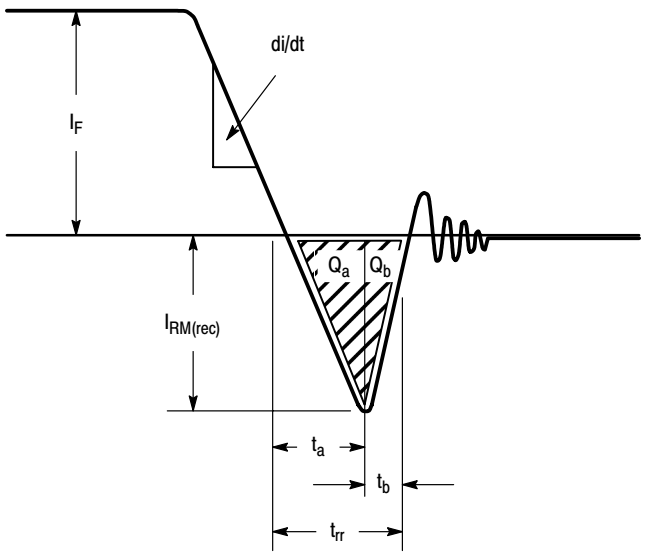

Figure A-2. Reverse Recovery Waveform

t_{rr} = total reverse recovery time
t_a = fall time due to stored minority charge
t_b = application and device dependent
$I_{RM(rec)}$ = peak reverse recovery current

A typical reverse recovery waveform is shown in Figure A-2. The reverse recovery time t_{rr} has been traditionally defined as the time from diode current zero crossing to where the current returns to within 10% of the peak recovery current $I_{RM(rec)}$. This does not give enough information to fully characterize the waveform shape. A better way to characterize the rectifier reverse recovery is to partition the reverse recovery time into two different regions t_a and t_b, as shown in Figure A-2. The t_a time is a function of the forward current and the applied di/dt. A charge can be assigned to this region denoted Q_a, the area under the curve. The t_b portion of the reverse recovery current is not very well understood. Measured t_b times vary greatly with the switch characteristics, circuit parasitics, load inductance and the applied reverse voltage. A relative softness can be defined as the ratio of t_b to t_a. General purpose rectifiers are very soft (softness factor of about 1.0), fast recovery diodes are fairly soft (softness factor of about 0.5) and ultrafast rectifiers are very abrupt (softness factor of about 0.2).

Appendix 3
5 Vdc to 3.3 Vdc Buck Converter Efficiency Test Equipment Configuration

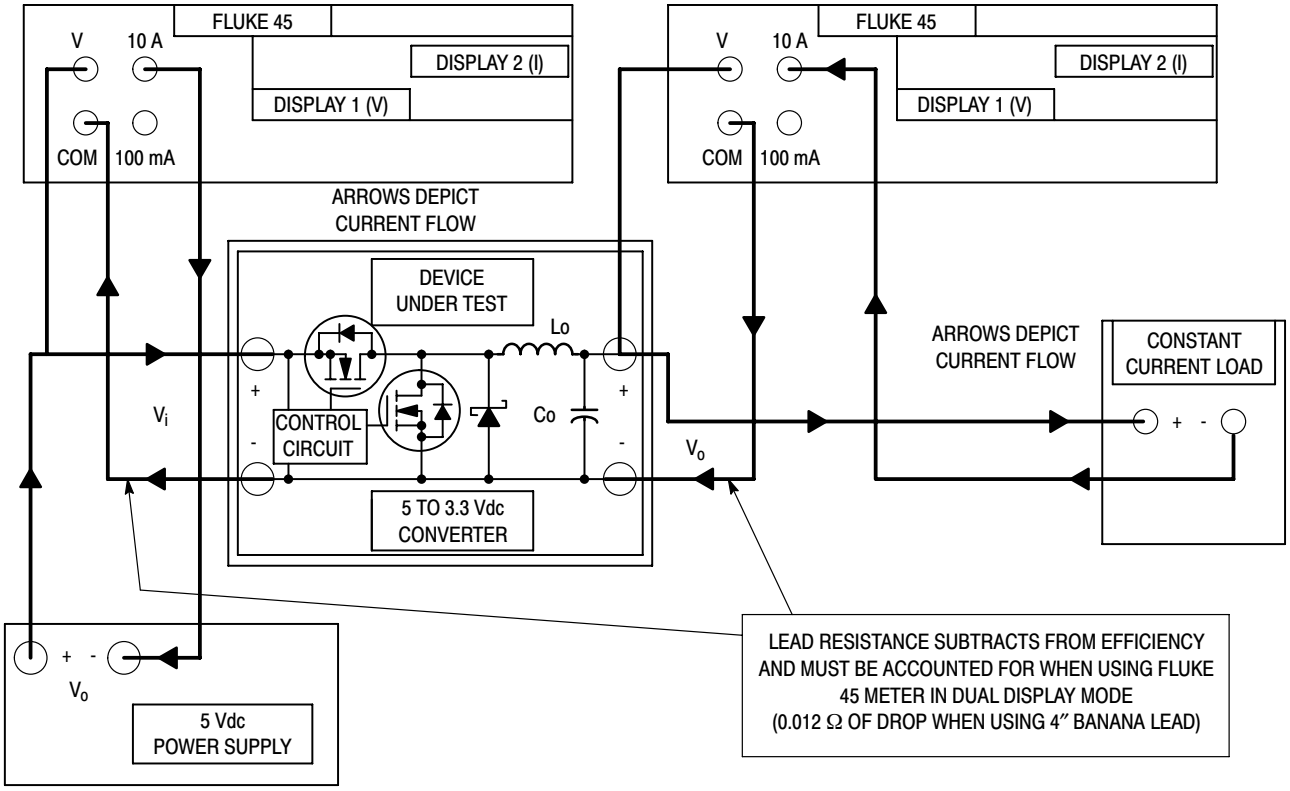

Figure A-3. Efficiency Test Equipment Configuration

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