

# MC10E157, MC100E157

## 5 V ECL Quad 2:1 Multiplexer

The MC10E/100E157 contains four 2:1 multiplexers with differential outputs. The output data are controlled by the individual Select (SEL) inputs. The individual select control makes the devices well suited for random logic designs.

The 100 Series contains temperature compensation.

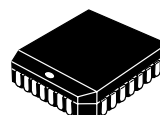
- Individual Select Controls
- 550 ps Max. D to Output
- 800 ps Max. SEL to Output
- PECL Mode Operating Range:  $V_{CC} = 4.2\text{ V}$  to  $5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V}$  to  $-5.7\text{ V}$
- Internal Input  $50\text{ K}\Omega$  Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection: Human Body Model;  $> 1\text{ KV}$ , Machine Model;  $> 75\text{ V}$
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 137 devices



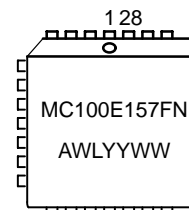
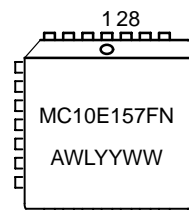
**ON Semiconductor®**

<http://onsemi.com>

### MARKING DIAGRAMS



**PLCC-28  
FN SUFFIX  
CASE 776**



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

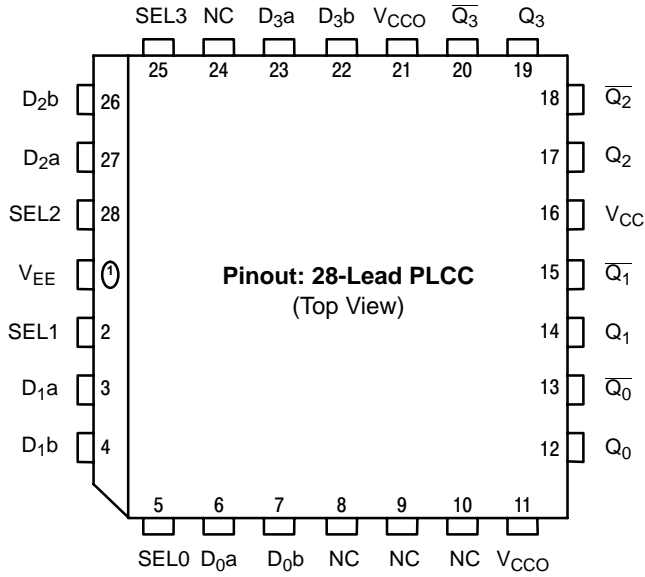
### ORDERING INFORMATION

Device	Package	Shipping†
MC10E157FN	PLCC-28	37 Units/Rail
MC10E157FNR2	PLCC-28	500 Units/Reel
MC100E157FN	PLCC-28	37 Units/Rail
MC100E157FNR2	PLCC-28	500 Units/Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC10E157, MC100E157

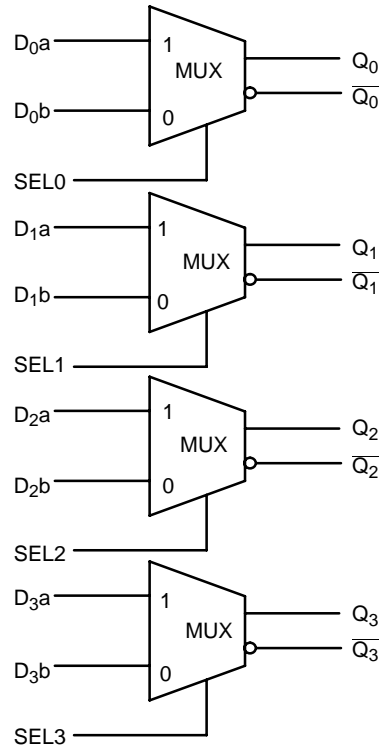
## LOGIC DIAGRAM AND PINOUT ASSIGNMENT



\* All  $V_{CC}$  and  $V_{CCO}$  pins are tied together on the die.

Warning: All  $V_{CC}$ ,  $V_{CCO}$ , and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

## LOGIC DIAGRAM



## PIN DESCRIPTION

PIN	FUNCTION
$D_{0a} - D_{3a}$	ECL Input Data a
$D_{0b} - D_{3b}$	ECL Input Data b
$SEL0 - SEL3$	ECL Select Inputs
$Q_0 - Q_3, \overline{Q_0} - \overline{Q_3}$	ECL Differential Outputs
$V_{CC}, V_{CCO}$	Positive Supply
$V_{EE}$	Negative Supply
NC	No Connect

## TRUTH TABLE

SEL	DATA
H	a
L	b

## MC10E157, MC100E157

### MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC2}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_I$	PECL Mode Input Voltage	$V_{EE} = 0\text{ V}$	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	$V_{CC} = 0\text{ V}$	$V_I \geq V_{EE}$	-6	V
$I_{out}$	Output Current	Continuous Surge		50	mA
				100	mA
$T_A$	Operating Temperature Range			0 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 LFPM	28 PLCC	63.5	°C/W
		500 LFPM	28 PLCC	43.5	°C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	28 PLCC	22 to 26	°C/W
$T_{sol}$	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

# MC10E157, MC100E157

## 10E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$ ; $V_{EE} = 0.0\text{ V}$ (Note 2)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		32	38		32	38		32	38	mA
$V_{OH}$	Output HIGH Voltage (Note 3)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 3)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
$V_{IH}$	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
$V_{IL}$	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
$I_{IH}$	Input HIGH Current			200 150			200 150			200 150	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .

3. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .

## 10E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ (Note 4)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		32	38		32	38		32	38	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 5)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
$V_{IH}$	Input HIGH Voltage	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
$V_{IL}$	Input LOW Voltage	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
$I_{IH}$	Input HIGH Current			200 150			200 150			200 150	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .

5. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .

# MC10E157, MC100E157

## 100E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$ ; $V_{EE} = 0.0\text{ V}$ (Note 6)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		32	38		32	38		37	44	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 7)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
$V_{IH}$	Input HIGH Voltage	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
$V_{IL}$	Input LOW Voltage	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
$V_{BB}$	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
$I_{IH}$	Input HIGH Current			200 150			200 150			200 150	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .

7. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .

## 100E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$ ; $V_{EE} = -5.0\text{ V}$ (Note 8)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		32	38		32	38		37	44	mA
$V_{OH}$	Output HIGH Voltage (Note 9)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
$V_{OL}$	Output LOW Voltage (Note 9)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
$V_{IH}$	Input HIGH Voltage	-1165	-1025	-880	-1165	-1025	-880	-1165	-1025	-880	mV
$V_{IL}$	Input LOW Voltage	-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1645	-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$I_{IH}$	Input HIGH Current			200 150			200 150			200 150	$\mu\text{A}$ $\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .

9. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .

# MC10E157, MC100E157

**AC CHARACTERISTICS**  $V_{CCx} = 5.0\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CCx} = 0.0\text{ V}$ ;  $V_{EE} = -5.0\text{ V}$  (Note 10)

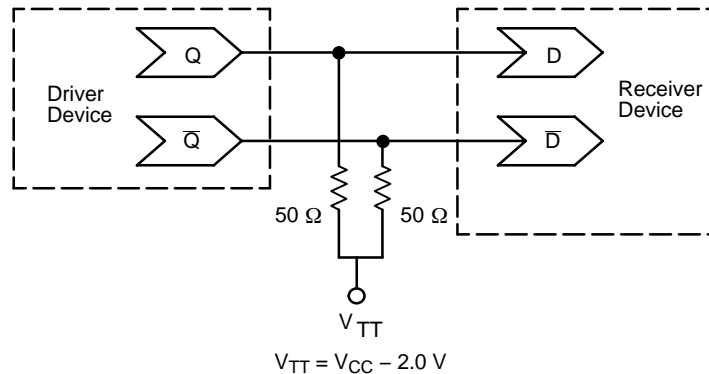
Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency	700	1100		700	1100		700	1100		MHz
$t_{PLH}$	Propagation Delay to Output D SEL	220	380	550	220	380	550	220	380	550	ps
$t_{PHL}$		425	600	800	425	600	800	425	600	800	
$t_{SKEW}$	Within-Device Skew (Note 11)		70			70			70		ps
$t_{JITTER}$	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
$t_r$	Rise/Fall Times (20 - 80%)	275	400	650	275	400	650	275	400	650	ps
$t_f$											

NOTE: Devices are designed to meet the AC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

10. 10 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.06\text{ V}$ .

100 Series:  $V_{EE}$  can vary  $-0.46\text{ V} / +0.8\text{ V}$ .

11. Within-device skew is defined as identical transitions on similar paths through a device.



**Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)**

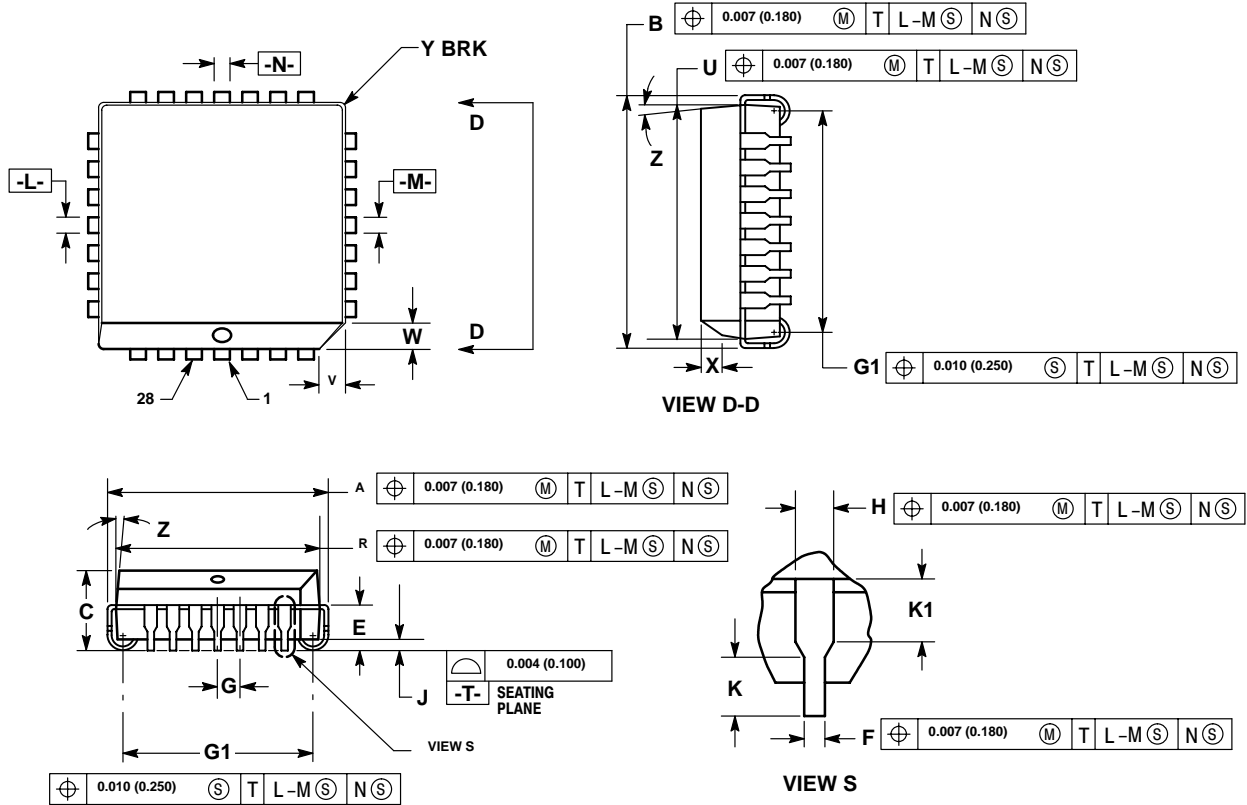
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC10E157, MC100E157

## PACKAGE DIMENSIONS

PLCC-28  
FN SUFFIX  
PLASTIC PLCC PACKAGE  
CASE 776-02  
ISSUE E




### NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

# MC10E157, MC100E157

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA

**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada

**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada

**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center

2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051

**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.