

MC100LVELT23

3.3 V Dual Differential LVPECL/LVDS to LVTTTL Translator

The MC100LVELT23 is a dual differential LVPECL/LVDS to LVTTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the LVELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The LVELT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the LVELT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100LVELT23 can accept any standard differential LVPECL input referenced from a V_{CC} of +3.3 V.

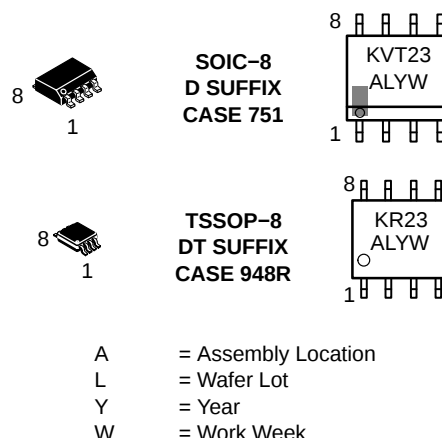
- 2.0 ns Typical Propagation Delay
- Maximum Frequency > 180 MHz
- Differential LVPECL Inputs
- PECL Mode Operating Range: $V_{CC} = 3.0$ V to 3.8 V with GND = 0 V
- 24 mA LVTTTL Outputs
- Flow Through Pinouts
- Internal Pulldown and Pullup Resistors
- Pb-Free Package is Available



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MARKING DIAGRAMS*



*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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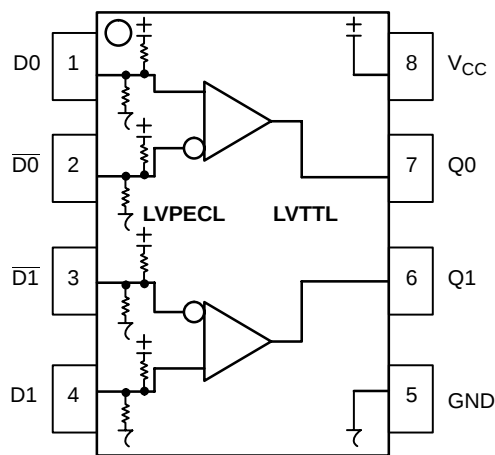


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
Q0, Q1	LVTTTL Outputs
D0*, D1*	
D0*, D1*	Differential LVPECL Inputs
V _{CC}	Positive Supply
GND	Ground

** Pins will default to $V_{CC}/2$ when left open.

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		50 kΩ
Internal Input Pullup Resistor		50 kΩ
ESD Protection	Human Body Model	> 1500 V
	Machine Model	> 100 V
	CDM	> 2000 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in
Transistor Count		91
Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. Refer to Application Note AND8003/D for additional information.

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Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Power Supply	GND = 0 V		3.8	V
V _I	Input Voltage	GND = 0 V, V _I not more positive than V _{CC}		3.8	V
I _{out}	Output Current	Continuous Surge		50 100	mA
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	SOIC–8 SOIC–8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction–to–Case)	Standard Board	SOIC–8	41 to 44 ± 5%	°C/W
θ _{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	TSSOP–8 TSSOP–8	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction–to–Case)	Standard Board	TSSOP–8	41 to 44 ± 5%	°C/W
T _{sol}	Solder Temperature	< 2 to 3 Seconds: 245°C desired		265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 3. LVPECL INPUT DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0 V (Note 2)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{CCH}	Power Supply Current (Outputs set to HIGH)	10	18	25	10	18	25	10	18	25	mA
I _{CCL}	Power Supply Current (Outputs set to LOW)	15	26	36	15	26	36	15	26	36	mA
V _{IH}	Input HIGH Voltage (Note 4)	2135		2420	2135		2420	2135		2420	mV
V _{IL}	Input LOW Voltage (Note 4)	1490		1825	1490		1825	1490		1825	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Notes 3 and 4)	1.2		V _{CC}	1.2		V _{CC}	1.2		V _{CC}	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	$\bar{D}$ –150			–150			–150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. All values vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
3. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.
4. LVTTTL output R_L = 500 Ω to GND.

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Table 4. LVTTTL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $GND = 0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ($I_{OH} = -3.0\text{ mA}$) (Note 6)	2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage ($I_{OL} = 24\text{ mA}$) (Note 6)			0.5			0.5			0.5	V
I_{OS}	Output Short Circuit Current	-180		-50	-180		-50	-180		-50	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. All values vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3\text{ V}$.

6. LVTTTL output $R_L = 500\ \Omega$ to GND.

Table 5. AC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $GND = 0\text{ V}$ (Notes 7, 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F_{max}	Maximum Toggle Frequency (Note 9)	180			180			180			MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	1.0	1.5	2.5	1.0	1.7	2.5	1.0	1.7	2.5	ns
t_{SK++} , t_{SK--} , t_{SKPP}	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 10)		15 35 70	60 80 500		15 40 70	70 80 500		30 40 140	125 80 500	ps
t_{JITTER}	Random Clock Jitter (RMS)		4.0	10		4.0	10		4.0	10	ps
V_{PP}	Input Voltage Swing (Differential Configuration) (Note 11)	200	800	1000	200	800	1000	200	800	1000	mV
t_r , t_f	Output Rise/Fall Times (0.8 V – 2.0 V) $Q, \bar{Q}$	330	600	900	330	600	900	330	650	900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. All values vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3\text{ V}$.

8. LVTTTL output $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND. Refer to Figure 2.

9. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

10. Skews are measured between outputs under identical conditions.

11. 200 mV input guarantees full logic swing at the output.

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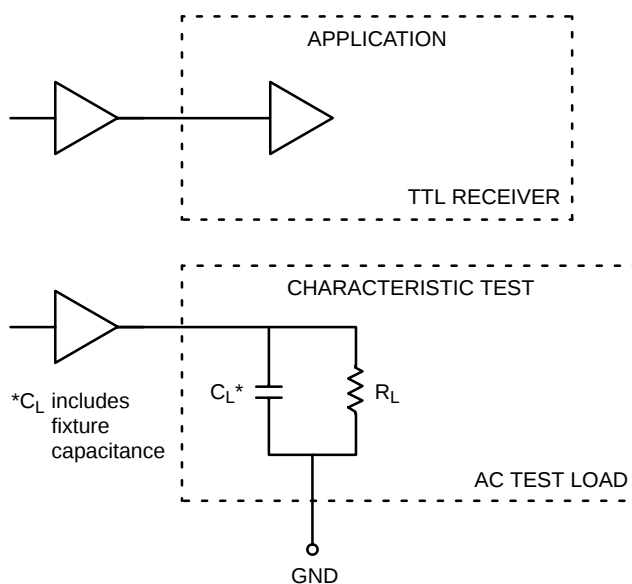


Figure 2. TTL Output Loading Used for Device Evaluation

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100LVELT23D	SOIC-8	98 Units / Rail
MC100LVELT23DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100LVELT23DR2	SOIC-8	2500 / Tape & Reel
MC100LVELT23DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100LVELT23DT	TSSOP-8	98 Units / Rail
MC100LVELT23DTRG	TSSOP-8 (Pb-Free)	98 Units / Rail
MC100LVELT23DTR2	TSSOP-8	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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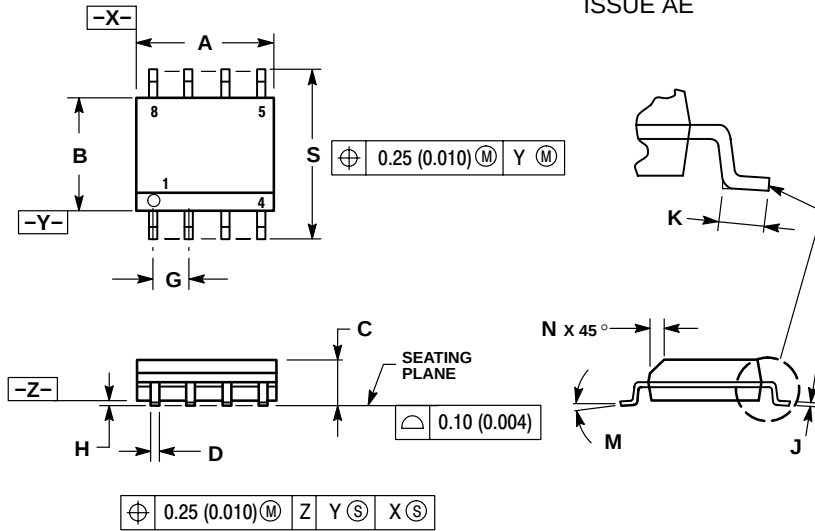
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SOIC-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-07
ISSUE AE

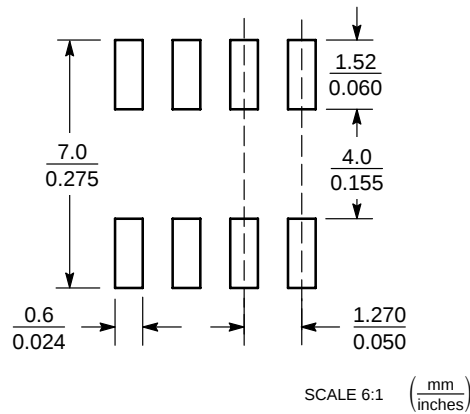


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



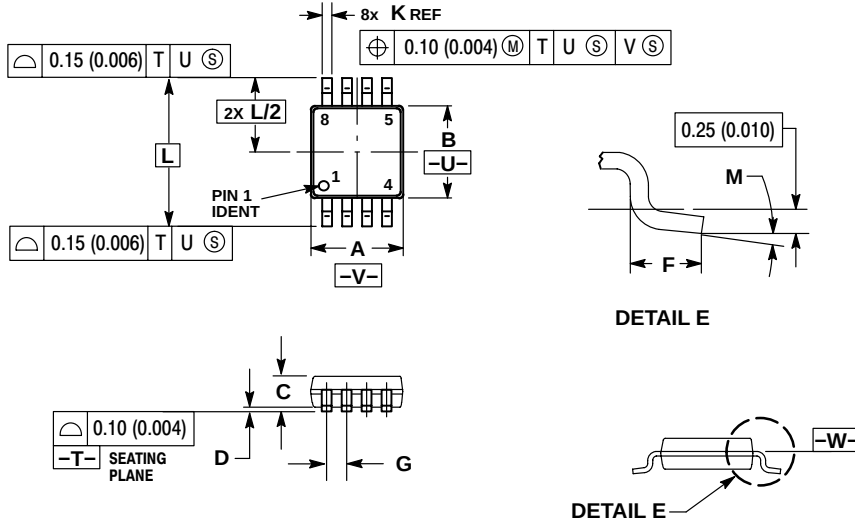
SO-8

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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