

MC100LVEP14

2.5V / 3.3V 1:5 Differential ECL/PECL/HSTL Clock Driver

The MC100LVEP14 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP14 is operating under PECL conditions.

The LVEP14 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into $50\ \Omega$ even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable (\overline{EN}) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

The MC100LVEP14, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVEP14 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single-ended CLK input pin operation is limited to a $V_{CC} \geq 3.0\ \text{V}$ in PECL mode, or $V_{EE} \leq -3.0\ \text{V}$ in NECL mode. Designers can take advantage of the LVEP14's performance to distribute low skew clocks across the backplane or the board.

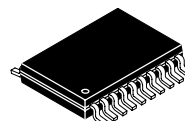
- 100 ps Device-to-Device Skew
- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode:
 $V_{CC} = 2.375\ \text{V}$ to $3.8\ \text{V}$ with $V_{EE} = 0\ \text{V}$
- NECL Mode:
 $V_{CC} = 0\ \text{V}$ with $V_{EE} = -2.375\ \text{V}$ to $-3.8\ \text{V}$
- LVDS Input Compatible
- Open Input Default State
- These devices are manufactured with a Pb-Free external lead finish only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



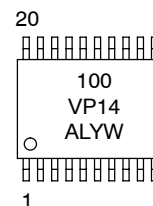
ON Semiconductor®

<http://onsemi.com>



TSSOP-20
DT SUFFIX
CASE 948E

MARKING DIAGRAM*



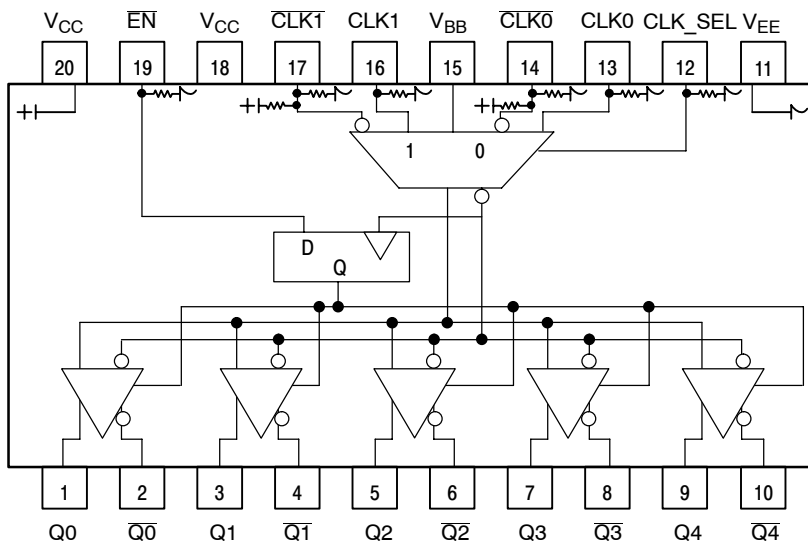
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC100LVEP14



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
CLK0*, $\overline{CLK0}$ **	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{CLK1}$ **	ECL/PECL/HSTL CLK Input
Q0:4, $\overline{Q0}$:4	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
\overline{EN} *	ECL Sync Enable
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

*Pins will default low when left open.

**Pins will default to $V_{CC}/2$ when left open.

Table 2. FUNCTION TABLE

CLK0	CLK1	CLK_SEL	\overline{EN}	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

On next negative transition of CLK0 or CLK1

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	37.5 k Ω
ESD Protection	Human Body Model > 2 kV Machine Model > 100 V Charged Device Model > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	357 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MC100LVEP14

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-20 TSSOP-20	140 100	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-20	23 to 41	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 5. 100LVEP DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V _{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V _{OL}	Output LOW Voltage (Note 3)	555	730	900	555	730	900	555	730	900	mV
V _{IH}	Input HIGH Voltage (Single-Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
V _{IL}	Input LOW Voltage (Single-Ended) (Note 4)	555		900	555		900	555		900	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	1.2		2.5	1.2		2.5	1.2		2.5	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	CLK -150			0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to -1.3 V.
- All loading with 50 Ω to V_{CC} - 2.0 V.
- Do not use V_{BB} at V_{CC} < 3.0 V.
- V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC100LVEP14

Table 6. 100LVEP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 7)	1355	1530	1700	1355	1530	1700	1355	1530	1700	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1700	1355		1700	1355		1700	mV
V_{BB}	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	CLK $\overline{\text{CLK}}$	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925 V to -0.5 V.
7. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
8. Single-ended input operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.
9. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. 100LVEP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	45	60	75	45	60	75	45	60	95	mA
V_{OH}	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 11)	-1945	-1770	-1600	-1945	-1770	-1600	-1945	-1770	-1600	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1600	-1945		-1600	-1945		-1600	mV
V_{BB}	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	$V_{EE}+1.2$		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	CLK $\overline{\text{CLK}}$	0.5 -150		0.5 -150			0.5 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with V_{CC} .
11. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.
12. Single-ended input operation is limited to $V_{EE} \leq 3.0\text{ V}$ in NECL mode.
13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

MC100LVEP14

Table 8. DC CHARACTERISTICS, HSTL $V_{CC} = 2.375\text{ V to }3.8\text{ V}$, $V_{EE} = 0\text{ V}$

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage	1200			1200			1200			mV
V_{IL}	Input LOW Voltage			400			400			400	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 9. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V to }-3.8\text{ V}$ or $V_{CC} = 2.375\text{ V to }3.8\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude @ 2.5 GHz (Figure 2)	330	425		280	375		230	295		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output Differential	300	375	425	300	400	475	300	430	525	ps
t_{skew}	Within-Device Skew Device-to-Device Skew (Note 15)		10 100	25 125		15 150	25 175		15 200	25 225	ps
t_s t_h	Setup Time Hold Time	\overline{EN} \overline{EN}	100 200	50 140	100 200	50 140		100 200	50 140		ps
t_{JITTER}	CLOCK Random Jitter (RMS) $\leq 2.5\text{ GHz}$		0.5	< 1.6		0.5	< 1.6		0.5	< 1.6	ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	125	165	225	125	180	250	125	200	275	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

15. Skew is measured between outputs under identical transitions.

MC100LVEP14

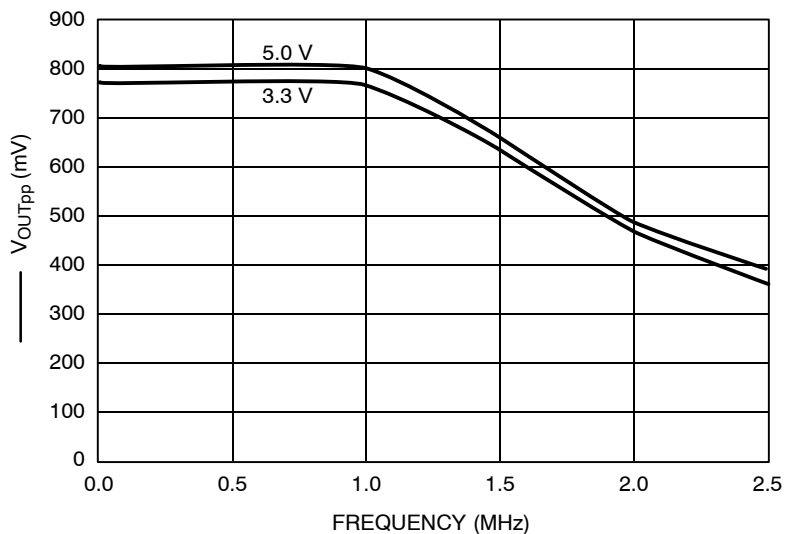


Figure 2. Typical V_{OUTpp} (mV) versus Frequency (MHz) @ 25°C

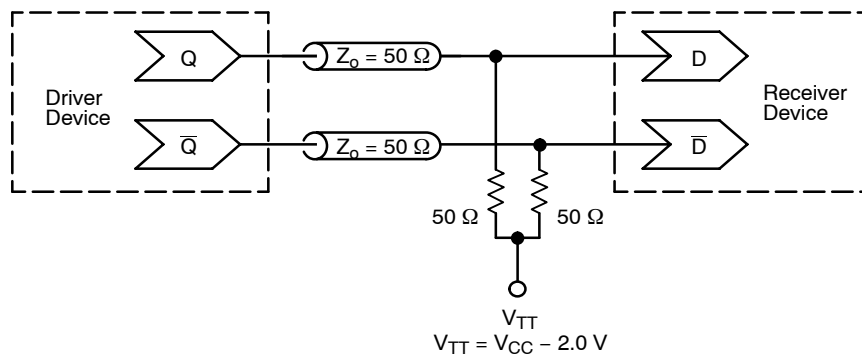


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100LVEP14DT	TSSOP-20*	75 Units / Reel
MC100LVEP14DTR2	TSSOP-20*	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC100LVEP14

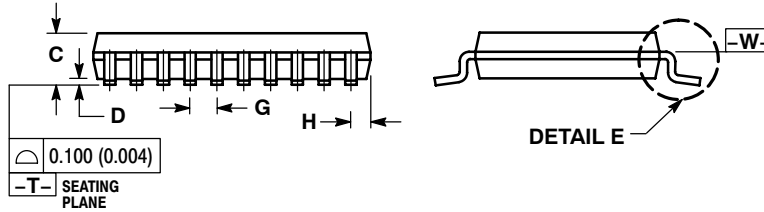
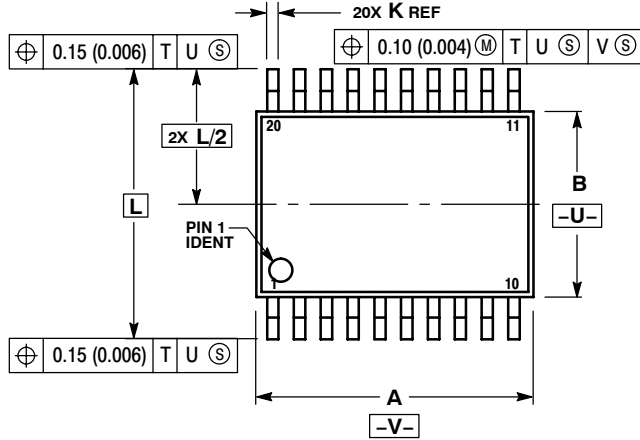
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC100LVEP14

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.