

MC10216

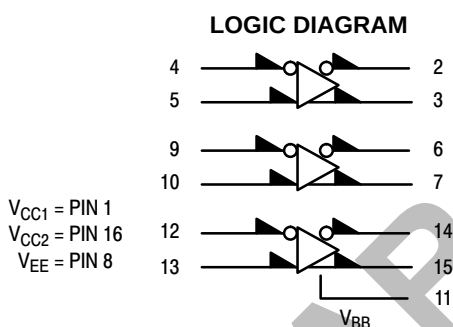
High Speed Triple Line Receiver

The MC10216 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

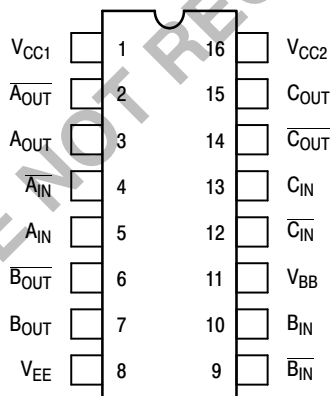
Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

- $P_D = 100 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 1.8 \text{ ns typ (Single ended)}$
- $t_r = 1.5 \text{ ns typ (Differential)}$
- $t_r, t_f = 1.5 \text{ ns typ (20\%–80\%)}$



* V_{BB} to be used to supply bias to the MC10216 only and bypassed (when used) with $0.01 \mu\text{F}$ to $0.1 \mu\text{F}$ capacitor.
 When the input pin with bubble goes positive, it's respective output pin with bubble goes positive.

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.

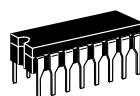
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



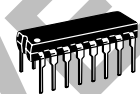
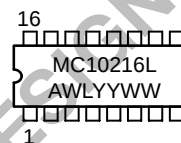
ON Semiconductor

<http://onsemi.com>

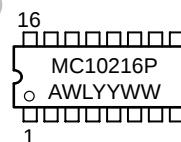
MARKING DIAGRAMS



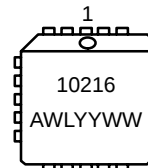
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648



PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10216L	CDIP-16	25 Units / Rail
MC10216P	PDIP-16	25 Units / Rail
MC10216FN	PLCC-20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		27		20	25		27	mAdc
Input Current	I _{inH}	4		180			115		115	μAdc
	I _{CBO}	4 9		1.5 1.5			1.0 1.0		1.0 1.0	μAdc
Output Voltage Logic 1	V _{OH}	2 3	-1.060 -1.060	-0.890 -0.890	-0.960 -0.960		-0.810 -0.810	-0.890 -0.890	-0.700 -0.700	Vdc
Output Voltage Logic 0	V _{OL}	2 3	-1.890 -1.890	-1.675 -1.675	-1.850 -1.850		-1.650 -1.650	-1.825 -1.825	-1.615 -1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	2 3	-1.080 -1.080		-0.980 -0.980			-0.910 -0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	2 3		-1.655 -1.655			-1.630 -1.630		-1.595 -1.595	Vdc
Reference Voltage	V _{BB}	11	-1.420	-1.280	-1.350		-1.230	-1.295	-1.150	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t ₄₊₂₊	2	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	
	t ₄₋₂₋	2	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	
	t ₄₊₃₋	3	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	
	t ₄₋₃₊	3	1.0	2.6	1.0	1.8*	2.5	1.0	2.8	
Rise Time (20 to 80%)	t ₂₊	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	
	t ₃₊	3	1.0	2.6	1.0	1.5	2.5	1.0	2.8	
Fall Time (20 to 80%)	t ₂₋	2	1.0	2.6	1.0	1.5	2.5	1.0	2.8	
	t ₃₋	3	1.0	2.6	1.0	1.5	2.5	1.0	2.8	

* Delay is 1.5ns when inputs are driven differentially.
 Delay is 1.8ns when inputs are driven single ended.

ELECTRICAL CHARACTERISTICS (continued)

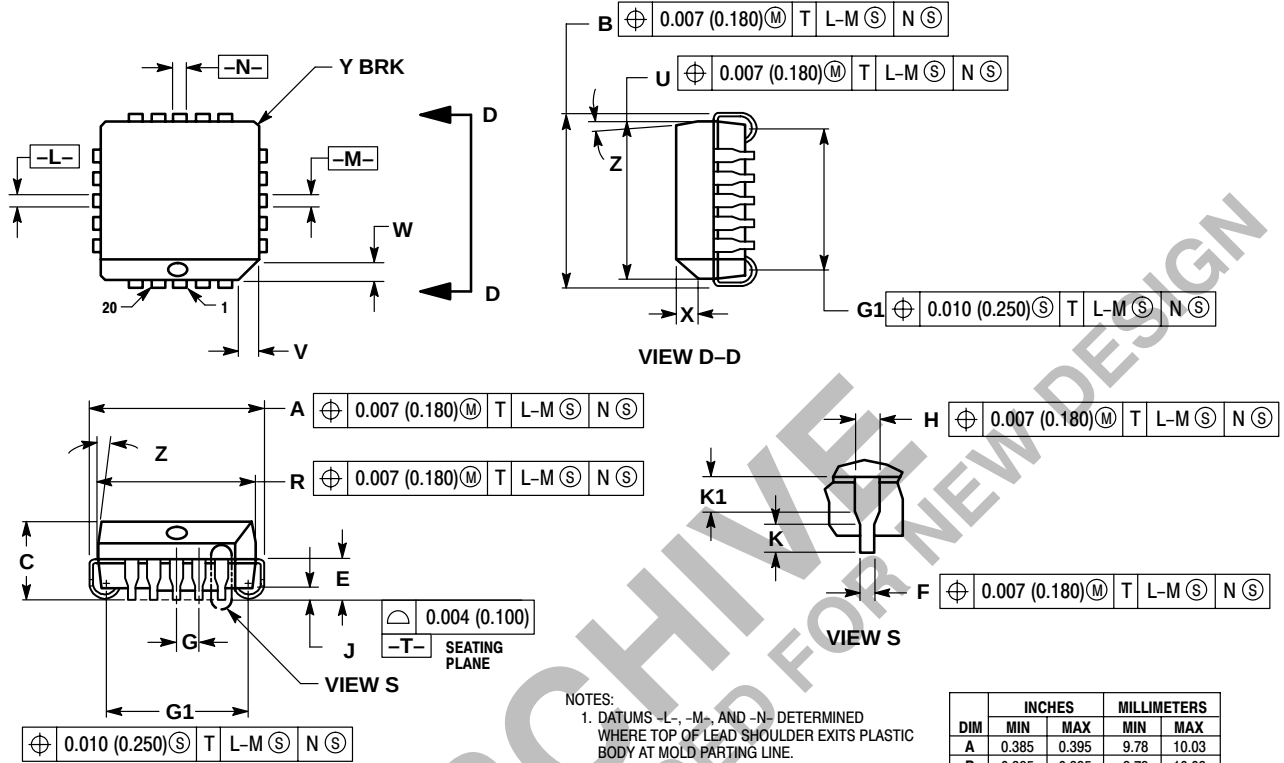
@ Test Temperature			TEST VOLTAGE VALUES (Volts)						(V _{CC}) Gnd	
			V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAMax}	V _{BB}	V _{EE}		
			−0.890	−1.890	−1.205	−1.500	From Pin 11	−5.2		
			+25°C	−0.810	−1.850	−1.105		−1.475		−5.2
			+85°C	−0.700	−1.825	−1.035		−1.440		−5.2
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW						(V _{CC}) Gnd	
			V _{IHmax}	V _{ILmin}	V _{IHAMin}	V _{ILAMax}	V _{BB}	V _{EE}		
Power Supply Drain Current	I _E	8	4, 9, 12				5, 10, 13	8	1, 16	
Input Current	I _{inH}	4	4	9, 12			5, 10, 13	8	1, 16	
	I _{CBO}	4 9		9, 12 4, 12			5, 10, 13 5, 10, 13	8, 4 8, 9	1, 16	
Output Voltage Logic 1	V _{OH}	2	4	9, 12			5, 10, 13	8	1, 16	
		3	9, 12	4			5, 10, 13	8	1, 16	
Output Voltage Logic 0	V _{OL}	2	9, 12	4			5, 10, 13	8	1, 16	
		3	4	9, 12			5, 10, 13	8	1, 16	
Threshold Voltage Logic 1	V _{OHA}	2		9, 12	4		5, 10, 13	8	1, 16	
		3	9, 12			4	5, 10, 13	8	1, 16	
Threshold Voltage Logic 0	V _{OLA}	2		9, 12		4	5, 10, 13	8	1, 16	
		3	9, 12		4		5, 10, 13	8	1, 16	
Reference Voltage	V _{BB}	11					5, 10, 13	8	1, 16	
Switching Times (50Ω Load)					Pulse In	Pulse Out		−3.2 V	+2.0 V	
Propagation Delay	t ₄₊₂₊	2			4	2	5, 10, 13	8	1, 16	
	t _{4−2−}	2			4	2	5, 10, 13	8	1, 16	
	t _{4+3−}	3			4	3	5, 10, 13	8	1, 16	
	t _{4−3+}	3			4	3	5, 10, 13	8	1, 16	
Rise Time (20 to 80%)	t ₂₊	2			4	2	5, 10, 13	8	1, 16	
	t ₃₊	3			4	3	5, 10, 13	8	1, 16	
Fall Time (20 to 80%)	t _{2−}	2			4	2	5, 10, 13	8	1, 16	
	t _{3−}	3			4	3	5, 10, 13	8	1, 16	

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10216

PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C

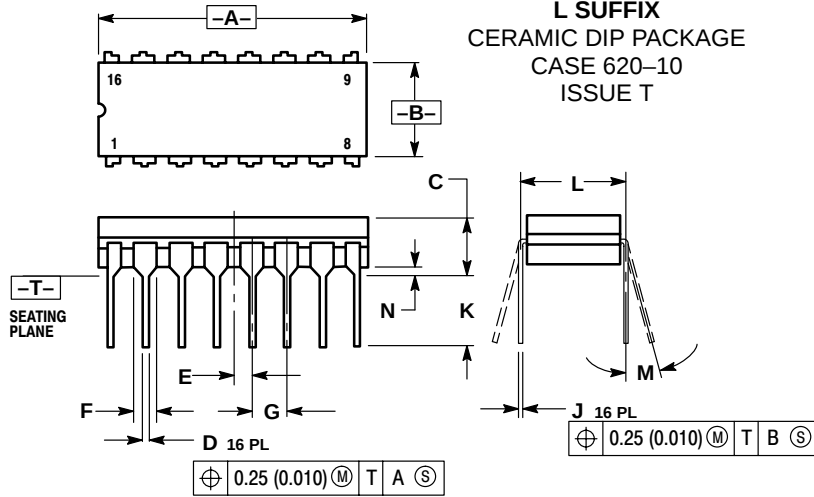


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC	1.27 BSC		
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10216

PACKAGE DIMENSIONS

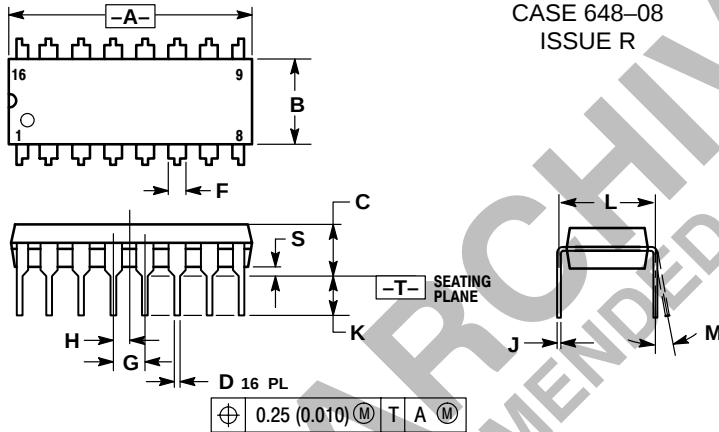
CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
J	0.125	0.170	3.18	4.31
K	0.300 BSC		7.62 BSC	
L	0°	15°	0°	15°
M	0.020	0.040	0.51	1.01
N				

PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

Notes

ARCHIVE
DEVICE NOT RECOMMENDED FOR NEW DESIGN

Notes

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