# Dual Binary to 1-of-4 Decoder/Demultiplexer

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the "high" state, and the MC14556B has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

#### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>) (Note 2)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	, V <sub>out</sub> Input or Output Voltage Range –0.5 to V <sub>DD</sub> + 0.5 (DC or Transient)		V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current ±10 (DC or Transient) per Pin		mA
PD	Power Dissipation, per Package (Note 3)	500	mW
T <sub>A</sub>	Ambient Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.

3. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$ 

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



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		DIAGRAMS
	PDIP-16 P SUFFIX CASE 648	16 MC1455xBCP O AWLYYWW 111111111111111111111111111111111
A DE BERRE	SOIC-16 D SUFFIX CASE 751B	16 1455xB AWLYWW 1 1
Provident.	SOEIAJ–16 F SUFFIX CASE 966	16 MC1455xB o ALYW 1
x A WL, L YY, Y	= Specific D = Assembly = Wafer Lot = Year	

WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14555BCP	PDIP-16	2000/Box
MC14555BD	SOIC-16	48/Rail
MC14555BDR2	SOIC-16	2500/Tape & Reel
MC14555BF	SOEIAJ-16	See Note 1
MC14555BFEL	SOEIAJ-16	See Note 1
MC14556BCP	PDIP-16	2000/Box
MC14556BD	SOIC-16	48/Rail
MC14556BDR2	SOIC-16	2500/Tape & Reel
MC14556BF	SOEIAJ-16	See Note 1

 For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

### **PIN ASSIGNMENTS**

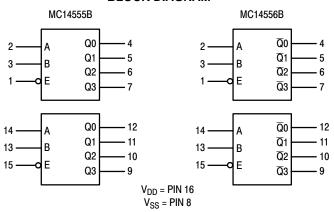
MC14555B							
ĒA	1●	16	] V <sub>DD</sub>				
A <sub>A</sub> [	2	15	] E <sub>B</sub>				
B <sub>A</sub> [	3	14	] A <sub>B</sub>				
Q0 <sub>A</sub> [	4	13	] B <sub>B</sub>				
Q1 <sub>A</sub> [	5	12	] Q0 <sub>B</sub>				
Q2 <sub>A</sub> [	6	11	] Q1 <sub>B</sub>				
Q3 <sub>A</sub> [ V <sub>SS</sub> [	7	10	] Q2 <sub>B</sub>				
v <sub>ss</sub> [	8	9	] Q3 <sub>B</sub>				

MC14556B							
1●	16	] V <sub>DD</sub>					
2	15	] Ē <sub>B</sub>					
3	14	A <sub>B</sub>					
4	13	] B <sub>B</sub>					
5	12	] <u>Q</u> 0 <sub>B</sub>					
6	11	] Q1 <sub>B</sub>					
7	10	]					
8	9	]					
	1 ● 2 3 4 5 6 7	1 ●     16       2     15       3     14       4     13       5     12       6     11       7     10					

### TRUTH TABLE

	Inputs				Outputs						
Е	nable	Select		MC14555B			Ν	/IC14	556	в	
	Ē	в	Α	Q3	Q2	Q1	QO	Q3	Q2	Q1	<u>Q</u> 0
	0	0	0	0	0	0	1	1	1	1	0
	0	0	1	0	0	1	0	1	1	0	1
	0	1	0	0	1	0	0	1	0	1	1
	0	1	1	1	0	0	0	0	1	1	1
	1	Х	Х	0	0	0	0	1	1	1	1

X = Don't Care



#### **BLOCK DIAGRAM**

ELECTRICAL CHARACTERISTICS	<b>S</b> (Voltages Referenced to V <sub>SS</sub> )
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			V <sub>DD</sub>	- 5	5°C	25°C			125°C		
Characteristic		Symbol	Vdc	Min	Max	Min	Typ <sup>(4)</sup>	Max	Min	Max	Unit
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	"1" Level	V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	"0" Level	VIL	5.0 10 15	_ _ _	1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
$\begin{array}{l} (V_{O} = 0.5 \text{ or } 4.5 \text{ Vdc}) \\ (V_{O} = 1.0 \text{ or } 9.0 \text{ Vdc}) \\ (V_{O} = 1.5 \text{ or } 13.5 \text{ Vdc}) \end{array}$	"1" Level	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
$\begin{array}{l} \text{Output Drive Current} \\ (V_{OH} = 2.5 \ \text{Vdc}) \\ (V_{OH} = 4.6 \ \text{Vdc}) \\ (V_{OH} = 9.5 \ \text{Vdc}) \\ (V_{OH} = 13.5 \ \text{Vdc}) \end{array}$	Source	I <sub>OH</sub>	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	- - -	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - -	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current		l <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)		C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I <sub>DD</sub>	5.0 10 15	_ _ _	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	μAdc
Total Supply Current <sup>(5)</sup> <sup>(6)</sup> (Dynamic plus Quiesce Per Package) (C <sub>L</sub> = 50 pF on all outp buffers switching)	ent,	ΙŢ	5.0 10 15			I <sub>T</sub> = (1	.85 μA/kHz) .70 μA/kHz) .60 μA/kHz)	f + I <sub>DD</sub>			μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
The formulas given are for the typical characteristics only at 25°C.
To calculate total supply current at loads other than 50 pF:

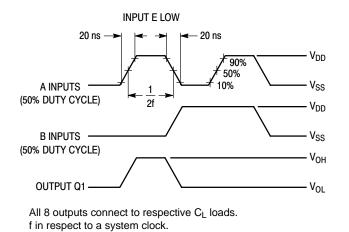
 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$ 

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF, V = ( $V_{DD} - V_{SS}$ ) in volts, f in kHz is input frequency, and k = 0.002.

### SWITCHING CHARACTERISTICS (7) ( $C_L = 50 \text{ pF}, T_A = 25^{\circ}C$ )

Characteristic	Symbol	V <sub>DD</sub>	Min	Тур <sup>(8)</sup>	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15		100 50 40	200 100 80	ns
Propagation Delay Time – A, B to Output $t_{PLH}$ , $t_{PHL}$ = (1.7 ns/pF) C <sub>L</sub> + 135 ns $t_{PLH}$ , $t_{PHL}$ = (0.66 ns/pF) C <sub>L</sub> + 62 ns $t_{PLH}$ , $t_{PHL}$ = (0.5 ns/pF) C <sub>L</sub> + 45 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	220 95 70	440 190 140	ns
Propagation Delay Time – E to Output $t_{PLH}$ , $t_{PHL}$ = (1.7 ns/pF) C <sub>L</sub> + 115 ns $t_{PLH}$ , $t_{PHL}$ = (0.66 ns/pF) C <sub>L</sub> + 52 ns $t_{PLH}$ , $t_{PHL}$ = (0.5 ns/pF) C <sub>L</sub> + 40 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	- - -	200 85 65	400 170 130	ns

The formulas given are for the typical characteristics only at 25°C.
Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

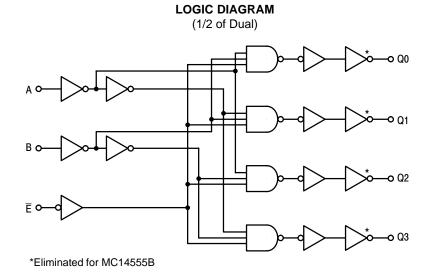


20 ns -— 20 ns  $V_{DD}$ 90% INPUT B 50% 10% VSS t<sub>PLH</sub> t<sub>PHL</sub> V<sub>OH</sub> 90% OUTPUT Q3 50% MC14556B 10%  $V_{OL}$ t<sub>THL</sub> - t<sub>TLH</sub> <sup>t</sup>PHL V<sub>OH</sub> t<sub>PLH</sub> 90% OUTPUT Q3 50% MC14555B 10% V<sub>OL</sub> t<sub>TLH</sub> t<sub>THL</sub>

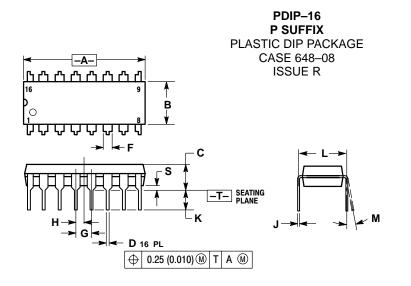
INPUT A HIGH, INPUT E LOW

Figure 1. Dynamic Power Dissipation Signal Waveforms

Figure 2. Dynamic Signal Waveforms



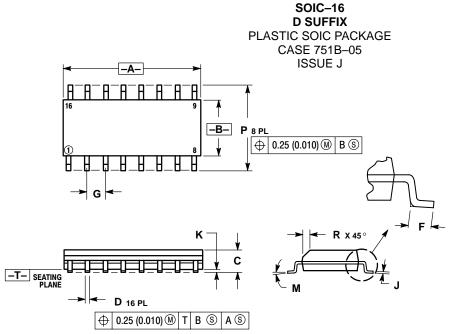
### PACKAGE DIMENSIONS



NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH. 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.145 0.175		4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27 BSC	
J	0.008	0.015	0.21	0.38
Κ	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
М	0°	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

### PACKAGE DIMENSIONS

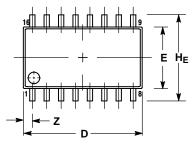


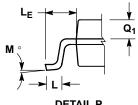
NOTES:
DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETER.
DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
Μ	0 °	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

### PACKAGE DIMENSIONS

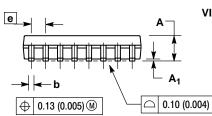
SOEIAJ-16 **F SUFFIX** PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O

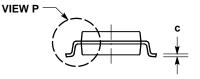




DETAIL P

A





NOTES:

DIMENSIONING AND TOLERANCING PER ANSI 1.

EDIMENSIONING AND TOLENAVING FEITAND
Y14.5M, 1982.
CONTROLLING DIMENSION: MILLIMETER.
DIMENSIONS DAND E DO NOT INCLUDE
MOLD FLASH OR PROTRUSIONS AND ARE
MEASURED AT THE PARTING LINE. MOLD FLASH
OR PROTRUSIONS SHALL NOT EXCEED 0.15
(2020 PER OUP

OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY. 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018). TO BE 0.46 ( 0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
e	1.27	BSC	0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
Μ	0 °	10 °	0 °	10 °
Q1	0.70	0.90	0.028	0.035
Ζ		0.78		0.031

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