One-Horsepower Off-Line Brushless Permanent Magnet Motor Drive

Ken Berringer
Semiconductor Products Sector
Discrete Applications Laboratory

INTRODUCTION

Brushless Permanent Magnet (BPM) motors, also known as brushless DC motors, using MOSFET inverters are fairly common in low voltage variable speed applications, such as disk drives. Higher voltage off-line applications can also utilize the same MOSFET driven BPM motor technology. High voltage MOSFETs have been available for some time. The real problem has been designing a reliable, low cost high side driver and understanding the more subtle effects of diode snap and PCB layout. Low cost linear control ICs such as the MC33035 can provide cost effective variable speed control. This application note will present the design of a one-horsepower off-line BPM motor drive board using opto-isolators and a special MOSFET turn-off IC for level translation. Switching time selection, PWM losses, effects of diode reverse recovery, effects of MOSFET parasitics and layout guidelines are also discussed.

BRUSHLESS PERMANENT MAGNET MOTORS

Brushless permanent magnet motors share the torque speed characteristics and basic operating principles of a brushed DC motor. A BPM motor is constructed like a brushed DC motor turned inside out. The permanent magnets are on the rotor and the field windings are on the stator. The task of commutation is then performed by electronic control using hall effect sensors to determine the rotor position. Rotor speed can then be varied by changing the effective DC link voltage through Pulse Width Modulation (PWM). This simple variable speed control strategy is easily achieved using low cost electronics.

TMOS™ power MOSFETs are an ideal switch for BPM motor speed control. Power MOSFETs are capable of switching at very high frequencies. Conduction losses due to the MOSFET's on resistance $R_{DS(on)}$ are very low for low voltage devices and reasonable for devices up to about 500 volts. Power MOSFETs have a built-in diode which can be used as a free wheeling diode. Recent improvements in MOSFET ruggedness allow the diode to withstand the high stresses imposed by forced commutation. Energy rated E-FETs™ are rated to withstand high di/dt stresses during forced commutation, and are capable of dissipating quite a bit of energy in avalanche during Unclamped Inductive Switching (UIS).

Much has been written about the apparent problems associated with MOSFET diode reverse recovery. Many engineers think these diodes are much too "slow" to be used in 20 kHz PWM applications. This is often not true. The reverse recovery times associated with a power MOSFET are comparable to a discrete fast rectifier. While ultrafast rectifiers and fast recovery MOSFETs (irradiated or heavy metal doped) have much shorter measured reverse recovery times, the abrupt recovery of these devices makes them difficult to use in practical circuitry.

FORCED DIODE REVERSE RECOVERY EFFECTS

The most important consideration in PWM controlled circuit operation and efficiency is diode reverse recovery. Unfortunately, the reverse recovery characteristics of power MOSFETs are frequently misunderstood. The conventional measurement of reverse recovery time, t_{rr}, does not fully explain all of the important device recovery characteristics.

A typical reverse recovery waveform is shown in Figure 1. The reverse recovery time t_{rr} has been traditionally defined as the time from diode current zero crossing to where the current

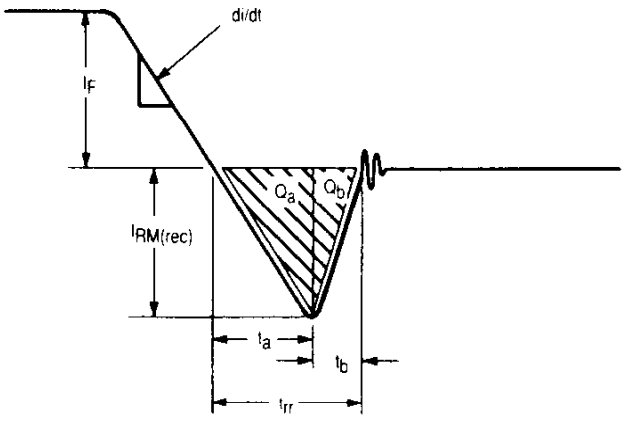

Figure 1. Reverse Recovery Waveform

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returns to within 10% of the peak reverse recovery current $I_{RM(rec)}$. This does not give enough information to fully characterize the waveform shape. A better way to characterize the rectifier reverse recovery is to partition the reverse recovery time into two different regions t_a and t_b, as shown in Figure 1. The t_a time is a function of the forward current and the applied di/dt. A charge can be assigned to this region denoted Q_a, the area under the curve. The t_b portion of the reverse recovery waveform is not very well understood. Measured t_b times vary greatly with the switch characteristics, circuit parasitics, load inductance and the applied reverse voltage. A relative softness can be defined as the ratio of t_b to t_a. General purpose rectifiers are very soft (softness factor of about 1.0), fast rectifiers are fairly soft (softness factor of about 0.5) and ultrafast rectifiers are very abrupt (softness factor of less than 0.2).

Due to the effect of circuit wiring inductances, real circuitry can only withstand a certain level of di/dt. Ultrafast rectifiers and fast recovery MOSFETs exhibit very snappy recovery characteristics. This means that the turn-on di/dt must be decreased in order to maintain acceptable performance. Therefore, PWM losses will increase as an indirect result of using abrupt recovery devices, when compared to soft devices with the same amount of stored charge. Power MOSFETs usually have about the same amount of stored charge as a fast rectifier, however they are more abrupt. Adding a soft rectifier in parallel with the MOSFET which is being PWM against, may reduce abruptness of the power MOSFET, allowing higher di/dts and consequently lower PWM losses, especially for the 500 volt devices.

PWM SWITCHING SPEEDS

A continuous-mode clamped inductive switching turn-on waveform is shown in Figure 2. Note that the current waveform is actually the diode reverse recovery waveform turned upside down. The drain voltage does not fall until after the current has reached its peak, except for a small dip resulting from the wiring inductance. The turn-on di/dt is controlled by the power MOSFET and gate resistor. During MOSFET turn-on the gate resistor R_G and input capacitance C_{iss} form an RC time constant. This means that the gate-to-source voltage will increase by Equation 1. As a convention, in all of the following equations capacitance is in Farads and inductance is in Henries.

$$V_{GS} = V_{CC}\left[1 - e^{(-t/R_G C_{iss})}\right] \quad (1)$$

Note that the drain-to-gate capacitance does not affect turn-on, since the voltage from drain-to-source has not yet changed significantly. Differentiating the first equation and using the definition of transconductance g_{FS} gives di/dt vs time, Equation 2.

$$\frac{dI_D}{dt} = V_{CC}\,\frac{g_{FS}}{R_G C_{iss}}\,e^{(-t/R_G C_{iss})} \quad (2)$$

Thus, di/dt is also varying over time. Actually, g_{FS} also varies directly with the gate voltage, however the typical g_{FS} specified at 1/2 rated current can be used for most approximations. These equations give the di/dt in units of amps per second, however di/dt is usually expressed as A/µs(10^6A/s), similarly dv/dt is usually expressed as V/µs(10^6V/s).

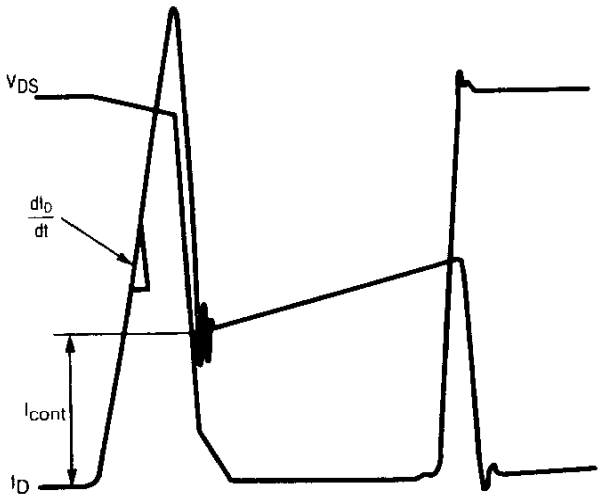

Figure 2. Continuous Mode Clamped Inductive Switching Voltage and Current Waveforms

Since the plateau voltage $V_{GS(plat)}$, corresponding with the flat part of the gate charge curve, does not vary greatly with current, we can use an approximation of the plateau voltage, normally 6 to 8 volts, to find the turn-on time and turn-on di/dt. Equations 1 and 2 can then be solved for the turn-on time and turn-on di/dt, Equations 3 and 4.

$$t_{on} \approx R_G C_{iss} ln\left(\frac{V_{CC}}{V_{CC} - V_{GS(plat)}}\right) \quad (3)$$

$$\frac{dI_D}{dt} \approx \frac{g_{FS}}{R_G C_{iss}}\,(V_{CC} - V_{GS(plat)}) \quad (4)$$

Up to now we have ignored the source inductance. The source inductance develops a voltage equal to L_S dI_D/dt, which subtracts from the true gate-to-source voltage and slows switching. Equation 5 includes the effect of the source inductance.

$$\frac{dI_D}{dt} \approx \frac{(V_{CC} - V_{GS(plat)})}{\frac{R_G C_{iss}}{g_{FS}} + L_S} \quad (5)$$

The effect of the source inductance is quite significant. This inductance has the effect of limiting and linearizing the dI_D/dt. Note that for very small values of resistance, the source inductance actually controls the di/dt. The source inductance used in this equation should include the wirebond inductance, all PCB trace inductances, sense resistor inductance and any other stray inductance up to where the gate drive ground path meets the motor current path. Typical MOSFET L_S specifications are 5 to 15 nH, while the typical total wiring circuit inductance may be 20 to 100 nH.

The maximum di/dt must be below the Commutating Safe Operating Area (CSOA) limit of the power MOSFET This means that you must use an energy rated device. The CSOA limit for most E-FETS is usually above practical di/dt

values for these types of circuits, depending on the particular device. Common practice is to limit the peak current to the pulsed current rating of the device. This would limit the maximum di/dt to the following value.

$$\left(\frac{dI_D}{dt}\right)_{max} = \frac{(I_{DM} - I_{cont})^2}{2\,Q_a} \qquad (6)$$

The pulsed current rating of a power MOSFET is usually based on a 10 μsec pulse, depending on the safe operating area curve. Since peak reverse recovery currents last less that a micro-second, this specification does not usually apply. Actually, most MOSFETs do not have enough gain to conduct their I_{DM} limit only 10 volts on the gate. This is not a problem, since the device is already in the saturation region, it is not critical if the MOSFET has enough gain. The energy absorbed by the MOSFET is actually lower at high di/dts, which will be shown later.

A practical suggestion for an initial design is to choose a fairly low di/dt of 25 to 100 A/μs, then find a suitable resistor using Equation 5. After the drive is working the resistor value may be decreased until noise becomes a problem or the MOSFET approaches it's CSOA limit.

PWM LOSSES

Diode clearing or PWM losses can be approximated by integration of the voltage and current waveforms during continuous mode inductive switching turn-on. The energy lost during turn-on is related to the turn-on time recovery time and stored charge as follows:

$$E_{on} \approx \left[\frac{1}{2}(V_{buss}I_{cont}t_{on}) + (V_{buss}I_{cont}t_a) + (V_{buss}Q_a) + \frac{1}{4}(V_{buss}Q_b)\right] \qquad (7)$$

Where V_{buss} is the buss or rail voltage, I_{cont} is the continuous current through the load, and t_{on} is the MOSFET turn-on time. A better understanding of these losses can be achieved by expressing energy losses in terms of turn-on di/dt and the diode stored charge only. Diode t_a, Q_a, and di/dt are related by the following equation.

$$t_a = \sqrt{\frac{2Q_a}{\frac{dI_D}{dt}}} \qquad (8)$$

Using this equation and the approximation of a constant di/dt with Equation 7 yields the following equation for turn on losses.

$$E_{on} \approx \frac{1}{2}\left(\frac{I^2_{cont}}{\frac{dI_D}{dt}}\right) + \frac{I_{cont}\sqrt{2Q_a}}{\sqrt{\frac{dI_D}{dt}}} + Q_a + \frac{1}{4}Q_b\,V_{buss} \qquad (9)$$

Equation 9 shows that in order to minimize PWM losses, the stored charge should be minimized and the turn-on di/dt should be as high as possible. Also, the power dissipated during the t_b time is a small fraction of the PWM losses. Therefore, we should gladly sacrifice t_b time for an increase in di/dt.

For purposes of calculating PWM losses, the stored charge for a Power MOSFET can be approximated by ignoring the t_b portion of the wave form and assuming:

$$Q_a \approx \frac{t^2_{rr}\left(\frac{dI_D}{dt}\right)_{tested}}{2} \qquad (10)$$

EFFECT OF MOSFET PARASITICS

A detailed drawing of a power MOSFET showing the parasitic components is shown in Figure 3. During diode snap the source inductance and drain-to-gate capacitance have large effects on the switching current and voltage waveforms, these effects are not easily understood.

As we have already seen, the source inductance effects the turn-on performance of the power MOSFET. During the t_b portion of the inductive load turn-on waveform, the current decreases rapidly causing a very high negative di/dt. This creates a negative voltage across the source inductance L_S. The voltage across the source inductance can be approximated by assuming a constant di/dt.

$$V_{S'S} \approx -L_S\frac{I_{RM(rec)}}{t_b} \qquad (11)$$

The actual source metal on the die itself, S' is pulled down by the source inductance, which cause the gate voltage to be pulled down through the gate-to-source capacitor. This appears in the apparent gate-to-source voltage as a downward spike during the t_b time. This additional voltage also appears across the series gate resistor, increasing the gate current and decreasing voltage fall time. Under high di/dts, greater than about 200 A/μs, the gate voltage may be pulled negative. This is especially true for higher current MOSFETs and IGBTs.

During this same time, t_b, the rapidly falling drain voltage couples through the drain-to-gate capacitor, pulling current out of the gate, and starving the MOSFET of gate charge. The

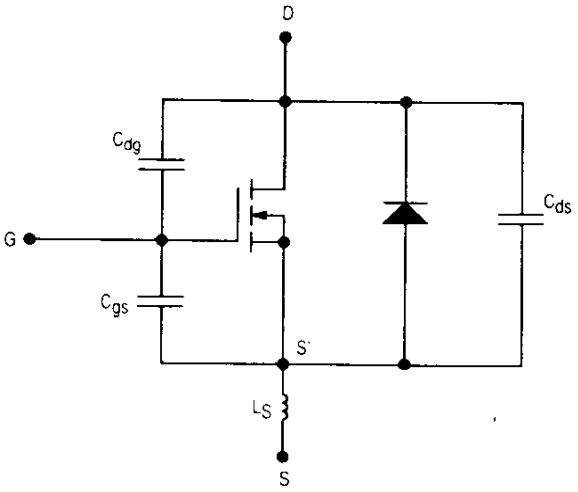

Figure 3. Power MOSFET Parasitic Components

current pulled out of the gate is determined by the Equation 12.

$$I_{G2} = -C_{dg}\frac{dV_{DS}}{dt} \quad (12)$$

Thus, high dv/dts can actually turn-off the MOSFET through the gate-to-drain capacitor. This is especially true for high voltage MOSFETs and IGBTs. The combination of the two effects, resulting from the source inductance and the gate-to-drain capacitance, can cause very high frequency oscillations well over 100 MHz. These oscillations can result in excessive electromagnetic interference or even destroy the devices due to excessive gate voltages or di/dt stresses. The oscillations can be minimized by limiting the turn-on di/dt, using a careful layout and using soft rectifiers.

The drain-to-gate capacitor also has a very significant effect on the MOSFET which is undergoing forced reverse recovery. When a MOSFETs intrinsic diode is being cleared, we would like the MOSFET to remain completely off. Unfortunately, the dv/dt which appears across drain-to-source during the t_b portion of reverse recovery waveform creates a positive current into the gate resistor of the MOSFET. The gate resistor then develops a positive voltage from gate-to-source, which will turn the device on and allow current flow. In practice this current appears to make the reverse recovery current larger and the recovery time longer than expected. This current can be distinguished from reverse recovery current in that it is also present during discontinuous operation.

LAYOUT GUIDELINES

There are three important rules to remember when laying out a PWM motor drive board.

1. Minimize the "uncoupled" half-bridge loop inductance.

2. Keep the motor currents out of the gate drive path, whenever possible.

3. Use back-to-back zener diodes directly across the gate-to-source of each power MOSFET to clamp the gate voltage.

The first rule dictates that the output transistors should be configured with the top and bottom transistors of each phase as close as physically possible. A high frequency decoupling capacitor should be placed across each half-bridge, again as close as physically possible, to decouple the additional inductance in the PCB traces and sense resistor. A low equivalent series inductance (ESL) metalized polypropylene or metalized polyester capacitor should be used to supply the high di/dts needed for inductive switching. Be very careful in adding capacitance to an existing circuit, as di/dts will increase and may exceed device limitations. The combination of an energy rated device, appropriate gate resistor and low loop inductance will allow predictable high-speed switching.

The second rule means that the gate drive should be grounded directly on the source of the power MOSFET. On larger power modules, such as the Energy Management Se-

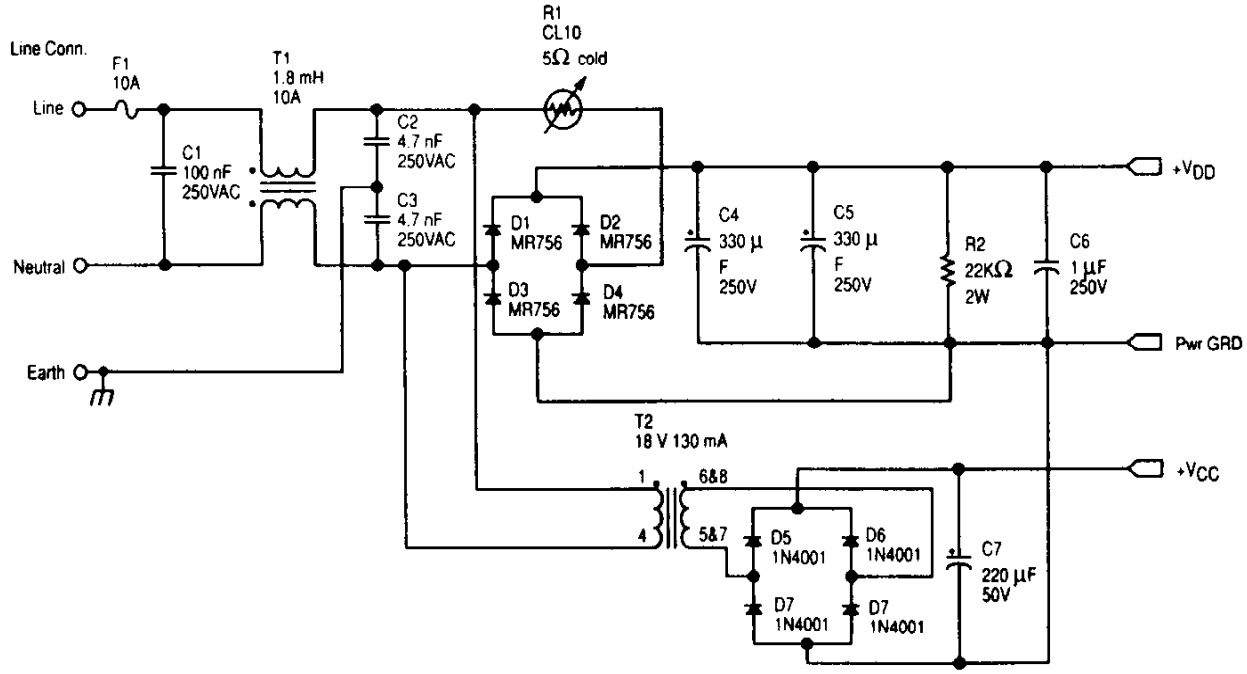

Figure 4a. Front End Section

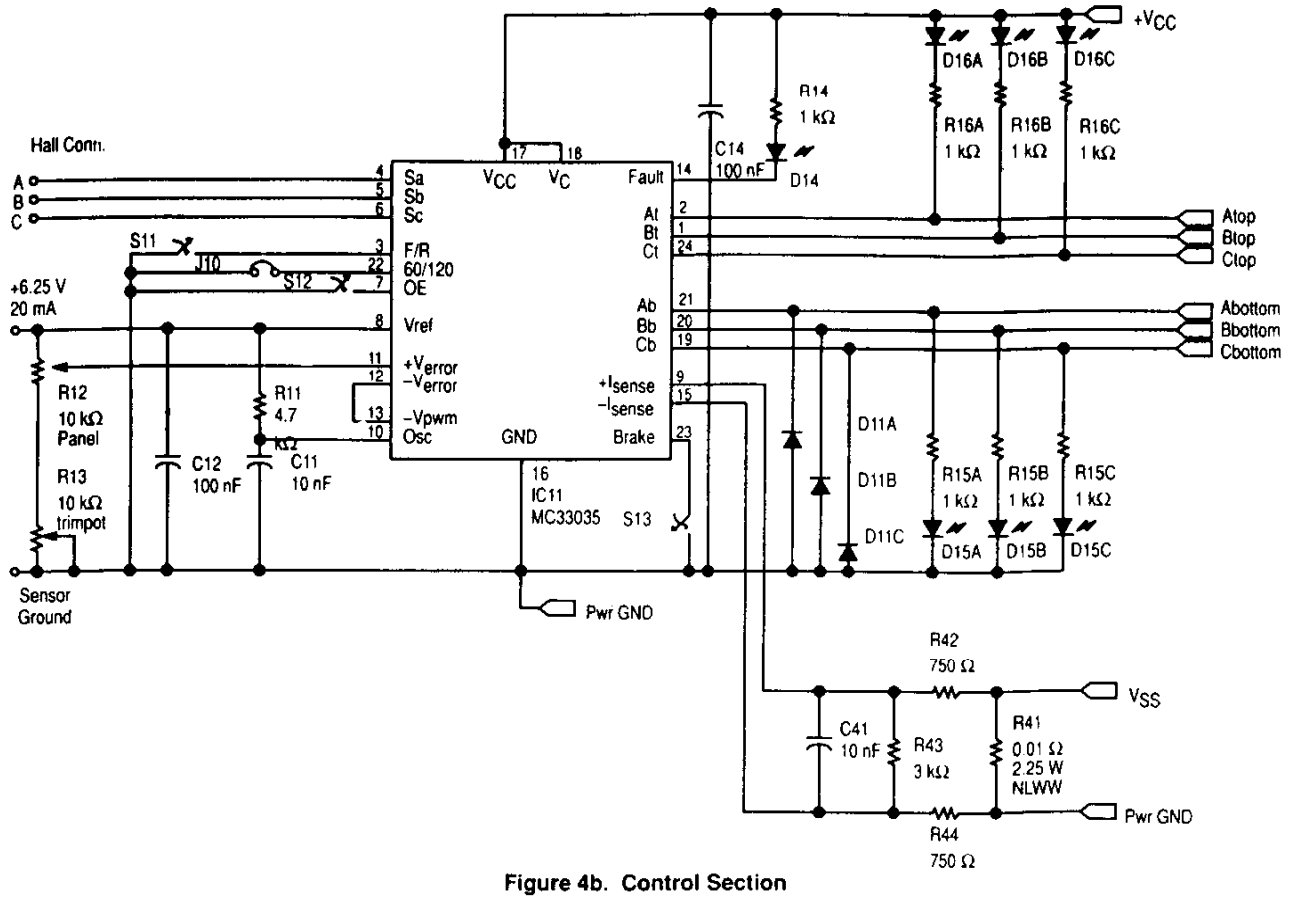

Figure 4b. Control Section

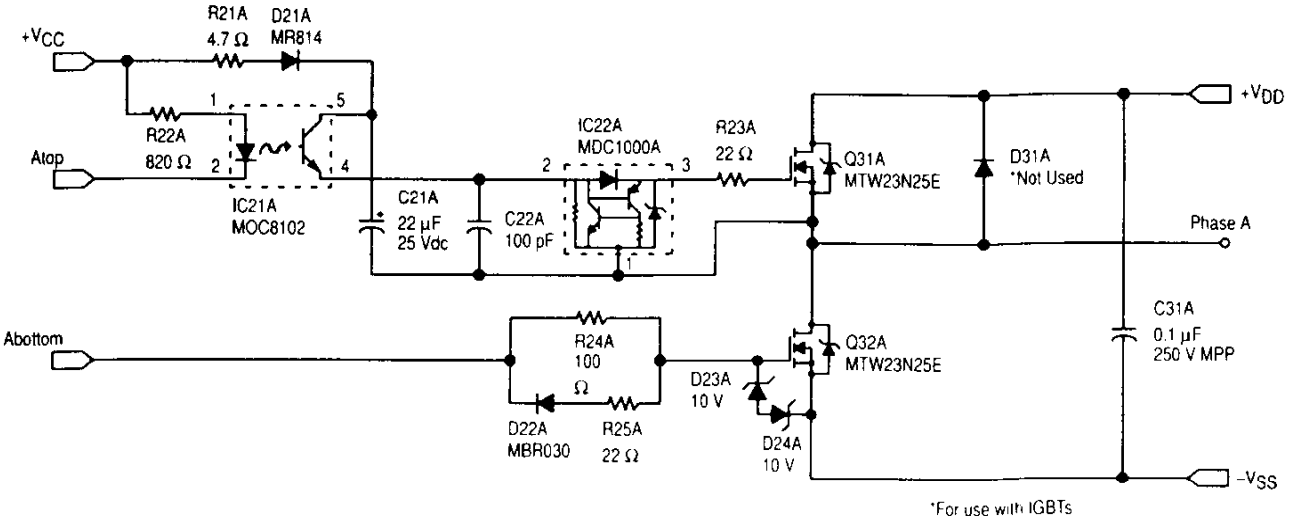

Figure 4c. Phase A Output Stage
(Phases B and C are Indentical)

ries power modules, a separate source Kelvin terminal is brought out to minimize the package inductance. Using three terminal devices on a PCB, the best you can do is to ground the gate drive on the source pad of the power MOSFET. This is important on both the high side drive and the lower side. When using a common IC to drive all three bottom devices, it is not possible to ground a single IC in three separate places. In this case, you should ground the driver IC to a high frequency decoupling capacitor where the sources for all three phases meet. Some linear ICs, such as the MC33034, bring out a separate gate drive return which is common to all three phases. This allows the sense resistor inductance to be eliminated for better turn-on characteristics. However, a clamp diode should be used so that the gate drive return cannot be pulled down below the IC ground.

A zener clamp is necessary to limit the gate voltage and protect the device. Back-to-back zeners are suggested because it is never possible to totally eliminate all of the source inductance. The effect of the source inductance has been discussed previously. During diode snap, a single zener may forward bias and cause oscillations or hyper-abrupt recovery. These zener diodes should be placed close to the power MOSFETs. Perhaps more importantly, a Kelvin source terminal or a separate track to the source pad should be used to connect the clamp directly from gate-to-source. This will eliminate any circuit related inductance in the source path and effectively protect the MOSFET from excessive gate voltages. Low speed switching with well controlled di/dts may not require back-to-back zeners. However, be very cautious when using a single zener. Note that 200 A/μs during the loosely controlled t_b period will develop 10 volts across 50 nH, enough to exceed the plateau voltage and forward bias a single zener diode.

OPTO-ISOLATED DRIVE CIRCUIT

The full schematic of the off-line BPM motor drive is shown in Figures 4a through 4c and a photograph of the BPM motor drive board is shown in Figure 5. The design of a BPM motor drive should start at the output stage and work backwards to the control, power supply and front end sections.

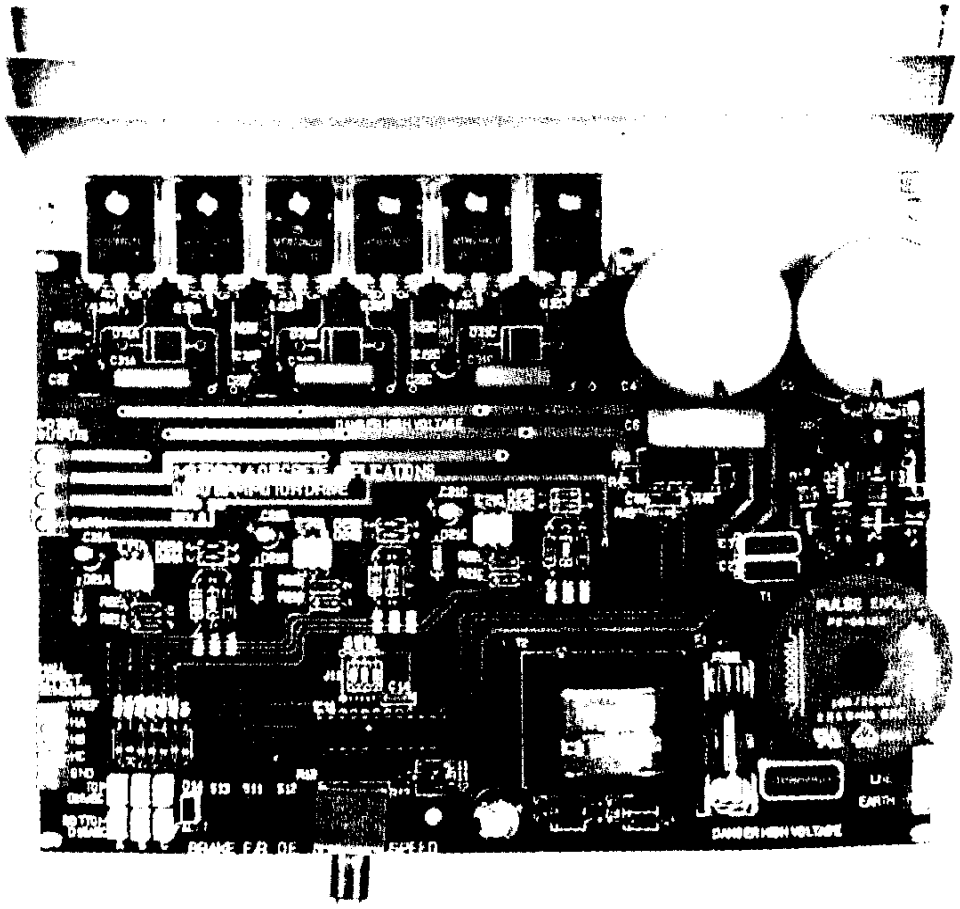

Figure 5. Brushless DC Motor Drive Circuit Board

The MOSFETs chosen for this BPM motor drive are the MTW23N25E, a 23 Amp, 250 Volt devices in a TO-247 package. Off-line applications that run directly off a rectified 115 VAC line require at least 250 volt MOSFETs. The nominal rectified DC voltage for a 115 VAC application is 163 volts. A 20% high-line condition will give a maximum DC link voltage of 195, giving 200 volt FETs no headroom for voltage transients. These voltage transients are present during turn-off for any clamped inductive load. The MOSFET must be sized for conduction, switching, and diode clearing losses. These devices are sufficient for motors up to 1 hp.

The high side drive circuit is greatly simplified by using two special devices, a new-generation opto-isolator, MOC8102, and a new device specifically designed for MOSFET gate turn-off, the MDC1000A. Level translation is performed by an opto-isolator. The MOC8102 opto-isolator features a tightly controlled current transfer ratio and a new super stable LED which effectively eliminates the problem of degradation of power output over time.

Boost voltage for the top gate drive is provided by a conventional bootstrap circuit. When the top MOSFET is off and it's source is pulled down close to ground by the bottom device, the bootstrap capacitor charges through the bootstrap diode and a current limiting resistor. When this transistor is turned back on current is supplied by the bootstrap capacitor. The value of the bootstrap capacitor is chosen to provide sufficient charge for the lowest desired motor speed.

The resistor in series with the opto-isolator's LED sets the current to about 20 mA. When the LED is turned on, about 20 mA of current flows through the opto-transistor and turns on the top MOSFET through the MDC1000A MOS Turn-Off device (MTO) and the series gate resistor. The Opto's LED series resistor therefore indirectly determines the top side turn-on time.

The MDC1000A provides a zener clamp and turn-off current to the power MOSFET. When driven by a current source, the internal diode conducts freely to turn-on the MOSFET. The zener diode clamps the gate-to-source voltage to about 10 volts. When the current source is turned off, an SCR fires and pulls the MOSFET's gate down to it's source. The series gate resistor determines the turn-off time and dissipates most of the energy stored in the MOSFET's gate, off-loading power from the MDC1000A. This resistor is chosen as low as possible, to minimize the possibility of turn-on due to the dv/dt impressed across device which couples through the drain-to-gate capacitor.

The lower side power MOSFET is driven directly by the controller IC. An additional diode and resistor provides faster turn-off times while the larger gate resistor sets the turn-on time and turn-on di/dt. These resistors are minimum practical values for very fast switching and low power losses. Electromagnetic interference may require the use of slower switching. An oscilloscope plot of continuous mode clamped inductive switching using these MOSFETs with the selected resistor values is shown in Figure 6. The peak drain current is almost 40 amps and the total reverse recovery time is about 300 ns with 10 amps of continuous current.

The MC33035 brushless DC motor controller provides all the necessary functions to complete an open loop system: Hall effect decoding, PWM control, high-current lower side gate drive, and fault detection. This is a very versatile IC which can be used with 60° and 120° BPM motors and brush DC motors as well. A slightly lower cost 20 pin version, the MC33033, is also available which does not have the brake input, non-inverting current sense error amplifier input, fault output, and separate output drive VC supply pin. The MC33039 closed-loop brushless motor adapter IC can be added to either the MC33033, MC33034, or the MC33035 to form a complete closed loop system.

A low inductance sense resistor provides over current and short circuit detection. A resistive divider network sets the current limit at about 15 amps and also provides a differential mode low pass filter with the 10 nF capacitor. This voltage is then fed into the MC33035's current sense amplifier. A 10 µs time constant in conjunction with the 10 volt gate clamp zeners on all six devices provides adequate protection against excessive stall currents and most line-to-line faults. A good low noise layout is absolutely essential in order to get the over-current detection circuitry to function properly. Dynamometer testing indicates the over current comparator trips at about 1 1/2 HP. The power MOSFETs also survived a dead short across two phases during start-up and repetitive shorts with a screwdriver across two phases while running.

The MC33035 provides a fault output but does not latch off. In order to fully protect the drive, a latch and reset circuit can be added. The under-voltage lockout provides adequate low line protection, however this drive does not have any over-voltage protection. A thermal overload for both the power MOSFETs and the motor would complete a reliable fault tolerant system.

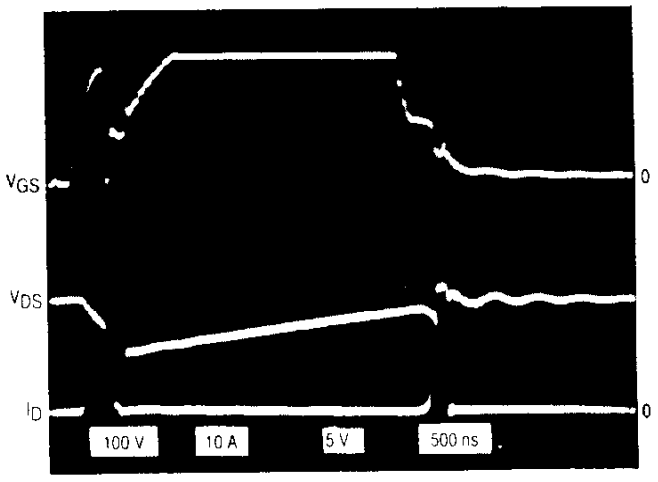

Figure 6. Voltage and Current Waveforms of Brushless DC Motor Drive

CONCLUSIONS

Brushless Permanent Magnet motors and power MOSFETs can provide useful Variable Speed Drives (VSDs) for 110 VAC and 230 VAC applications up to about 1 HP. This encompasses the majority of the consumer, and commercial variable speed motors. An understanding of the problems associated with all PWM circuitry, diode reverse recovery characteristics and MOSFET parasitics is necessary in order to design such a BPM motor drive.

Emerging fast IGBT technology may provide cost effective BPM motor and AC induction motor drives for motors operating off 230 VAC for the 1 to 5 HP level. However, power MOSFETs and MOSFET/IGBT combinations should continue to prevail in the fractional horsepower motors, especially 110 VAC applications. Developments in drive circuitry can further improve the cost, performance, and reliability of VSDs, while future developments in MOS and rectifier technology may greatly improve noise performance and efficiency.

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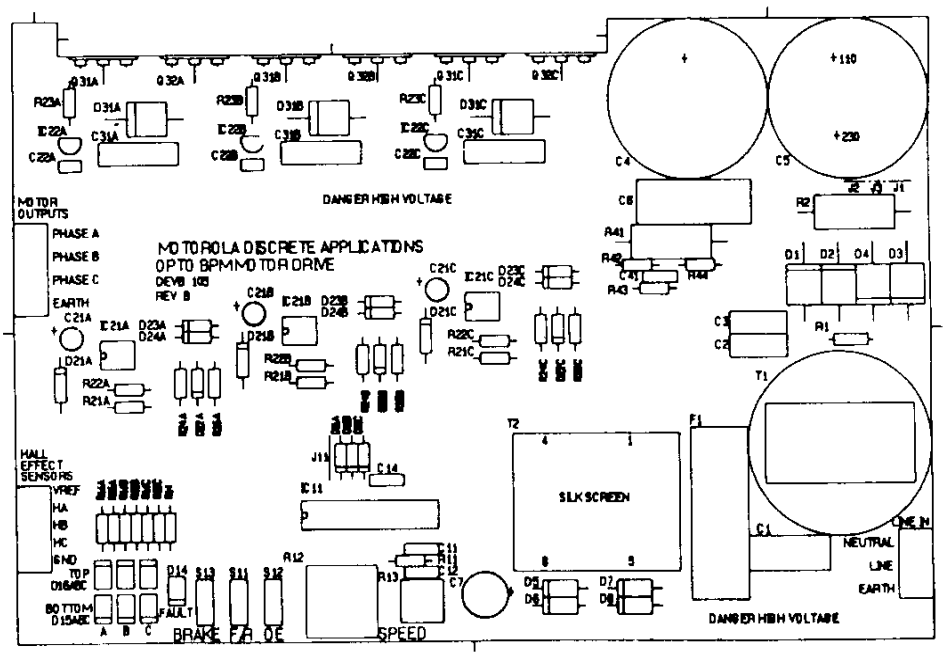

Figure 7. Silkscreen Layer (not full size)

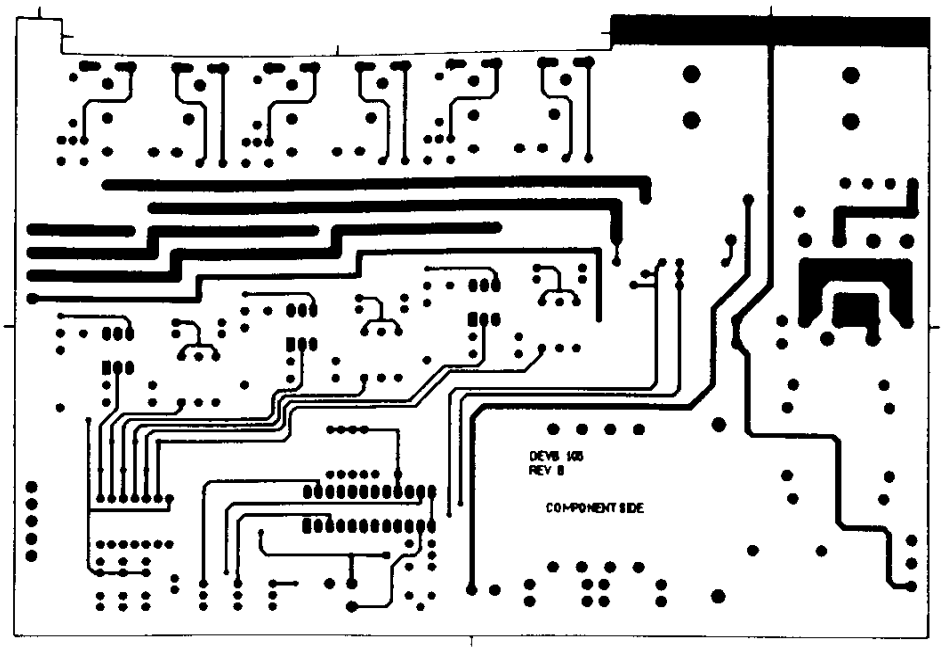

Figure 8. Component Side (not full size)

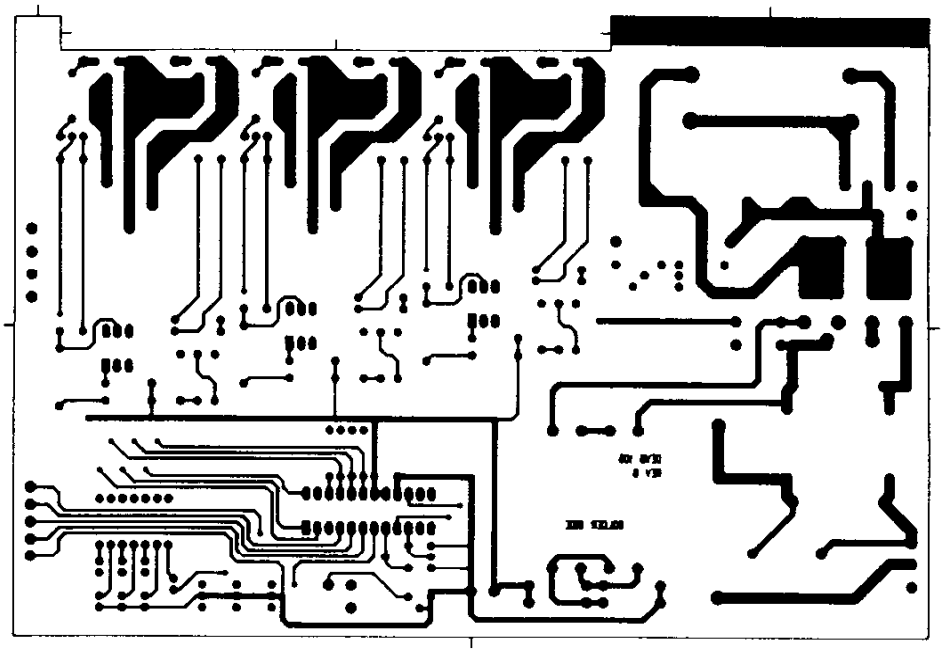

Figure 9. Solder Side (not full size)

Table 1. Parts List By Component Values and Part Numbers

Designators	Quantity	Description	Rating	Tolerance	Manufact.	Part Number	Comp.
C21A,C21B,C21C	3	22 µF Electrolytic Cap	25 VDC				AL
C7	1	220 µF Electrolytic Cap	50 V				AL
C4,C5	2	330 µF Electrolytic Cap	250 V		Sprague	80D	AL
C2,C3	2	4.7 nF AC Cap	250 VAC		Rifa	PME 289 MA	
C1	1	100 nF AC Cap	250 VAC		Rifa	PME 285 MB	
C31A,C31B,C31C	3	0.1 µF Capacitor	250 V	5%	Wima	MKP 10	MPP
C6	1	1 µF Capacitor	250 V	10%	Wima	MKP 4	MPP
C11,C41	2	10 nF Capacitor	50 V	10%			Ceramic
C12,C14	2	100 nF Capacitor	50 V	10%			Ceramic
C22A,C22B,C22C	3	100 pF Capacitor	50 V	10%			Ceramic
Power Line Connector	1	3 pin Connector	0.200"		Phoenix	1729131	
Motor Output	1	4 pin Connector	0.200"		Phoenix	1729144	
Hall Switch Connector	1	5 pin Connector	0.150"		Phoenix	1727049	
D5,D6,D7,D8	4	50 V Diode	1 A		Motorola	1N4001	
D1,D2,D3,D4	4	600 V Diode	6 A		Motorola	MR756	
D21A,D21B,D21C	3	600 V Diode			Motorola	MR816	
D31A,D31B,D31C	3	Diode				Not Used	
D11A,D11B,D11C,D22A,D22B,D22C	6	30 V Schottky	1/2 A		Motorola	MBR030	
F1	1	10 A Fuse					
D15A,D15B,D15C,D16A,D16B,D16C	6	Green LED			GI	MV54124A	
D14	1	Red LED			GI	MV57124A	
IC11	1	Control IC			Motorola	MC33035	
IC22A,IC22B,IC22C	3	MTO			Motorola	MDC1000A	
Q31A,Q31B,Q31C,Q32A,Q32B,Q32C	6	N-ch Power MOSFET			Motorola	MTW23N25E	
IC21A,IC21B,IC21C	3	Optocoupler			Motorola	MOC8102	
R12	1	10 kΩ Potentiometer			Bourns	81A1AB28A15	
R13	1	10 kΩ Potentiometer	trimpot		Bourns	3386P1 103	
R41	1	0.01 Ω Resistor	2.25 W	5%	Mills	MRP-2-NI	NLWW
R14,R15A,R15B,R15C,R16A,R16B,R16C	7	1 kΩ Resistor	1/4 W	5%			
R43	1	3 kΩ Resistor	1/4 W	5%			
R11	1	4.7 kΩ Resistor	1/4 W	5%			
R21A,R21B,R21C	3	4.7 Ω Resistor	1/4 W	5%			
R2	1	22 KΩ Resistor	2 W	10%			
R23A,R23B,R23C,R25A,R25B,R25C	6	22 Ω Resistor	1/4 W	5%			
R24A,R24B,R24C	3	100 Ω Resistor	1/4 W	5%			
R42,R44	2	750 Ω Resistor	1/4 W	5%			
R22A,R22B,R22C	3	820 Ω Resistor	1/4 W	5%			
S11,S12,S13	3	SPDT Switch	submin		NKK	#SS 12SDP2	
R1	1	5 Ω cold Thermistor			Keystone	CL10	
T1	1	1.8 mH Transformer	10 A		Pulse Eng.	PE-96188	
T2	1	18 V Transformer	130 mA		Stancor	SW336	
D23A,D23B,D23C,D24A,D24B,D24C	6	10 V Zener			Motorola	1N4697	