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Application Note

PARALLELING POWER MOSFETs IN SWITCHING APPLICATIONS

by Kim Gauen

This article updates and supplements the present TDT series of Motorola Applications Notes with a more detailed analysis and design guide for TMOS power MOSFET parallel applications to account for device to device parameter differences and responses.

POWER MOSFET FEATURES

The thermally-triggered adaptive responses of power MOSFETs to high current loads make the devices easy to employ in parallel applications. The designer must observe only a few pertinent design considerations for their use in static and dynamic applications switching resistive and inductive loads. In fact, in most applications, these designs do not require the use of ballasting resistors or current sensing and control loops commonly necessary for balanced current distribution in bipolars.

Static Current Sharing Design Considerations

Although increasing junction temperature raises the on-resistance and conduction losses of the power MOSFET, definite benefits are attributable to the positive temperature coefficient of $r_{DS(on)}$. If a portion of the chip begins to hog current, the localized temperature will increase, causing a corresponding increase in the $r_{DS(on)}$ of that portion of the chip, and current will shift away to the cooler, less active, portions of the die. This trait accounts for the tendency of the device to share current over the entire surface of the die's active region. Because current crowding and hotspotting are eliminated under normal operating conditions, there is no need to derate power MOSFETs to guard against secondary breakdown.

The argument supporting current sharing within a device, due to the positive temperature coefficient of $r_{DS(on)}$, is easily extended to the case of paralleled devices. As within a single device with some imbalance in $r_{DS(on)}$ over the die's active area, an imbalance or mismatch of $r_{DS(on)}$ between devices will cause an intitial current loading imbalance between devices. The resulting rise in junction temperature and on-resistance of the device with the lowest $r_{DS(on)}$ will decrease that device's drain current and will establish a more equal distribution of the total load current in all paralleled devices.

While this tendency is definitely observable, its influence on the degree of current sharing is often overestimated. In the power MOSFET, the current sharing mechanism is not triggered simply by high junction temperature, but by the difference in T_J between the low and high $r_{DS(on)}$ devices. Due to the generally small thermal coefficient of $r_{DS(on)}$, this difference in junction temperature sometimes must be substantial to attain a high degree of current sharing.

Since the ultimate concern is for optimum reliability, the emphasis should not be placed on obtaining large deltas in T_J to force a greater degree of current sharing. On the contrary, the effort should be focused on decreasing the T_J of the hottest device. This is accomplished by close thermal coupling of the paralleled devices, provided that the total heatsinking capability is not compromised by doing so. This will tend to minimize the differences in both case and junction temperature. Before a worst case example of these concepts can be examined, some knowledge of the range of the variation of $r_{DS(on)}$ within production devices must be obtained.

TABLE 1
Variation of $r_{DS(on)}$, g_{fs}, and $V_{GS(TH)}$ in Two Wafer Lots of the MTP8N18

	$r_{DS(on)}$		g_{fs}		$V_{GS(TH)}$		Sample Size
	Min.	Max.	Min.	Max.	Min.	Max.	
Wafer Lot I	0.231	0.297	3.704	4.878	2.300	4.080	100
Wafer Lot I	0.239	0.305	3.571	4.878	3.685	3.910	50

* Maximum Rated $r_{DS(on)}$ is 0.4 ohms.

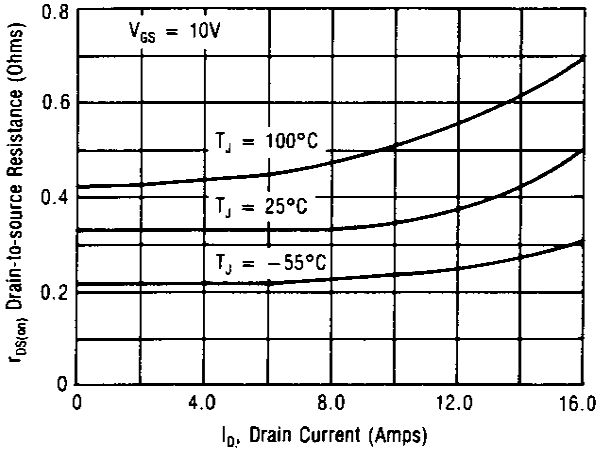

FIGURE 1 — On-Resistance vs Drain Current — MTP8N18

Unless devices are matched for identical on-resistances, there will be at least a slight mismatch in their individual drain currents. The worst case situation is obviously the paralleling of devices with the widest possible variation in $r_{DS(on)}$. Two wafer lots of the MTP8N18 were sampled to obtain some idea of the range of variation of $r_{DS(on)}$ within the same wafer lot and between wafer lots. In addition to information on $r_{DS(on)}$, Table 1 contains data on the parameters important to dynamic current sharing which will be addressed later. From this information, one will have to design for a worst case $r_{DS(on)}$ mismatch of 30%.

$r_{DS(on)}$ is influenced by the magnitude of the drain current and the junction temperature. I_D and T_J are, in turn, a function of the power dissipation, which is strongly dependent upon $r_{DS(on)}$. The quality of heatsinking and thermal coupling between devices also affects I_D and T_J. These interdependent relationships make an analytical attempt to determine the degree of current sharing between several devices with a given $r_{DS(on)}$ mismatch rather complicated. An example of an iterative analytical process used to accomplish this end follows. The estimated I_D mismatch is somewhat dependent on the initial assumptions.

Design requirements could include the following:

1. Maximum desired junction temperature is 125°C.
2. Sufficient heatsinking will be supplied to maintain a 90°C case temperature when T_A = 35°C during maximum power dissipation.
3. Assume worst case $r_{DS(on)}$ mismatch for the MTP8N18 is 0.230 to 0.400 ohms @ I_D = 4A and T_J = 25°C.

From these conditions, the worst case variation in I_D, P_D and T_J needs to be determined. First, the thermal coefficient of $r_{DS(on)}$, denoted C_T, must be determined from the on-resistance vs. drain current curve (Figure 1).

$$C_T\Big|_{I_D = 8A} = \frac{\Delta r_{DS(on)}}{\Delta T} = \frac{r_{DS(on)}\Big|_{T_J = 100°C} - r_{DS(on)}\Big|_{T_J = 25°C}}{100°C\text{-}25°C}$$

$$= \frac{.47 - .32\ \Omega}{75°C} = 0.002\,\Omega/°C$$

In addition to assuming that C_T is invariant with temperature and drain current, it is also supposed that thermal coupling between device heat sinks is negligible. From the maximum desired junction temperature (T_J = 125°C), case temperature (T_C = 90°C), and the junction to case thermal resistance ($R_{\theta JC}$ = 1.67°C/W) of the MTP8N18, the maximum power dissipation and case to ambient thermal resistance are easily calculated.

$$P_D = \frac{T_{JC}}{R_{\theta JC}} = \frac{125\text{-}90°C}{1.67°C/W} = 20.96W$$

$$R_{\theta CA}\ \frac{T_{CA}}{P_D} = \frac{90\text{-}35°C}{20.96W} = 2.62°C/W$$

Attention is then focused on the device with the lowest $r_{DS(on)}$ since it will be dissipating the most power. At a T_J of 125°C its $r_{DS(on)}$, drain current, and V_{DS} are:

$$r_{DS(on)}\Big|_{T_J = 125°C} = r_{DS(on)}\Big|_{T_J = 25°C} + (T_J - 25°C)\,C_T$$

$$= .230 + (125\text{-}25).002$$

$$= .430\,\Omega$$

$$I_D = \sqrt{\frac{P_D}{r_{DS(on)}}} = \sqrt{\frac{20.96}{.430}} = 6.98 \approx 7Amp$$

$$V_{DS} = I_D * r_{DS(on)} = (7) * (.430) = 3.0\ Volts$$

To determine the operating conditions of a high resistance device operated in parallel with a low resistance device, an iterative technique must be employed. The approach is to estimate the junction temperature of the cooler device and from that, compute the $r_{DS(on)}$ at that T_J, the current and power dissipated, and the new junction temperature. The computations are then repeated until the process converges on the correct solution.

The first iteration proceeds as follows:

For $T_J = 100°C$:

$$r_{DS(on)}\Big|_{T_J = 100°C} = r_{DS(on)}\Big|_{T_J = 25°C} + (T_J - 25°C)C_T$$

$$= .400 + (100-25)\ .002 = .550\ \Omega$$

$$P_D = \frac{V^2}{r_{DS(on)}} = \frac{3^2}{.550} = 16.36W$$

$$T_{JC} = P_D * R_{\theta JC} = 16.36 * 1.67 = 27.33°C$$

$$T_{CA} = P_D * R_{\theta CA} = 16.36 * 2.62 = 42.87°C$$

$$T_J = T_{JC} + T_{CA} + T_A = 27.33 + 42.87 + 35 = 105.2°C$$

After two more iterations, the algorithm converges. The results are tabulated for comparison with those of the low resistance device in Table 2. In addition to the case of negligible thermal coupling, the idealized situation of perfect thermal coupling of the cases is also included for direct comparison. The performance tradeoff between the two examples is that little thermal coupling will achieve a greater degree of current sharing at the expense of a higher junction temperature in the hottest device (119°C vs 125°C). Since $T_{J(max)}$ most directly influences reliability, close thermal coupling of devices is encouraged. The manufacturer can best do this by paralleling chips on a common heat sink.

A point essential to the above calculations is that the steady state thermal resistance was employed to compute the junction temperatures. For pulsed conditions $R_{\theta JC}$ can vary significantly, and the transient thermal resistance obtained from the thermal response curves must be used to make this calculation. During switching transitions, there is insufficient time to establish differences in junction temperature and power MOSFETs may not current share in the same manner.

Dynamic Current Sharing Design Considerations

The term "dynamic" is broadened here to include not only current during turn-on and turn-off, but also peak current during narrow pulses and small duty cycles. Under these conditions, not enough RMS current is present to cause differential heating of the junctions which triggers the tendencies of the devices to share current. Since the argument supporting current sharing under static conditions is based on differences in junction temperature due to an imbalance of power dissipation and drain currents, that reasoning does not support the concept of current sharing during dynamic conditions. However, even without the benefit of the positive temperature coefficient, power MOSFETs can current share reasonably well with simple and efficient gate drive circuitry.

The issues of greatest concern to those interested in dynamic current sharing of paralleled MOSFETs are listed and described in order below.

1. Device parameters that influence dynamic current sharing.
2. Variation of pertinent device parameters from lot to lot.
3. Required device parameter matching to achieve safe levels of current distribution.
4. The effects of switching speed on dynamic current sharing.
5. The requirements and effects of circuit layout.
6. The possiblity of self induced oscillations.

TABLE 2
Static Current Sharing Performance of Mismatched MTP8N18s

	Negligible Thermal Case Coupling		Perfect Thermal Case Coupling	
	$r_{DS(on)}$ Min Device	$r_{DS(on)}$ Max Device	$r_{DS(on)}$ Min Device	$r_{DS(on)}$ Max Device
$r_{DS(on)}$ @ $T_J = 25°C$ (Ohms)	0.230	0.400	0.230	0.400
I_D (Amps)	7.00	5.38	7.14	5.24
P_D (Watts)	21.0	16.1	21.3	15.7
Steady State T_J(°C)	125	104	119	110
$r_{DS(on)}$ @ Steady State T_J(Ω)	0.430	0.558	0.419	0.570

Device Parameters That Influence Dynamic Current Sharing

The device parameters that influence the degree of dynamic current sharing are the transconductance (g_{fs}), gate-source threshold voltage ($V_{GS(TH)}$), input capacitance, and the on-resistance $r_{DS(on)}$. However, the device characteristic that most accurately predicts how well paralleled MOSFETs will current share during turn-on or turn-off is the transconductance curve, i.e., the relationship between the drain current and the gate-source voltage. To obtain optimum current distribution during turn-on and turn-off, the ideal situation is to have all gate-source voltages rising (or falling) simultaneously on devices with identical transconductance curves. This combination would ensure that as the devices switch through the active region, none would be overstressed by a current imbalance. Figures 2a, b, and c show the nearly perfect degree of current sharing obtainable solely by matching the g_{fs} curves. The current probe used induced a 20ns delay in the current waveform in the oscillograms shown.

Since plotting the entire g_{fs} curve of each device is very time consuming, matching $V_{GS(TH)}$ or g_{fs} at some drain current has been suggested as a simpler criterion for matching paralleled MOSFETs. While much of the literature suggests the importance of matching $V_{GS(TH)}$, which is normally defined as the minimum gate voltage at which a small drain current (usually specified as 1.0 mA) begins to flow, this does not accurately indicate the shape of the I_D vs. V_{GS} curve at higher currents. Devices with 1.0 mA thresholds that vary by as much as 2 volts do not usually, but can, have nearly identical transconductance curves above 100 mA. Conversely, those devices out of a group of one hundred MTP8N18s found to have the widest variation of g_{fs} curves had thresholds that varied by only 4%. Therefore, for optimum current sharing, the ideal solution is to use devices with identical g_{fs} curves, and comparing thresholds may not be the best way to achieve this.

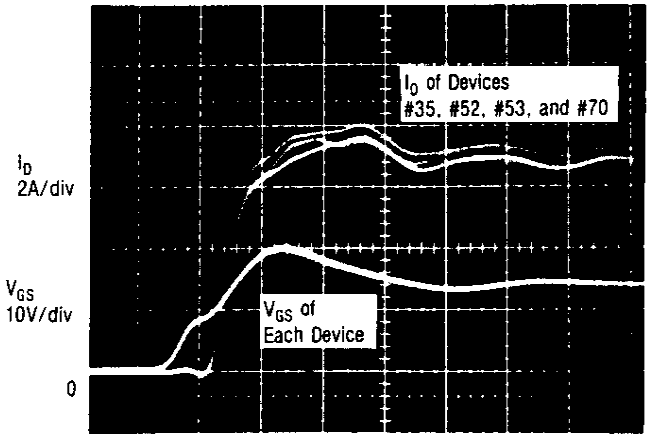

FIGURE 2a — Paralleled Turn-On

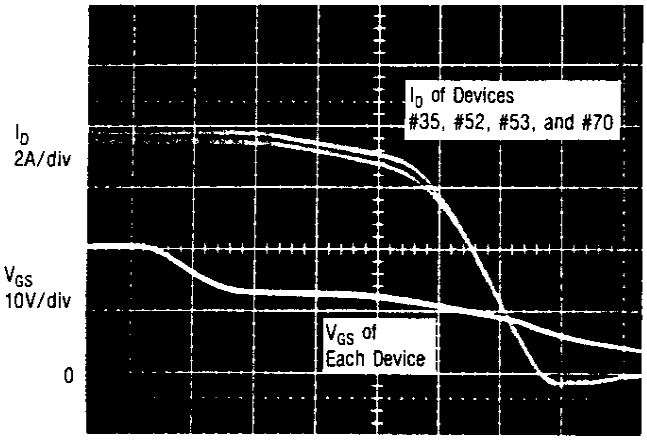

FIGURE 2b — Paralleled Turn-Off

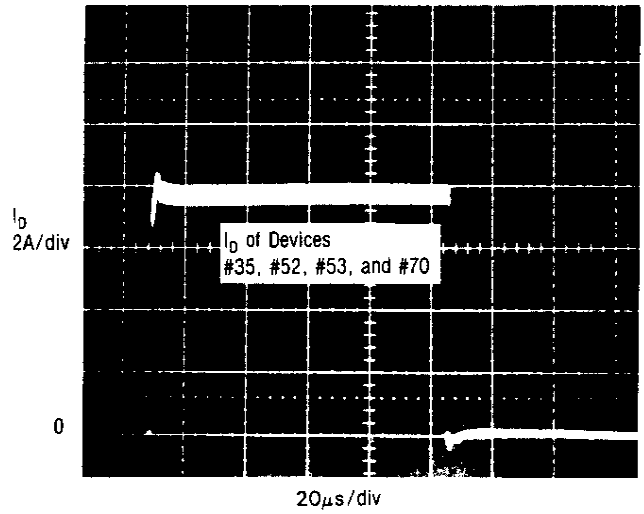

FIGURE 2c — Composite I_D Waveform for Turn-On and Turn-Off

FIGURE 2 — Individual I_D Waveforms of Four Paralleled MTP8N18s with Matched Transconductance Curves -Resistive Load (Drain Current Waveforms are delayed 20ns)

Another simple, yet more consistent, method is to match devices by comparing the maximum drain current they will conduct at a gate voltage higher than $V_{GS(TH)}$. For example, all four devices shown in Figure 2, conduct an I_D of 4.0 A at a V_{GS} of 6.0 volts and were found to have nearly identical g_{fs} curves (Figure 3). Though similar to matching thresholds, this method matches points on the g_{fs} curve that are more germane to the intended application of the devices.

Variation of Pertinent Device Parameters from Lot to Lot.

Before any definitive statement may be made concerning the degree or type of matching required for safe dynamic current sharing, the variation of pertinent device parameters from lot to lot must be known. Two wafer lots of the MTP8N18s, with sample sizes of 100 and 50 units respectively, were characterized for this purpose. The maximum and minimum values of threshold voltage, transconductance, and on-resistance are shown in Table 1. Figure 4 illustrates the widest variation in g_{fs} curves within Wafer Lot I and is similar to the results obtained from Wafer Lot II.

Obviously, the possibility of larger than expected variations in these pertinent parameters diminishes as the number of sampled wafer lots increases. To get an adequate sampling of available devices, the user could characterize devices with different date codes or obtain units from several distributors.

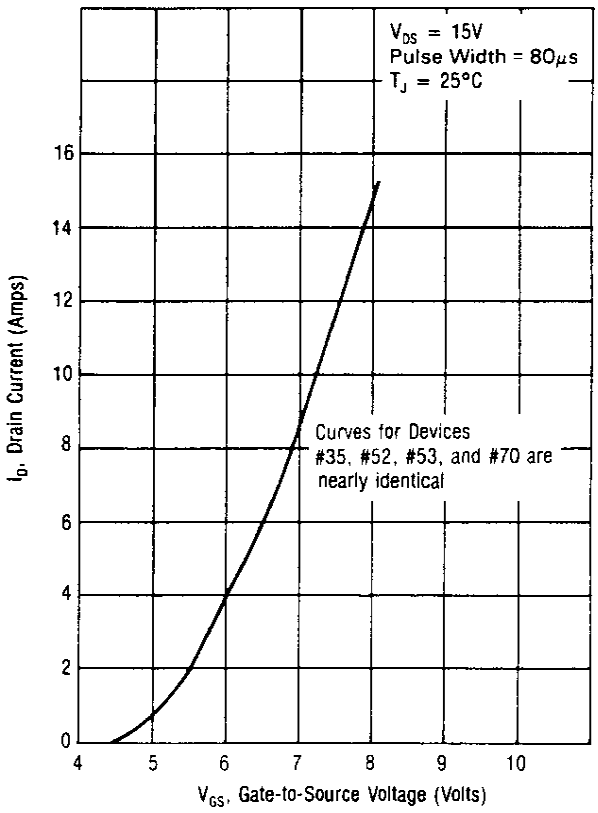

FIGURE 3 — Transconductance Curves of Matched MTP8N18s

Required Matching for Safe Levels of Current Distribution.

After characterization and determining the degree of variation possible, the effects of matching or mismatching the critical device characteristics can be observed. The circuit used for this study is shown in Figure 5. Some of the possible modifications of the circuit include adding resistors in series with the gate to slow the turn-on and turn-off, and a second MOSFET may be included to clamp the gate bus to ground to observe the effects of very rapid turn-off.

In this discussion of resistive switching, Figure 2 will serve as a standard for comparisons since matching transconductance curves has achieved such good performance. Extreme care was taken to provide as pure a resistive load as possible. The 1.6 ohm load was constructed from 39 62-ohm carbon composition resistors connected in parallel between two copper plates. Though the drain wiring and load inductances were very small, during rapid turn-on, the L/R time constant of the circuit may be the factor that limits the current rise times and not the switching speed of the MOSFETs.

One of the worst case situations is to parallel devices with greatly mismatched g_{fs} curves. Representing the widest variation in the g_{fs} curves in Wafer Lot I, Figure 4 shows the curve of a device that will begin to turn on with a rising V_{GS} slightly sooner than the other three devices. It may be expected that device #33 will turn on

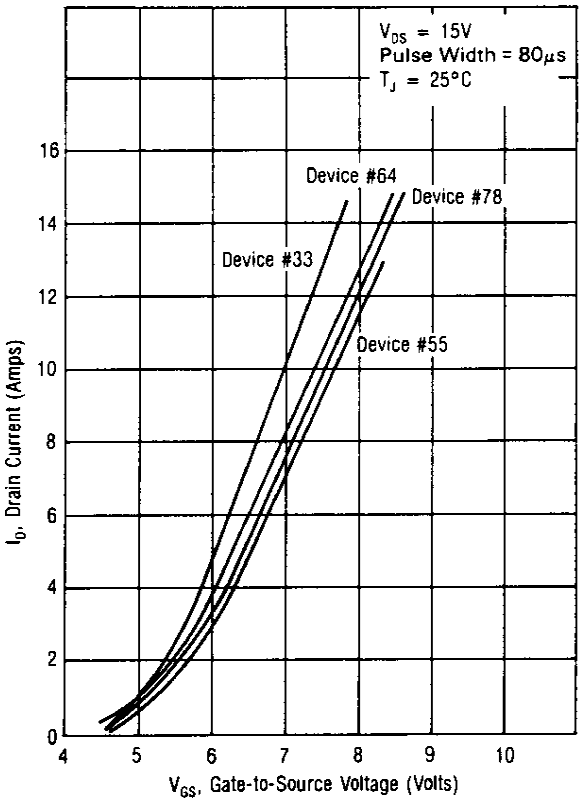

FIGURE 4 — Widest Variation in Transconductance Curves Found in Wafer Lot I.

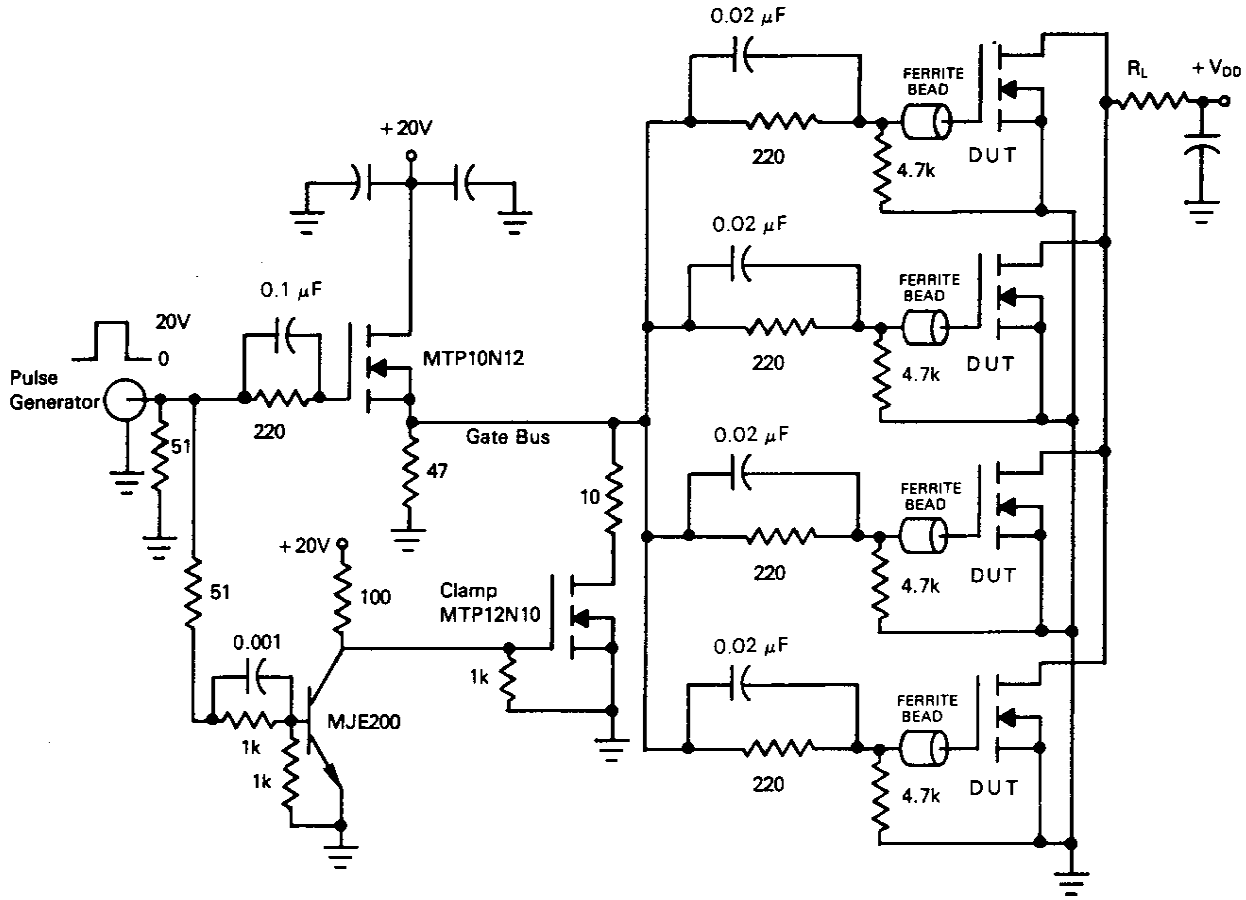

FIGURE 5 — Dynamic Current Sharing Test Circuit

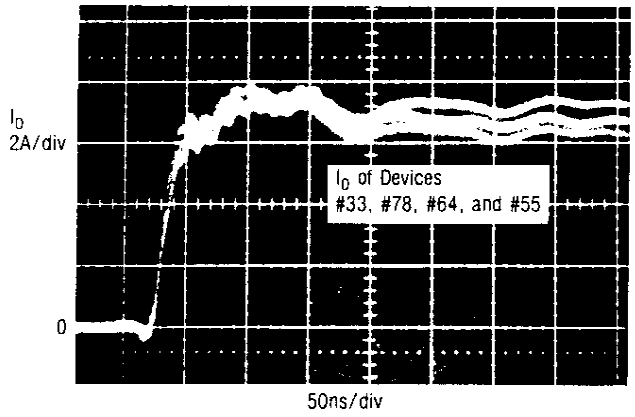

FIGURE 6a — Paralleled Turn-On

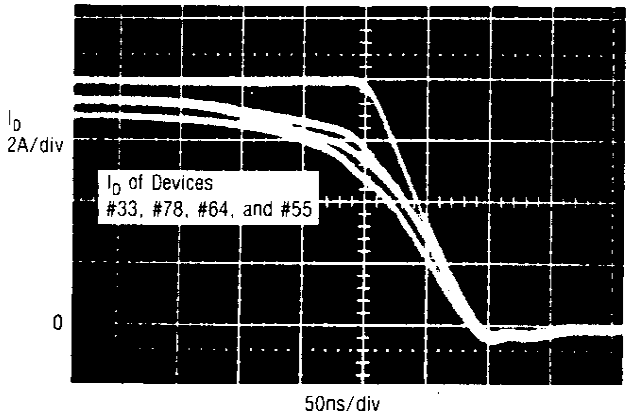

FIGURE 6b — Paralleled Turn-Off

FIGURE 6 — Individual I_D Waveforms of Four Paralleled MTP8N18s with Mismatched Transconductance Curves -Resistive Load

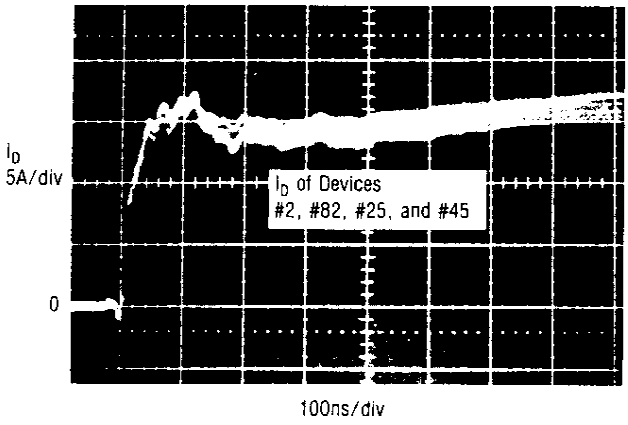

FIGURE 7a — Paralleled Turn-On

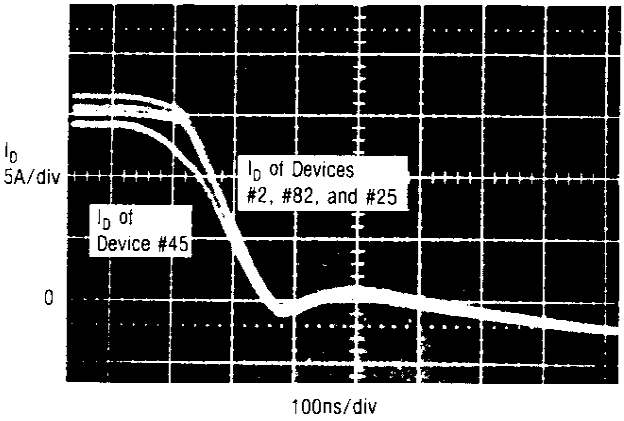

FIGURE 7b — Paralleled Turn-Off

FIGURE 7 — Individual I_D Waveforms of Four Paralleled MTP8N18s with Matched Transconductance Curves -Resistive Load

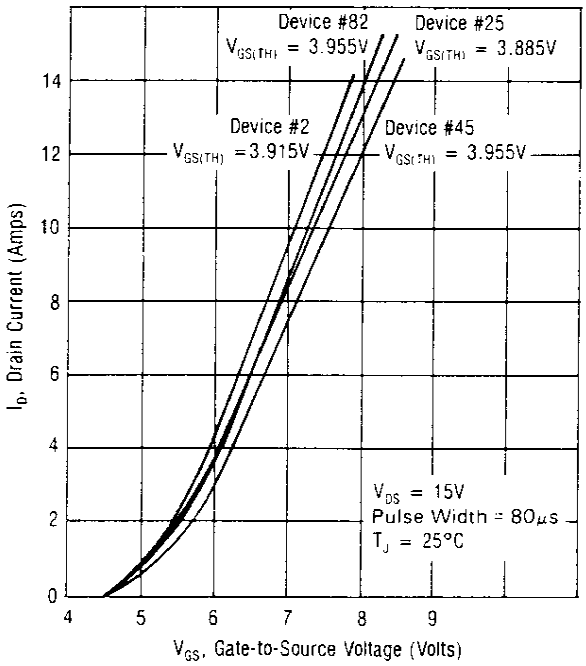

FIGURE 8 — Transconductance Curves of MTP8N18s with Matched Threshold Voltages

Waveform / Curve Relations

Note: The order of the device numbers shown in all the current waveforms is important. The first number indicates the upper current waveform in each group with succeeding curves corresponding to the following device numbers. The order of waveforms is identified to enable the reader to correlate the devices' performance in the current waveforms to the devices' g_{fs} curves provided.

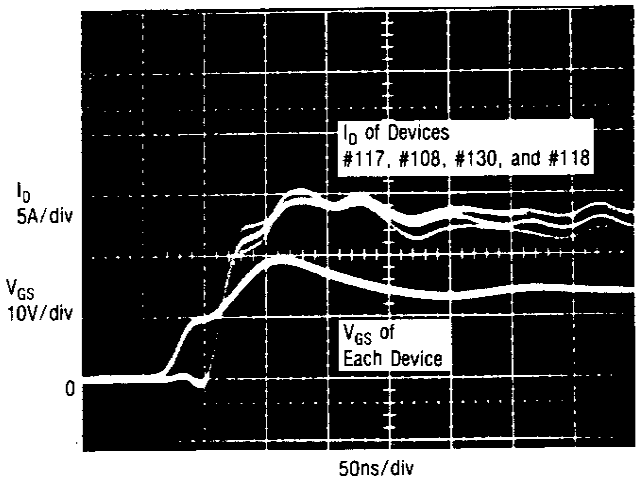

FIGURE 9a — Paralleled Turn-On

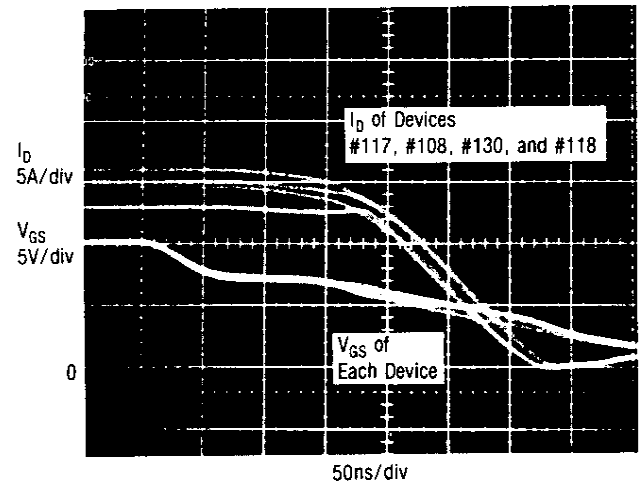

FIGURE 9b — Paralleled Turn-Off

FIGURE 9 — Individual I_D Waveforms of Four MTP8N18s with Matched Transconductance Curves and Mismatched Threshold Voltages

first and possibly fail due to current overload. However, since the variation in the I_D vs V_{GS} curves of these mismatched devices is small, the failure will not occur. As shown in Figure 6, parallel operation of these mismatched devices in the given circuit poses no significant reliability hazard.

Matching the 1.0 mA thresholds does not guarantee the nearly perfect results of matching the g_{fs} curves, as shown in Figure 7. Although their thresholds were matched to within 2%, these devices exhibited a fairly wide variation in g_{fs} curves (Figure 8) which resulted in device #45 beginning its turn-off slightly sooner than the rest. The waveform photos again indicate that the performance of this group is also quite adequate. For comparison, the devices in Figures 9 and 10 have fairly similar g_{fs} curves even though their 1.0 mA threshold voltages vary by as much as 33%. Turn-on times for this group are almost simultaneous while the turn-off is just short of ideal.

Because the MTP8N18s of the two wafer lots were so close in characteristics, the worst conceivable mismatch that could occur could not be found. In order to study the effects of such a wide disparity between parameters, an MTP12N10 was paired with three closely matched MTP8N18s. The MTP12N10 is a 12A, 100V device with the same die dimensions as the MTP8N18. Table 3 and Figure 11 compare the the different device characteristics. The result of paralleling these four devices is shown in Figure 12.

The MTP12N10 is the last device to begin turn-on even though its transconductance curve rises earlier than those of the MTP8N18s. This is due to the larger C_{RSS} (reverse transfer or gate-drain capacitance) which is effectively multiplied in value by the device gain due to the Miller effect. Although not completely simultaneous, the turn-off is smooth. By the time the MTP8N18s have completely switched off, the MTP12N10 has moved well into the active, or constant current region. At that time, the total load current has been substantially reduced and the slightly unsynchronized turn-off posed no threat to the MTP12N10 at these switching speeds.

It is apparent that for this specific application, i.e., resistive switching at moderate switching speed, device matching improves paralleled performance but is not necessary for safe operation. This recommendation will be extended to include both fast and slow switching speeds for both resistive and inductive loads provided certain circuit layout criteria are met.

TABLE 3
Parameter Comparison of One MTP12N10 and Three MTP8N18s

Device Number	Device Type	$r_{DS(on)}$ I_D = 4A (Ohm)	$V_{GS(TH)}$ I_D = 1mA (Volts)	g_{fs} I_D = 4A V_{GS} = 15V (Volts)	C_{RSS} (pF)	C_{ISS} (pF)	C_{OSS} (pF)
#122	MTP12N10	0.145	3.600	4.300	90	685	395
#52	MTP8N18	0.238	3.955	4.762	45	700	220
#53	MTP8N18	0.256	3.900	4.444	45	700	245
#70	MTP8N18	0.255	3.930	4.444	45	700	235

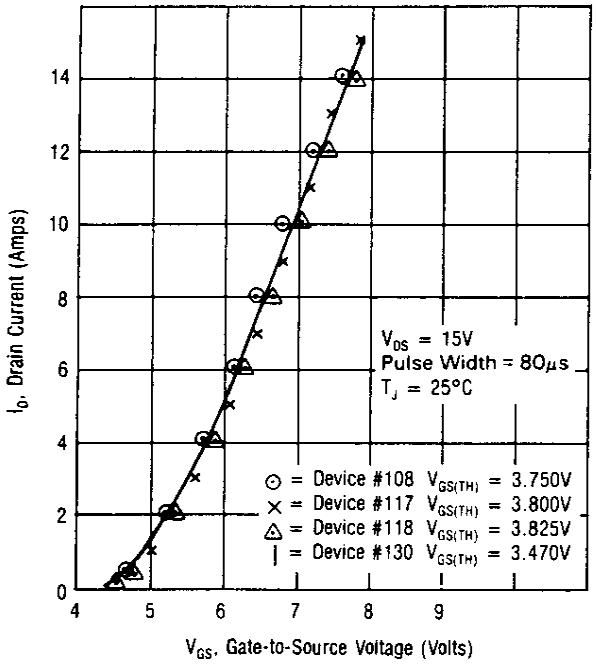

FIGURE 10 — Transconductance Curves of MTP8N18s with Threshold Voltage $V_{GS(TH)}$ Mismatch

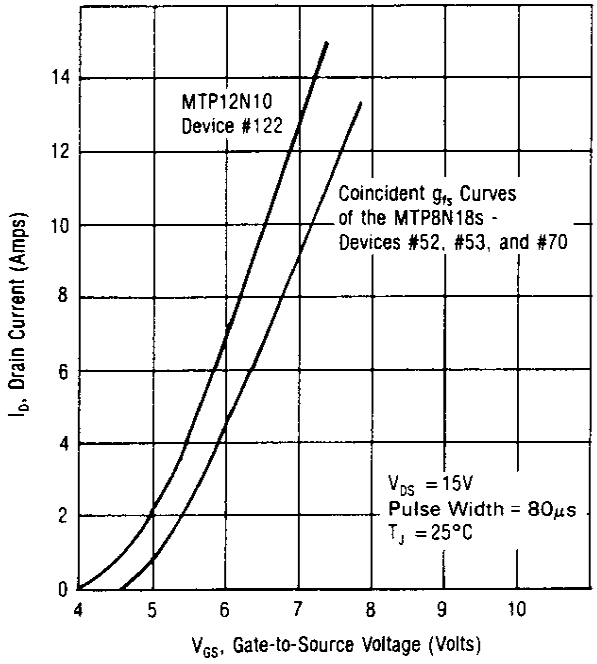

FIGURE 11 — Transconductance Curves of an MTP12N10 and three MTP8N18s

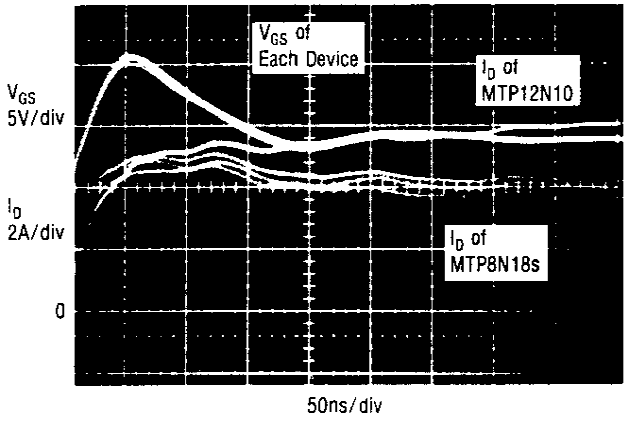

FIGURE 12a — Paralleled Turn-On

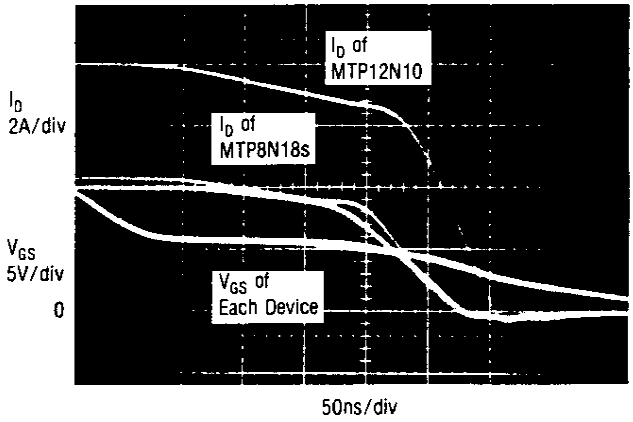

FIGURE 12b — Paralleled Turn-Off

FIGURE 12 — Individual I_D Waveforms of an MTP12N10 Paralleled with Three MTP8N18s - Resistive Load

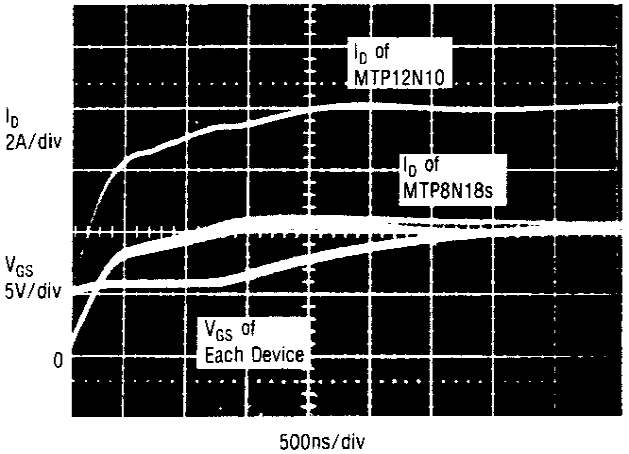

FIGURE 13a — Paralleled Turn-On

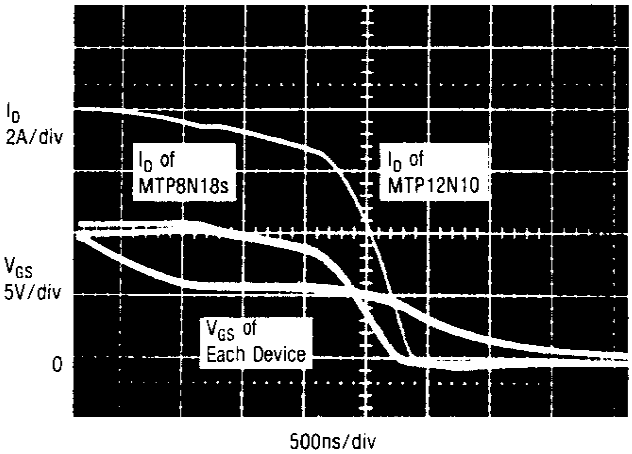

FIGURE 13b — Paralleled Turn-Off

FIGURE 13 — Individual I_D Waveforms of an MTP12N10 Paralleled with Three MTP8N18s - Resistive Load - Slow Switching

Effects of Switching Speed on Dynamic Current Sharing

The gate drive circuit used to switch the MTP12N10 and the three MTP8N18s was altered to either increase or decrease the switching speed. The four 0.02 μF speed-up capacitors were removed to determine the quality of current sharing as the gate-source voltages rise or fall at speeds that are fairly slow for power MOSFETs. The MTP12N10 is the first to turn on and the last to turn off (Figure 13) due to the differences in the devices' g_{fs} curves. During slow switching, the g_{fs} vs. V_{GS} curves can be used to accurately predict the I_D curves. For instance, the MTP12N10 begins to turn on when the composite gate-source voltage waveform reaches 4 volts, but the MTP8N18s hesitate until V_{GS} reaches 4.5 volts. Since the I_D waveforms are easily related via the g_{fs} curves to the rising or falling gate voltages and the variation in the g_{fs} curves over a product line are fairly small, slow switching of unmatched TMOS power MOSFETs can be a safe undertaking.

To judge the effects of rapid turn-off, a second MOSFET was added to clamp the gate to ground. This method achieves the 20ns current fall times depicted in Figure 14. During such rapid switching, the V_{GS} and g_{fs} curves can no longer be used to accurately predict device performance due to package and lead parasitics such as the package source inductance. Once again however, these mismatched devices performed well as they were switched very rapidly through the active region. Although not quite as predictable, rapid resistive switching also appears safe.

A comparison of Figures 12, 13, and 14 indicates that faster switching tends to improve dynamic current sharing. This is in part a consequence of switching the devices through the active region at a much faster rate and correspondingly decreasing any difference in switching speeds. The parasitic source inductance also plays an important role as discussed below.

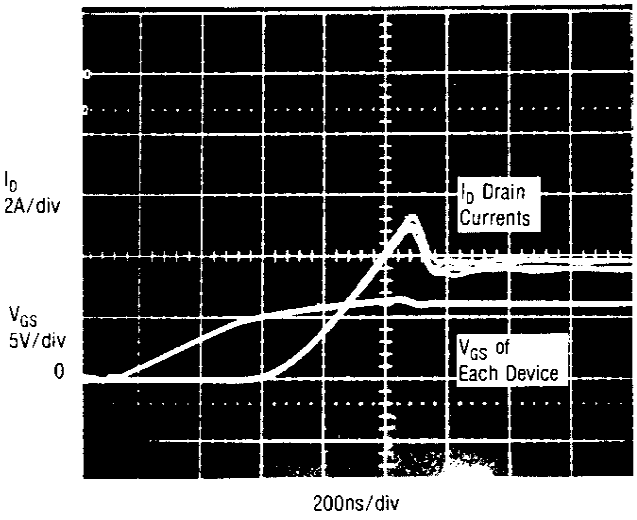

FIGURE 15a — Paralleled Turn-On

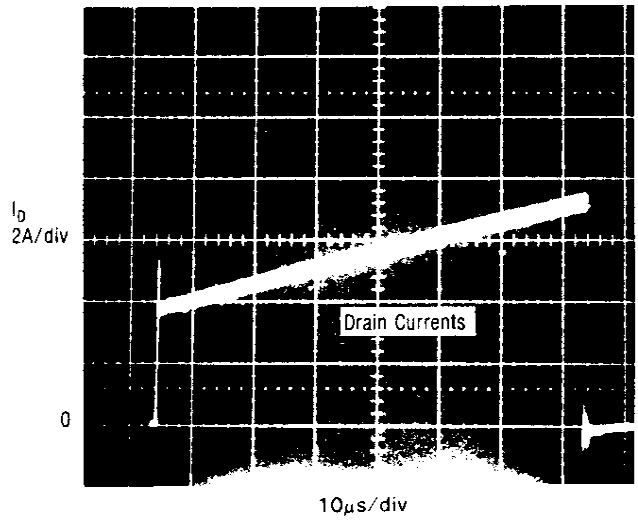

FIGURE 15b — Composite Turn-on and Turn-off Waveform

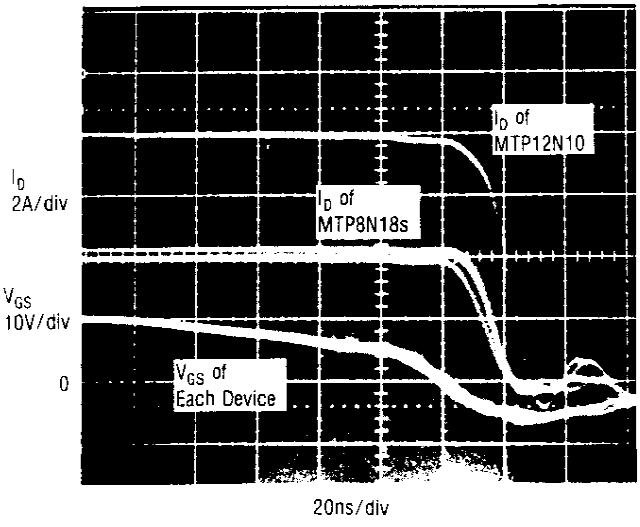

FIGURE 14 — Individual I_D Waveforms of an MTP12N10 Paralleled with Three MTP8N18s - Resistive Load - Rapid Turn-Off

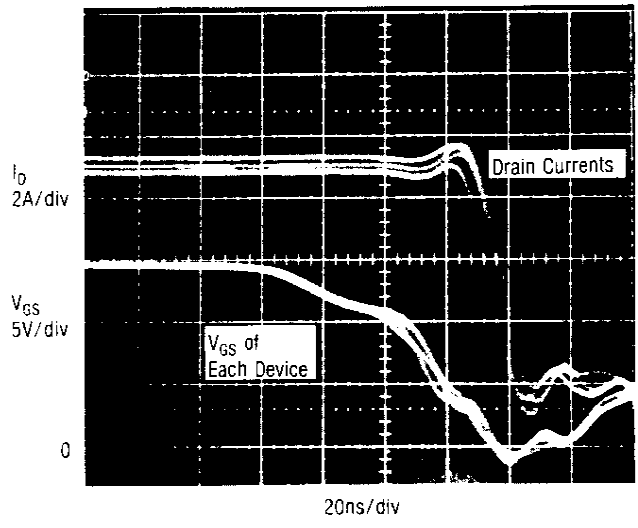

FIGURE 15C — Paralleled Turn-Off

FIGURE 15 — Individual I_D Waveforms of Matched MTP8N18s Switching an Inductive Load - Devices #36, #52, #53, and #70

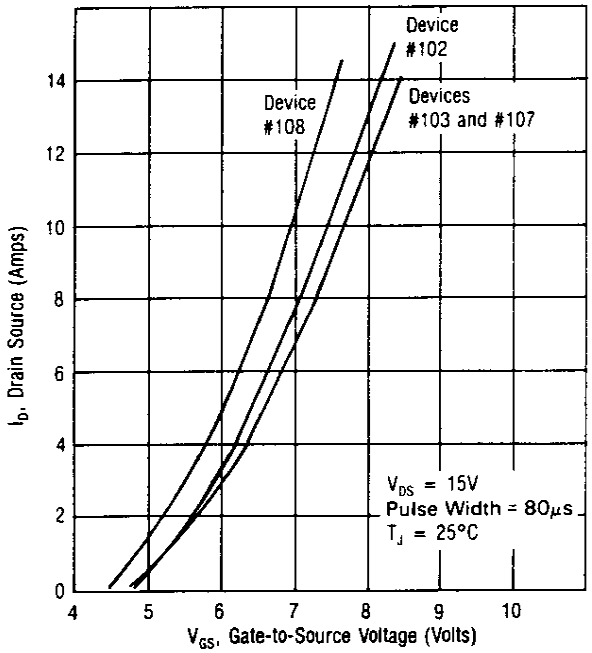

FIGURE 16 — Widest Variation in Transconductance Curves of 250 Additional MTP8N18s

Dynamic Current Sharing With Inductive Loads.

The investigation of the effects of current sharing with inductive loads was conducted using a fast recovery diode (40A, 400V) placed in parallel with a 135 μH inductor as a load. The diode was included not so much to protect the MOSFET against flyback voltages, but to test the paralleled transistors' ability to conduct the large peak reverse recovery current required by the diode. The standard of performance is again set by devices with matched g_{fs} curves and is shown in Figure 15.

To obtain a larger sample size for the worst case inductive testing, 250 additional MTP8N18s of unknown wafer origin were characterized for their widest variation in g_{fs} curves. The mismatched transconductance curves are shown in Figure 16. Figure 17 depicts both rapid and slow inductive turn-on and turn-off. This group of figures represents the greatest current imbalance seen in any set of mismatched MTP8N18s under any load conditions. While there are obvious current mismatches, they require only a small amount of derating to guardband against possible harmful situations. The keys to success are: 1) that pertinent device characteristics do not vary widely; and, 2) that strict attention is given to the symmetry of the circuit layout.

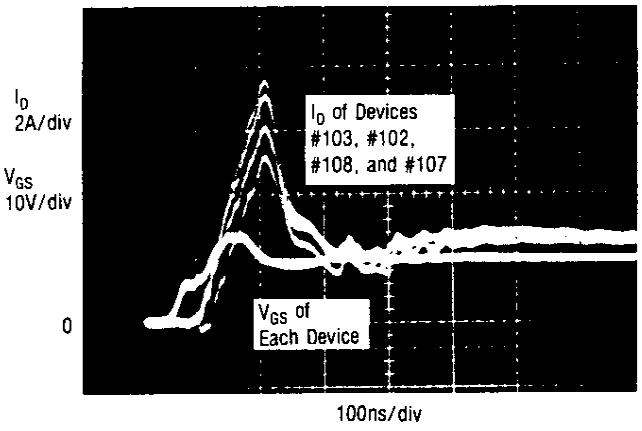

FIGURE 17a — Rapid Turn-On Supplying Reverse Recovery Current of Freewheeling Diode

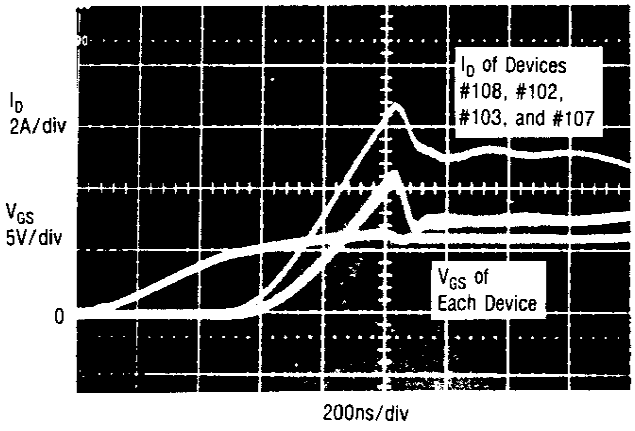

FIGURE 17b — Slow Turn-On Supplying Reverse Recovery Current of Freewheeling Diode

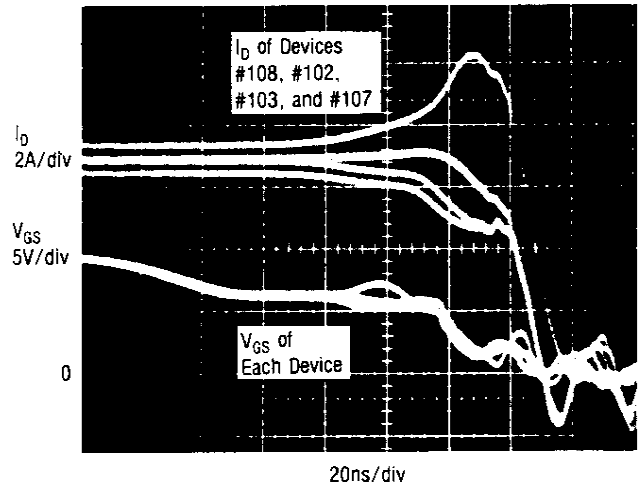

FIGURE 17c — Rapid Inductive Turn-Off

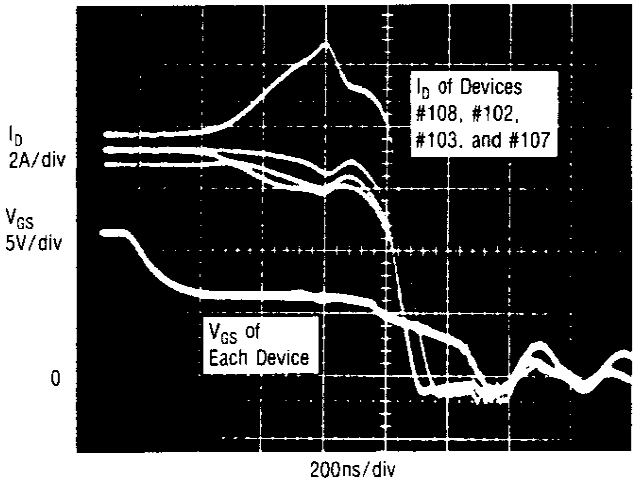

FIGURE 17d — Slow Inductive Turn-Off

FIGURE 17 — Individual I_D Waveforms of Mismatched MTP8N18s Switching an Inductive Load

Circuit Layout — A Critical Concern

Even with identically matched devices, dynamic current sharing between MOSFETs will be poor if an asymmetrical circuit layout is used. Obviously, if the gate drives are different, unequal rates of gate-source voltage rise and fall can cause unsynchronized switching and even device failure in extreme cases. As the switching speeds of these devices are increased, the designer's perception as to what may constitute an important parasitic circuit element must change. When approaching the maximum switching speeds of power MOSFETs, even small variations in lead length may influence their paralleled switching performance. Unequal source wiring inductances are especially deleterious.

Figures 18a and 18b illustrate the effects of an imbalance in source wiring inductance. The devices and circuit layout are both closely matched except that an additional source lead inductance of 50 nH (1.5 inches of #22 wire formed into a 1½ turn loop) was added to one device. As can be seen in the photographs, any source lead or wiring inductance will degenerate both the turn-on and turn-off speeds. Fortunately, perhaps the most important consideration for successful operation of paralleled MOSFETs is completely within easy control of the circuit designer. The circuit should be free from parasitics and as symmetrical as possible, especially for higher switching speeds.

Another obvious consideration is that the output impedance of the gate drive circuits must be matched. Mismatched gate drives will cause unsynchronized charging or discharging of the input capacitances, forcing the devices to begin switching at different times and rates.

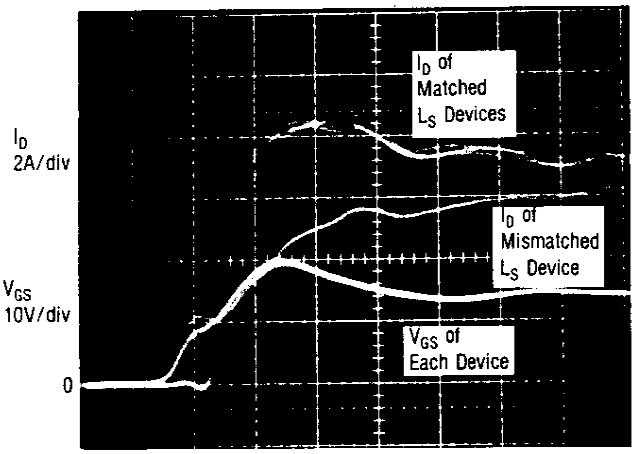

FIGURE 18a — Turn-On

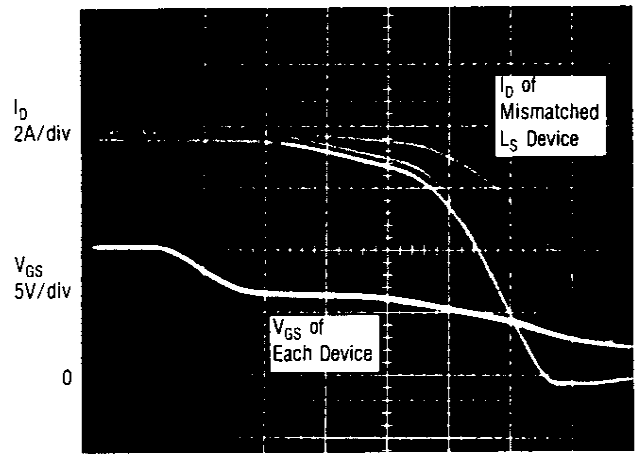

FIGURE 18b — Turn-Off

FIGURE 18 — Effects of Imbalanced Source Inductances on Paralleled Performance

The Benefit of Parasitic Source Inductance

Provided that the circuit layout is symmetrical, especially with respect to the source wiring inductance, faster switching can actually benefit the degree of current sharing between paralleled MOSFETs. During switching transitions of less than 100 ns, the source package inductance (approximately 7 nH) plays an important part in determining the shape of the rising and falling drain current waveform. The following example assumes the wiring inductance is negligible and relates only the effect of the source package inductance. The intent of this illustration is to show the significance of the package inductance and by extention relate the importance of the usually much larger wiring inductance.

Assuming a very rapid turn-off accompanied by a di/dt of 8A/50ns, the voltage appearing across the parasitic lead inductance is approximately 1.1 volts ($v = L\ di/dt$ = 7 nH x 8A/50ns). This inductive drop must be added to the voltage appearing across the gate-source terminals to reveal the potential impressed at the chip. A difference in gate voltage of this size makes a significant difference in the magnitude of the drain current as the device switches through the active region. Therefore, equal source inductances will tend to equalize the rate of the rise and fall of the individual drain currents during rapid switching of paralleled MOSFETs. In effect, source ballasting is achieved during rapid switching.

Protecting the Circuit From Self-Induced Oscillations

Two of the most highly esteemed characteristics of the power MOSFET can combine to cause a problem in paralleled devices. Their high input impedance and very high frequency response may cause parasitic oscillations at frequencies greater than 100 MHz. This problem occurs when all gates are driven directly from a common node as in the circuit of Figure 19. Without individual gate resistances a high-Q network (Figure 20) is established that may cause the device to oscillate when operating or switching through the active region. The device transconductance, gate-to-drain parasitic capacitance, and source and gate parasitic inductances have all been shown to influence the stability of the circuit.

Although potentially serious, this problem is easily averted. By decoupling the gates of each device with lossy elements such as resistors or ferrite beads, the Q of the

circuit can be sufficiently degraded to the point that oscillations are no longer possible (note dotted resistors shown in Figure 19). For the maximum switching speeds, the value of gate decoupling resistors should be kept as low as safely allowable. A value in the range of 10 to 20 ohms is generally sufficient.

Conclusions

The following is a summary of recommendations and findings concerning current sharing in paralleled power MOSFETs.

1. For static current sharing, the current mismatches are determined by the $r_{DS(on)}$ mismatch. A small degree of guardbanding or $r_{DS(on)}$ matching will ensure safe operation.
2. For dynamic current sharing, the turn-on and turn-off waveforms are largely determined by the transconductance curves. If matching is deemed necessary in a particular application, selecting devices by comparing g_{fs} curves is the most accurate approach. A simple, yet adequate, substitute is to match a single point on the g_{fs} curves at which the devices conduct significant drain currents.
3. Increasing the switching speeds in symmetrical circuits tends to equalize the rate of current rise and fall in paralleled devices due to the ballasting effect of the parasitic source inductance.
4. The circuit layout should be as symmetrical as possible with respect to the gate drive and the source, gate, and drain parasitic inductances.
5. In all applications, the gates should be decoupled with small resistors or ferrite beads to eliminate parasitic oscillations.

Reference:

Kassakian, John G., "Some Issues Related To The Behavior of Multiple Paralled Power MOSFETs," Electrical Power Systems Engineering Laboratory, M.I.T., Cambridge, Massachusetts 02139.

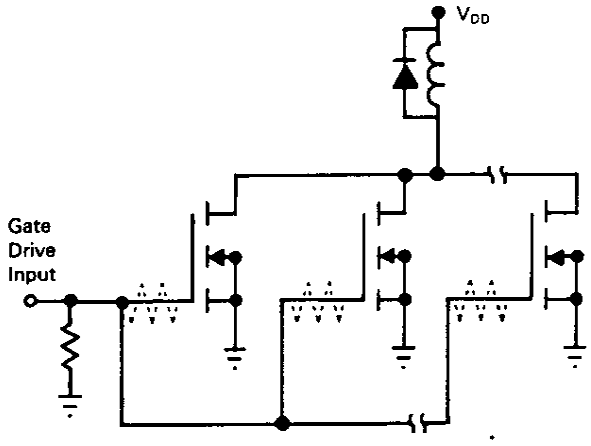

FIGURE 19 — Method for Driving Paralleled MOSFETs Using Gate Decoupling Resistors

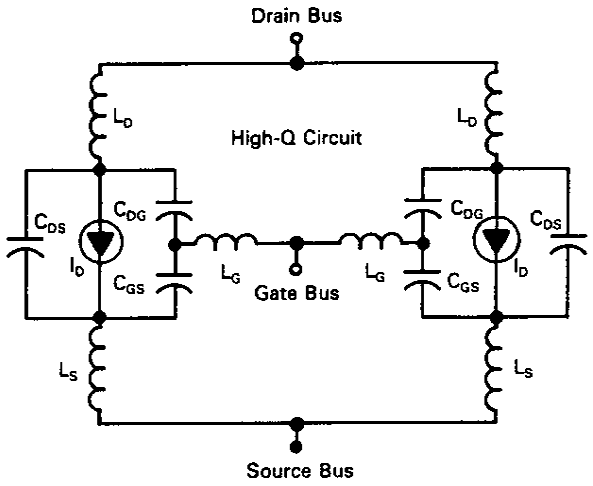

FIGURE 20 - Parasitic High-Q Equivalent Circuit of Paralleled MOSFETs without Gate Decoupling Resistors

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