

MC74HCT14A

Hex Schmitt-Trigger Inverter with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

The MC74HCT14A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

The HCT14A is useful to “square up” slow input rise and fall times. Due to the hysteresis voltage of the Schmitt trigger, the HCT14A finds applications in noisy environments.

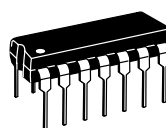
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates



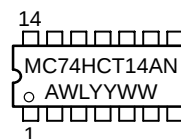
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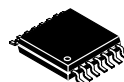
MARKING DIAGRAMS



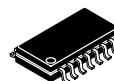
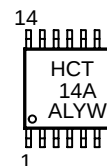
PDIP-14
N SUFFIX
CASE 646



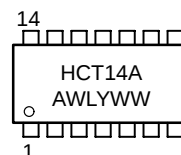
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



EIAJ-14
F SUFFIX
CASE 965

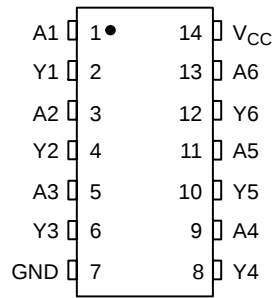


A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HCT14AN	PDIP-14	2000/Box
MC74HCT14AD	SOIC-14	55/Rail
MC74HCT14ADR2	SOIC-14	2500/Reel
MC74HCT14ADTR2	TSSOP-14	2000/Reel
MC74HCT14AFEL	EIAJ-14	2000/Reel

MC74HCT14A



FUNCTION TABLE

Input A	Output Y
L	H
H	L

Figure 1. Pin Assignment

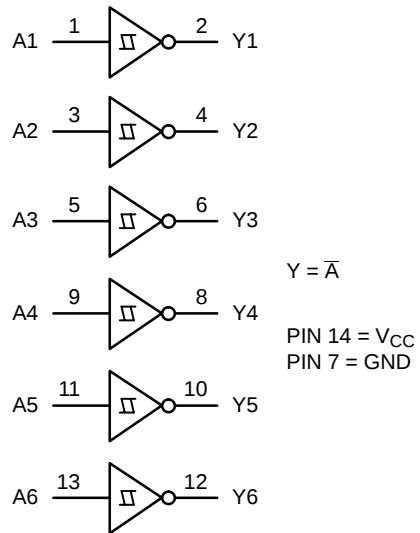


Figure 2. Logic Diagram

MC74HCT14A

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	− 0.5 to + 7.0	V
V _I	DC Input Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage (Referenced to GND)	− 0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 25	mA
I _O	DC Output Sink Current	± 25	mA
I _{CC}	DC Supply Current per Supply Pin	± 50	mA
I _{GND}	DC Ground Current per Ground Pin	± 50	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance PDIP SOIC TSSOP	78 125 170	°C/W
P _D	Power Dissipation in Still Air at 85°C PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% - 35%	UL-94-VO (0.125 in)	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>4000 >300 >1000	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and Below GND at 85°C (Note 5)	± 300	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.
6. For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _I , V _O	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	− 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 3)	—	(Note 7)	ns

7. No Limit when V_I ≈ 50% V_{CC}, I_{CC} > 1 mA.
8. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

MC74HCT14A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC}	Temperature Limit						Unit
			Volts	–55°C to 25°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
V _{T+} max	Maximum Positive-Going Input Threshold Voltage	V _O = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5		1.9 2.1		1.9 2.1		1.9 2.1	V
V _{T+} min	Minimum Positive-Going Input Threshold Voltage	V _O = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	1.2 1.4		1.2 1.4		1.2 1.4		V
V _{T–} max	Maximum Negative-Going Input Threshold Voltage	V _O = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5		1.2 1.4		1.2 1.4		1.2 1.4	
V _{T–} min	Minimum Negative-Going Input Threshold Voltage	V _O = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	0.5 0.6		0.5 0.6		0.5 0.6		
V _H max	Maximum Hysteresis Voltage	V _O = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5		1.4 1.5		1.4 1.5		1.4 1.5	
V _H min	Minimum Hysteresis Voltage	V _O = 0.1 V or V _{CC} – 0.1 V I _{out} ≤ 20 μA	4.5 5.5	0.4 0.4		0.4 0.4		0.4 0.4		
V _{OH}	Minimum High-Level Output Voltage	V _I < V _{T–} min I _{out} ≤ 20 μA	4.5 5.5	4.4 5.4		4.4 5.4		4.4 5.4		V
		V _I < V _{T–} min I _{out} ≤ 4.0 mA	4.5	3.98		3.84		3.7		
V _{OL}	Maximum Low-Level Output Voltage	V _I ≥ V _{T+} max I _{out} ≤ 20 μA	4.5 5.5		0.1 0.1		0.1 0.1		0.1 0.1	V
		V _I ≥ V _{T+} max I _{out} ≤ 4.0 mA	4.5		0.26		0.33		0.4	
I _{IK}	Maximum Input Leakage Current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per package)	V _I = V _{CC} or GND I _{out} = 0 μA	5.5		1.0		10		40	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _I = 2.4 V, Any One Input V _I = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ –55°C		25°C to 125°C				mA
				2.9		2.4				

9. Information on typical parametric values can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS (C_L = 50 pF; Input t_r = t_f = 6.0 ns)

Symbol	Parameter	Test Conditions	Figures	Guaranteed Limit						Unit
				− 55°C to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Output Y (L to H)	V _{CC} = 5.0 V ± 10% C _L = 50 pF, Input t _r = t _f = 6.0 ns	3 & 4		32		40		48	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output	V _{CC} = 5.0 V ± 10% C _L = 50 pF, Input t _r = t _f = 6.0 ns	3 & 4		15		19		22	ns

10. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance, per Inverter (Note 11)	Typical @ 25°C, V _{CC} = 5.0 V	pF
		32	

11. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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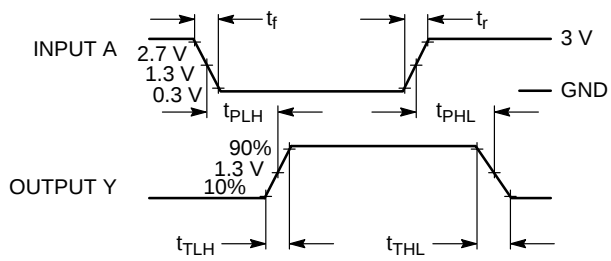
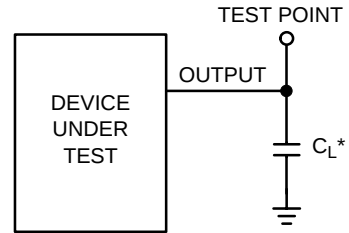


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance.

Figure 4. Test Circuit

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