

MC74VHC4051, MC74VHC4052, MC74VHC4053

Analog Multiplexers / Demultiplexers High-Performance Silicon-Gate CMOS

The MC74VHC4051, MC74VHC4052 and MC74VHC4053 utilize silicon-gate CMOS technology to achieve fast propagation delays, low ON resistances, and low OFF leakage currents. These analog multiplexers/demultiplexers control analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The VHC4051, VHC4052 and VHC4053 are identical in pinout to the high-speed HC4051A, HC4052A and HC4053A, and the metal-gate MC14051B, MC14052B and MC14053B. The Channel-Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

The Channel-Select and Enable inputs are compatible with standard CMOS outputs; with pullup resistors they are compatible with LSTTL outputs.

These devices have been designed so that the ON resistance (R_{ON}) is more linear over input voltage than R_{ON} of metal-gate CMOS analog switches.

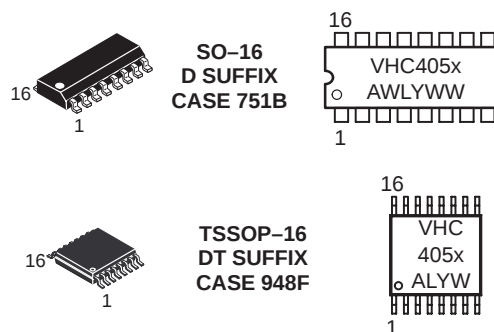
- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Diode Protection on All Inputs/Outputs
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = 2.0 to 12.0 V
- Digital (Control) Power Supply Range ($V_{CC} - GND$) = 2.0 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal-Gate Counterparts
- Low Noise
- Chip Complexity: VHC4051 — 184 FETs or 46 Equivalent Gates
VHC4052 — 168 FETs or 42 Equivalent Gates
VHC4053 — 156 FETs or 39 Equivalent Gates



ON Semiconductor

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MARKING DIAGRAMS

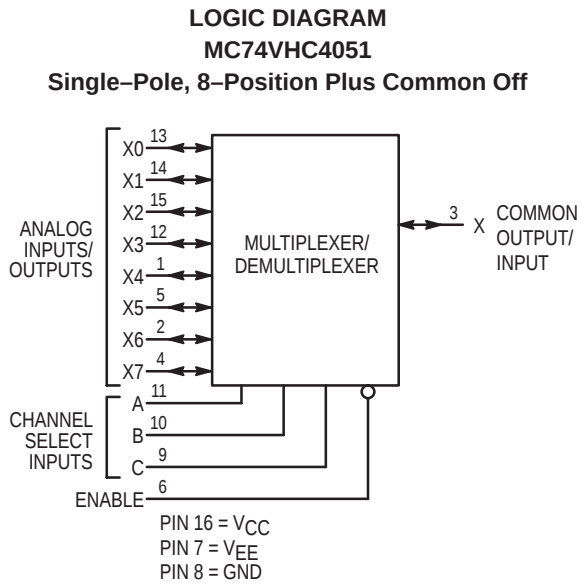


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

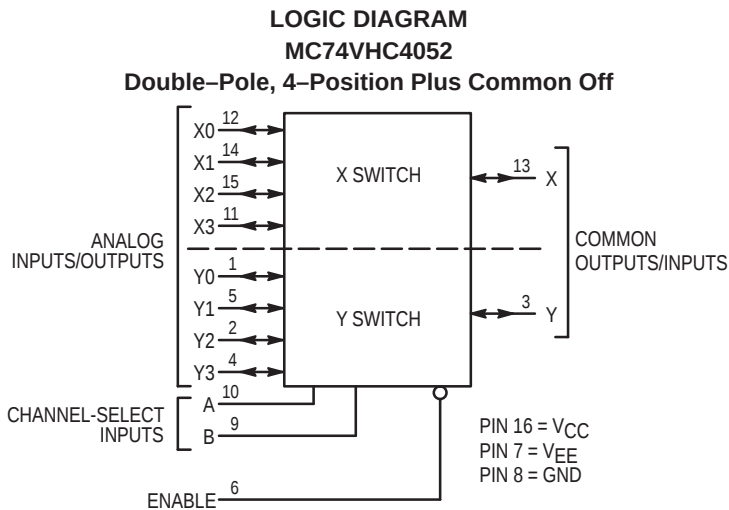
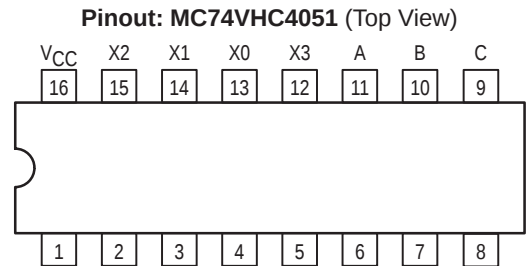
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

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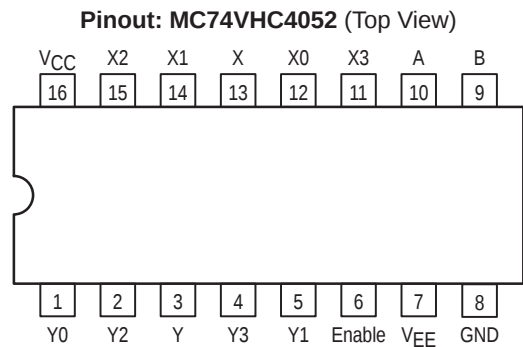
Control Inputs				ON Channels
Enable	Select			
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care



Control Inputs				
Enable	Select			
	B	A	ON Channels	
L	L	L	Y0	X0
L	L	H	Y1	X1
L	H	L	Y2	X2
L	H	H	Y3	X3
H	X	X	NONE	

X = Don't Care

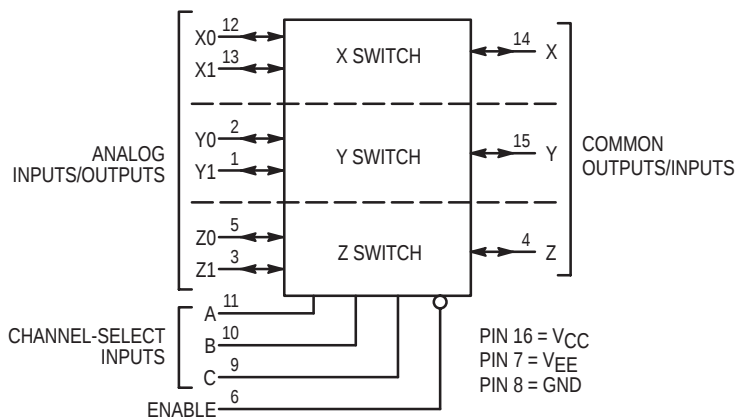


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LOGIC DIAGRAM

MC74VHC4053

Triple Single-Pole, Double-Position Plus Common Off



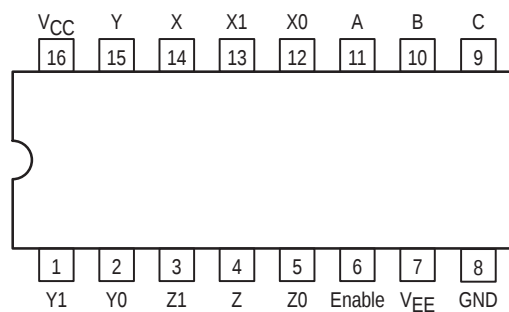
NOTE: This device allows independent control of each switch. Channel-Select Input A controls the X-Switch, Input B controls the Y-Switch and Input C controls the Z-Switch

FUNCTION TABLE – MC74VHC4053

Control Inputs						
Enable	Select					
	C	B	A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

Pinout: MC74VHC4053 (Top View)



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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V _{EE})	– 0.5 to + 7.0 – 0.5 to + 14.0	V
V _{EE}	Negative DC Supply Voltage (Referenced to GND)	– 7.0 to + 5.0	V
V _{IS}	Analog Input Voltage	V _{EE} – 0.5 to V _{CC} + 0.5	V
V _{in}	Digital Input Voltage (Referenced to GND)	– 0.5 to V _{CC} + 0.5	V
I	DC Current, Into or Out of Any Pin	± 25	mA
P _D	Power Dissipation in Still Air, SOIC Package† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature Range	– 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C

TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V _{EE})	2.0 2.0	6.0 12.0	V	
V _{EE}	Negative DC Supply Voltage, Output (Referenced to GND)	– 6.0	GND	V	
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V	
V _{in}	Digital Input Voltage (Referenced to GND)	GND	V _{CC}	V	
V _{IO} *	Static or Dynamic Voltage Across Switch		1.2	V	
T _A	Operating Temperature Range, All Package Types	– 55	+ 125	°C	
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs)	V _{CC} = 2.0 V V _{CC} = 3.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0 0	1000 800 500 400	ns

*For voltage drops across switch greater than 1.2V (switch on), excessive V_{CC} current may be drawn; i.e., the current out of the switch may contain both V_{CC} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

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DC CHARACTERISTICS — Digital Section (Voltages Referenced to GND) $V_{EE} = \text{GND}$, Except Where Noted

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage, Channel-Select or Enable Inputs	$R_{ON} = \text{Per Spec}$	2.0	1.50	1.50	1.50	V
			3.0	2.10	2.10	2.10	
			4.5	3.15	3.15	3.15	
			6.0	4.20	4.20	4.20	
V_{IL}	Maximum Low-Level Input Voltage, Channel-Select or Enable Inputs	$R_{ON} = \text{Per Spec}$	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
I_{in}	Maximum Input Leakage Current, Channel-Select or Enable Inputs	$V_{in} = V_{CC}$ or GND, $V_{EE} = -6.0 \text{ V}$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and $V_{IS} = V_{CC}$ or GND; $V_{EE} = \text{GND}$ $V_{IO} = 0 \text{ V}$ $V_{EE} = -6.0$	6.0	1	10	40	μA
			6.0	4	40	80	

DC ELECTRICAL CHARACTERISTICS Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					- 55 to 25°C	≤ 85°C	≤ 125°C	
R_{ON}	Maximum "ON" Resistance	$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ to V_{EE} $I_S \leq 2.0 \text{ mA}$ (Figures 1, 2)	3.0	0.0	200	240	320	Ω
			4.5	0.0	160	200	280	
			4.5	- 4.5	120	150	170	
			6.0	- 6.0	100	125	140	
		$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = V_{CC}$ or V_{EE} (Endpoints) $I_S \leq 2.0 \text{ mA}$ (Figures 1, 2)	3.0	0.0	150	180	230	
			4.5	0.0	110	140	190	
			4.5	- 4.5	90	120	140	
			6.0	- 6.0	80	100	115	
ΔR_{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	$V_{in} = V_{IL}$ or V_{IH} $V_{IS} = 1/2 (V_{CC} - V_{EE})$ $I_S \leq 2.0 \text{ mA}$	3.0	0.0	40	50	80	Ω
			4.5	0.0	20	25	40	
			4.5	- 4.5	10	15	18	
			6.0	- 6.0	10	12	14	
I_{off}	Maximum Off-Channel Leakage Current, Any One Channel	$V_{in} = V_{IL}$ or V_{IH} ; $V_{IO} = V_{CC} - V_{EE}$; Switch Off (Figure 3)	6.0	- 6.0	0.1	0.5	1.0	μA
	Maximum Off-Channel VHC4051 Leakage Current, VHC4052 Common Channel VHC4053	$V_{in} = V_{IL}$ or V_{IH} ; $V_{IO} = V_{CC} - V_{EE}$; Switch Off (Figure 4)	6.0	- 6.0	0.2	2.0	4.0	
			6.0	- 6.0	0.1	1.0	2.0	
I_{on}	Maximum On-Channel VHC4051 Leakage Current, VHC4052 Channel-to-Channel VHC4053	$V_{in} = V_{IL}$ or V_{IH} ; Switch-to-Switch = $V_{CC} - V_{EE}$; (Figure 5)	6.0	- 6.0	0.2	2.0	4.0	μA
			6.0	- 6.0	0.1	1.0	2.0	
			6.0	- 6.0	0.1	1.0	2.0	

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AC CHARACTERISTICS ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			−55 to 25°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Channel–Select to Analog Output (Figure 9)	2.0	270	320	350	ns
		3.0	90	110	125	
		4.5	59	79	85	
		6.0	45	65	75	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Analog Input to Analog Output (Figure 10)	2.0	40	60	70	ns
		3.0	25	30	32	
		4.5	12	15	18	
		6.0	10	13	15	
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	160	200	220	ns
		3.0	70	95	110	
		4.5	48	63	76	
		6.0	39	55	63	
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figure 11)	2.0	245	315	345	ns
		3.0	115	145	155	
		4.5	49	69	83	
		6.0	39	58	67	
C _{in}	Maximum Input Capacitance, Channel–Select or Enable Inputs		10	10	10	pF
C _{I/O}	Maximum Capacitance Analog I/O		35	35	35	pF
	(All Switches Off) Common O/I: VHC4051		130	130	130	
	VHC4052		80	80	80	
	VHC4053		50	50	50	
	Feedthrough		1.0	1.0	1.0	
C _{PD}	Power Dissipation Capacitance (Figure 13)*	Typical @ 25°C, V _{CC} = 5.0 V, V _{EE} = 0 V				pF
		VHC4051	45			
		VHC4052	80			
		VHC4053	45			

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V _{CC} V	V _{EE} V	Limit*			Unit
					25°C			
BW	Maximum On–Channel Bandwidth or Minimum Frequency Response (Figure 6)	f _{in} = 1MHz Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{OS} ; Increase f _{in} Frequency Until dB Meter Reads –3dB; R _L = 50Ω, C _L = 10pF			'51	'52	'53	MHz
			2.25	–2.25	80	95	120	
			4.50	–4.50	80	95	120	
			6.00	–6.00	80	95	120	
—	Off–Channel Feedthrough Isolation (Figure 7)	f _{in} = Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{IS} f _{in} = 10kHz, R _L = 600Ω, C _L = 50pF	2.25	–2.25	–50			dB
			4.50	–4.50	–50			
			6.00	–6.00	–50			
		f _{in} = 1.0MHz, R _L = 50Ω, C _L = 10pF	2.25	–2.25	–40			
			4.50	–4.50	–40			
			6.00	–6.00	–40			
—	Feedthrough Noise. Channel–Select Input to Common I/O (Figure 8)	V _{in} ≤ 1MHz Square Wave (t _r = t _f = 6ns); Adjust R _L at Setup so that I _S = 0A; Enable = GND R _L = 600Ω, C _L = 50pF	2.25	–2.25	25			mV _{pp}
			4.50	–4.50	105			
			6.00	–6.00	135			
		R _L = 10kΩ, C _L = 10pF	2.25	–2.25	35			
			4.50	–4.50	145			
			6.00	–6.00	190			
—	Crosstalk Between Any Two Switches (Figure 12) (Test does not apply to VHC4051)	f _{in} = Sine Wave; Adjust f _{in} Voltage to Obtain 0dBm at V _{IS} f _{in} = 10kHz, R _L = 600Ω, C _L = 50pF	2.25	–2.25	–50			dB
			4.50	–4.50	–50			
			6.00	–6.00	–50			
		f _{in} = 1.0MHz, R _L = 50Ω, C _L = 10pF	2.25	–2.25	–60			
			4.50	–4.50	–60			
			6.00	–6.00	–60			
THD	Total Harmonic Distortion (Figure 14)	f _{in} = 1kHz, R _L = 10kΩ, C _L = 50pF THD = THD _{measured} – THD _{source} V _{IS} = 4.0V _{pp} sine wave V _{IS} = 8.0V _{pp} sine wave V _{IS} = 11.0V _{pp} sine wave						%
			2.25	–2.25	0.10			
			4.50	–4.50	0.08			
			6.00	–6.00	0.05			

*Limits not tested. Determined by design and verified by qualification.

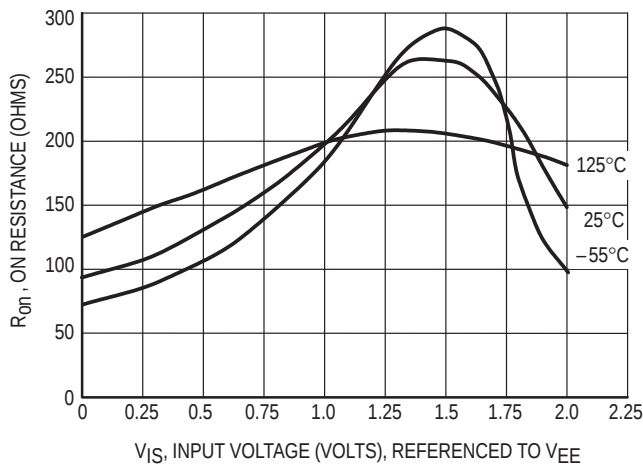


Figure 1a. Typical On Resistance, V_{CC} - V_{EE} = 2.0 V

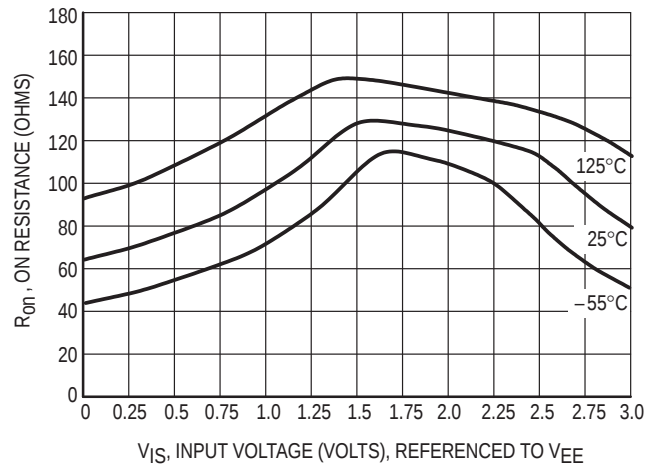


Figure 1b. Typical On Resistance, V_{CC} - V_{EE} = 3.0 V

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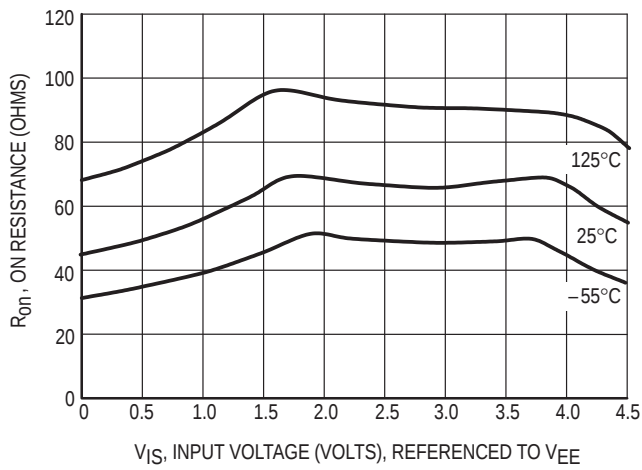


Figure 1c. Typical On Resistance, $V_{CC} - V_{EE} = 4.5\text{ V}$

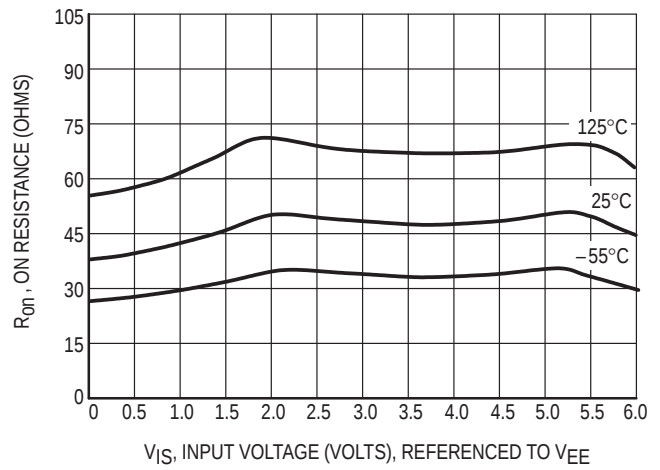


Figure 1d. Typical On Resistance, $V_{CC} - V_{EE} = 6.0\text{ V}$

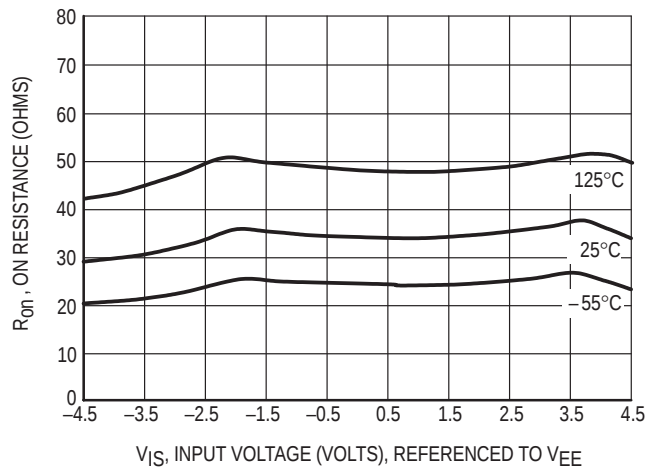


Figure 1e. Typical On Resistance, $V_{CC} - V_{EE} = 9.0\text{ V}$

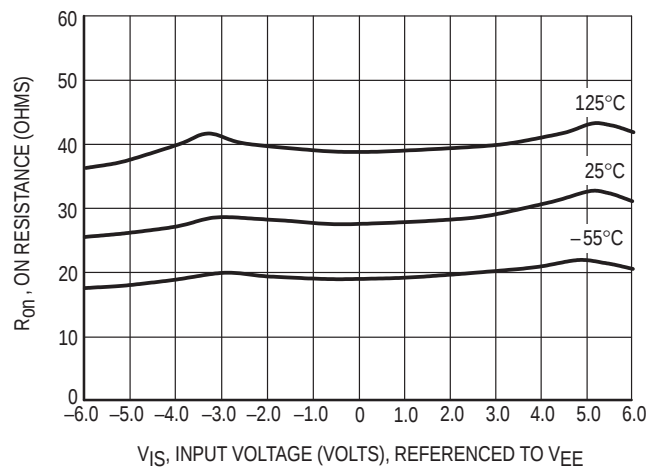


Figure 1f. Typical On Resistance, $V_{CC} - V_{EE} = 12.0\text{ V}$

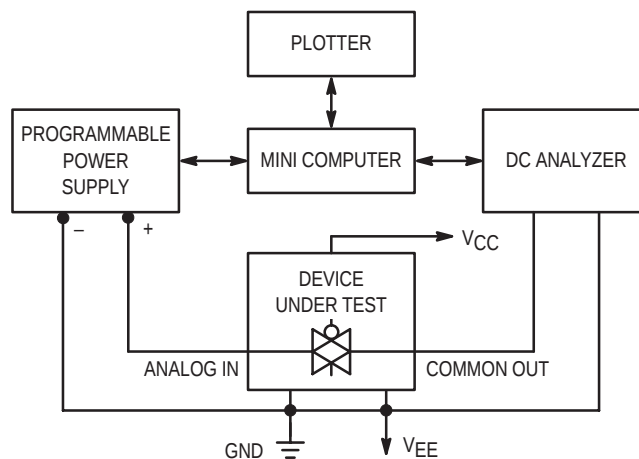


Figure 1. On Resistance Test Set-Up

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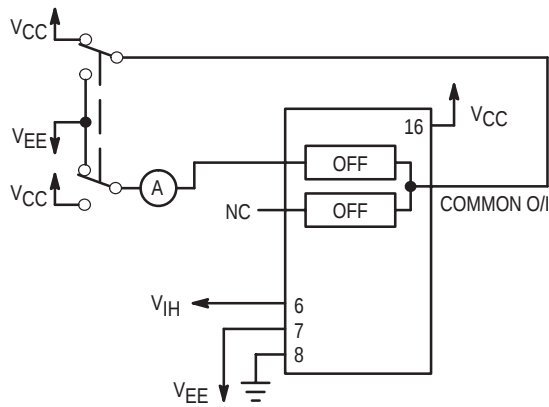


Figure 2. Maximum Off Channel Leakage Current, Any One Channel, Test Set-Up

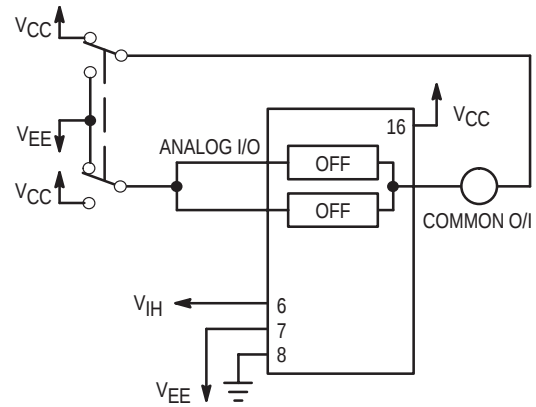


Figure 3. Maximum Off Channel Leakage Current, Common Channel, Test Set-Up

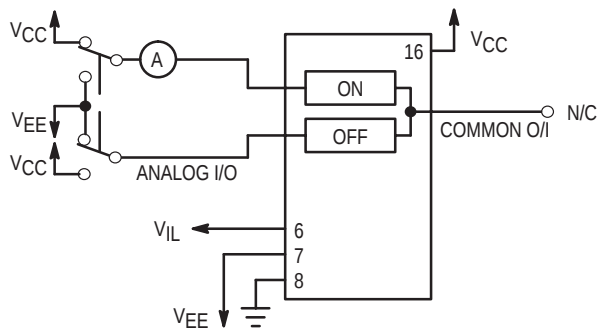


Figure 4. Maximum On Channel Leakage Current, Channel to Channel, Test Set-Up

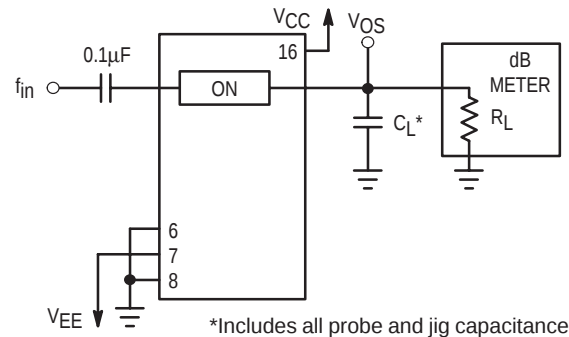


Figure 5. Maximum On Channel Bandwidth, Test Set-Up

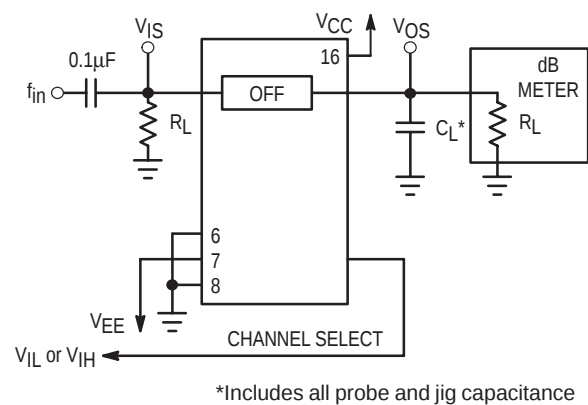


Figure 6. Off Channel Feedthrough Isolation, Test Set-Up

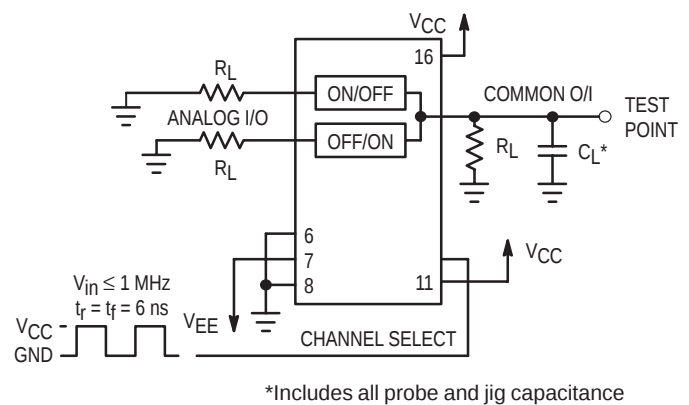


Figure 7. Feedthrough Noise, Channel Select to Common Out, Test Set-Up

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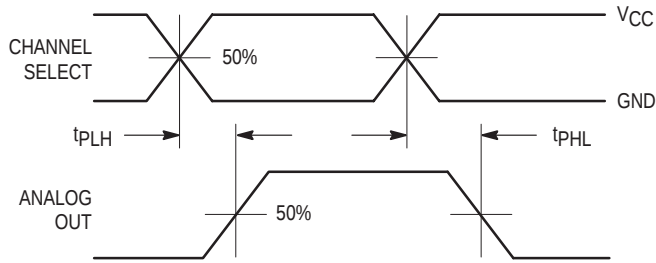
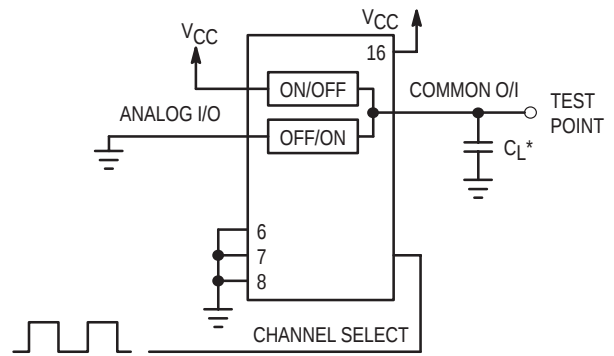


Figure 9a. Propagation Delays, Channel Select to Analog Out



*Includes all probe and jig capacitance

Figure 8b. Propagation Delay, Test Set-Up Channel Select to Analog Out

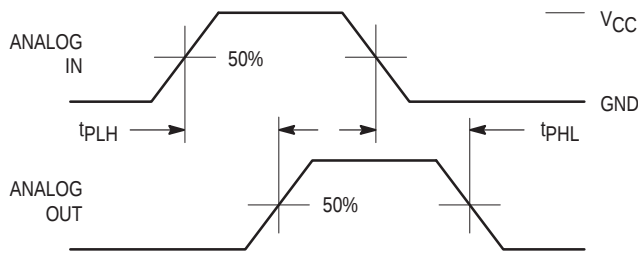
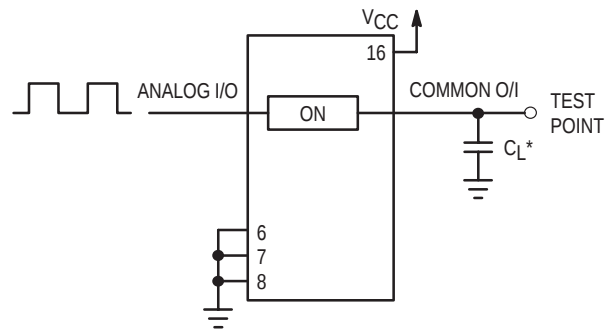


Figure 10a. Propagation Delays, Analog In to Analog Out



*Includes all probe and jig capacitance

Figure 9b. Propagation Delay, Test Set-Up Analog In to Analog Out

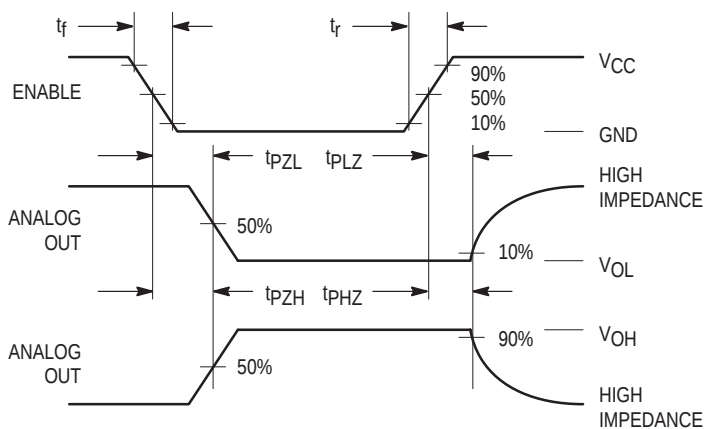


Figure 11a. Propagation Delays, Enable to Analog Out

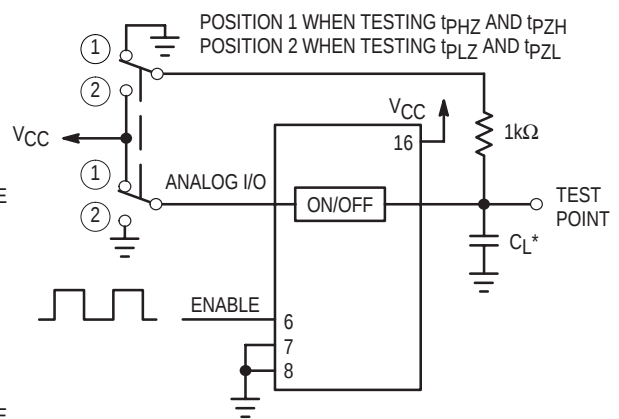
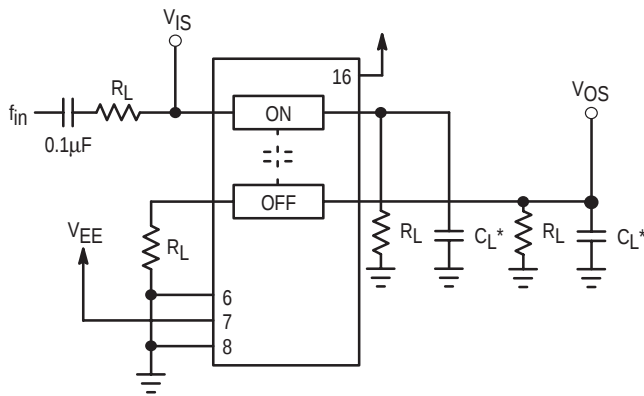


Figure 10b. Propagation Delay, Test Set-Up Enable to Analog Out

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*Includes all probe and jig capacitance

Figure 11. Crosstalk Between Any Two Switches, Test Set-Up

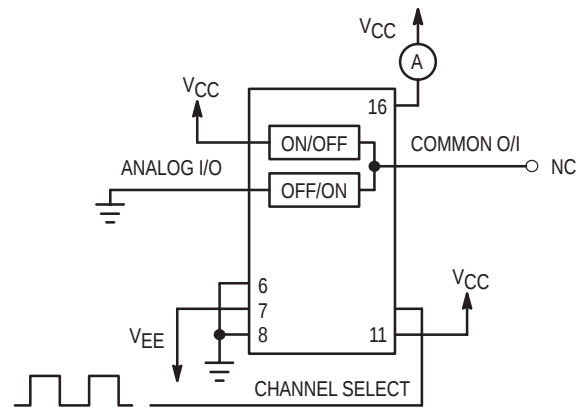
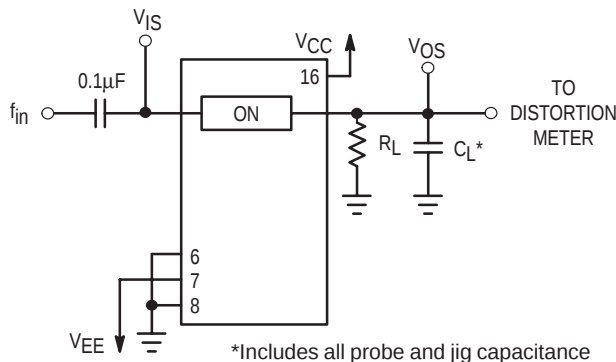


Figure 12. Power Dissipation Capacitance, Test Set-Up



*Includes all probe and jig capacitance

Figure 14a. Total Harmonic Distortion, Test Set-Up

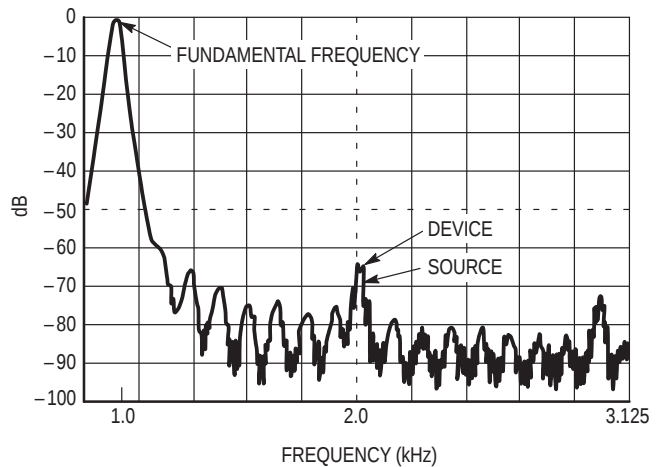


Figure 13b. Plot, Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$\begin{aligned} V_{CC} &= +5V = \text{logic high} \\ \text{GND} &= 0V = \text{logic low} \end{aligned}$$

The maximum analog voltage swings are determined by the supply voltages V_{CC} and V_{EE} . The positive peak analog voltage should not exceed V_{CC} . Similarly, the negative peak analog voltage should not go below V_{EE} . In this example, the difference between V_{CC} and V_{EE} is ten volts. Therefore, using the configuration of Figure 15, a maximum analog signal of ten volts peak-to-peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and

outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$\begin{aligned} V_{CC} - \text{GND} &= 2 \text{ to } 6 \text{ volts} \\ V_{EE} - \text{GND} &= 0 \text{ to } -6 \text{ volts} \\ V_{CC} - V_{EE} &= 2 \text{ to } 12 \text{ volts} \\ &\text{and } V_{EE} \leq \text{GND} \end{aligned}$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_X) are recommended as shown in Figure 16. These diodes should be able to absorb the maximum anticipated current surges during clipping.

MC74VHC4051, MC74VHC4052, MC74VHC4053

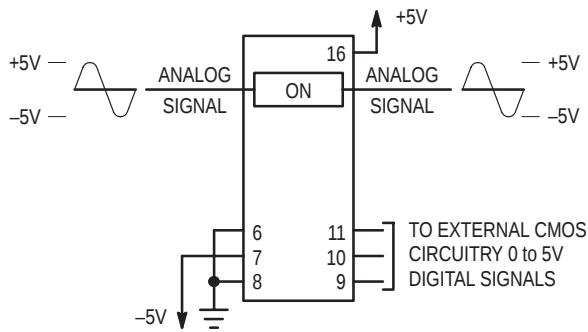


Figure 14. Application Example

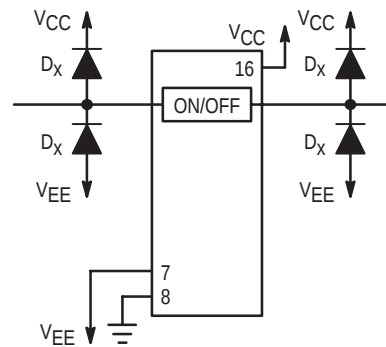
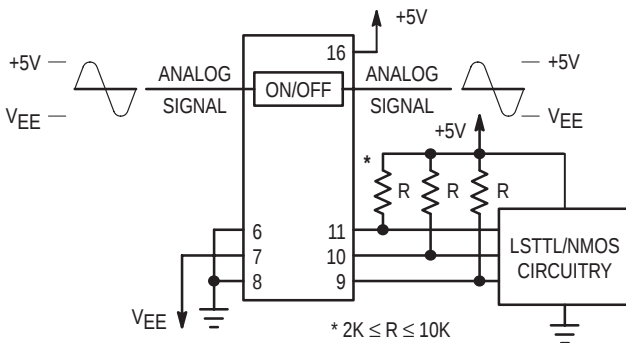
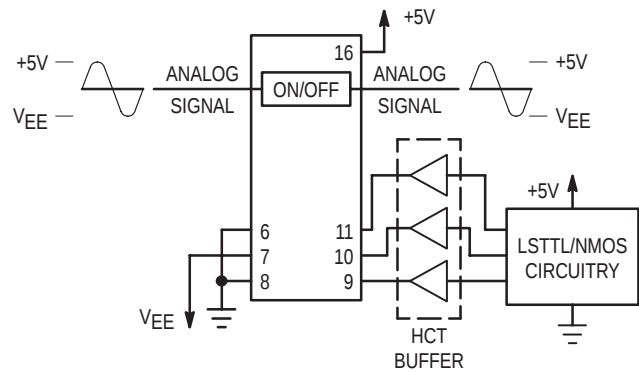


Figure 15. External Germanium or Schottky Clipping Diodes



a. Using Pull-Up Resistors



b. Using HCT Interface

Figure 16. Interfacing LSTTL/NMOS to CMOS Inputs

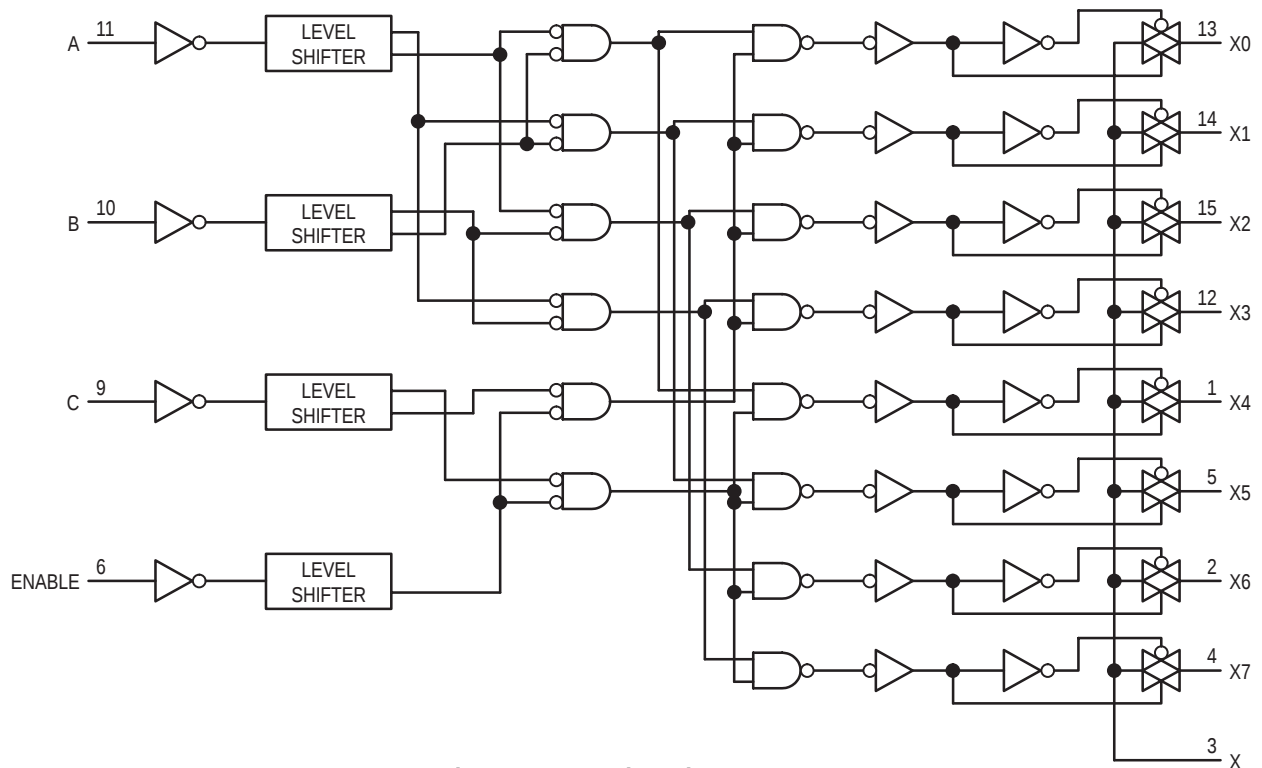


Figure 18. Function Diagram, VHC4051

MC74VHC4051, MC74VHC4052, MC74VHC4053

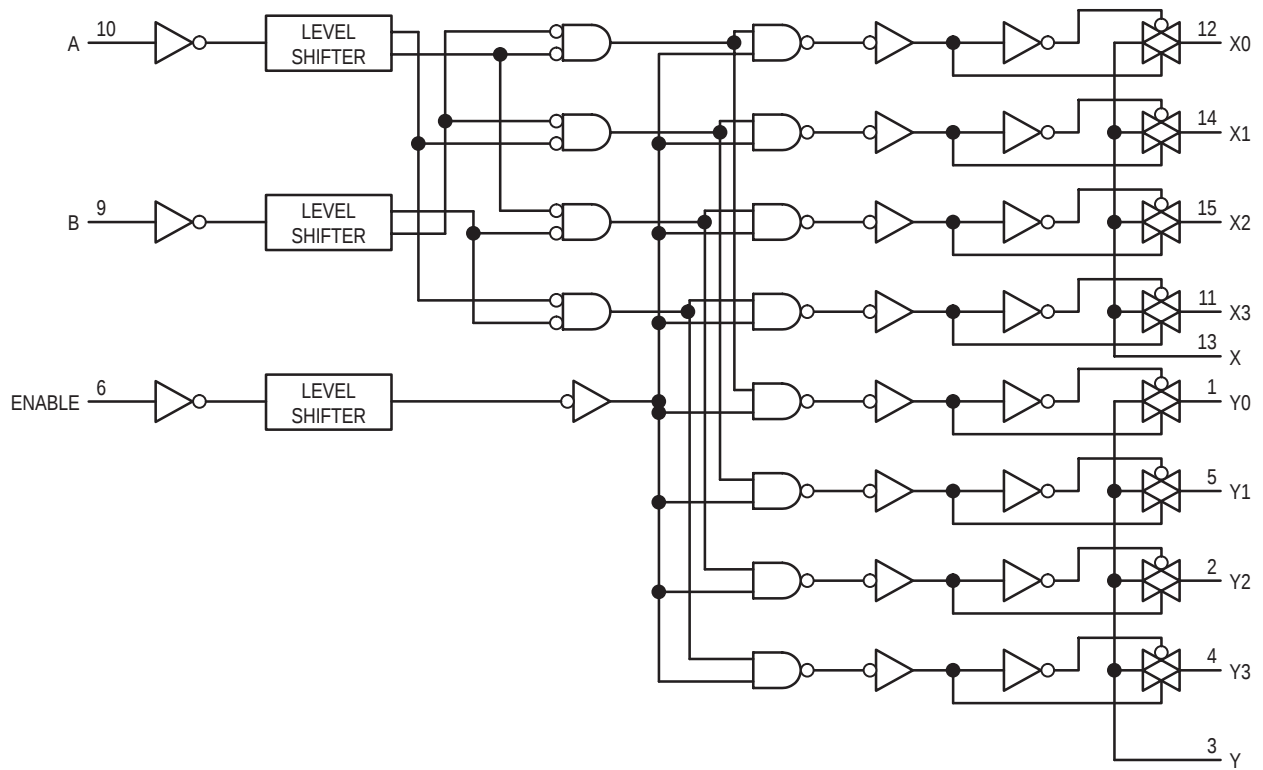


Figure 19. Function Diagram, VHC4052

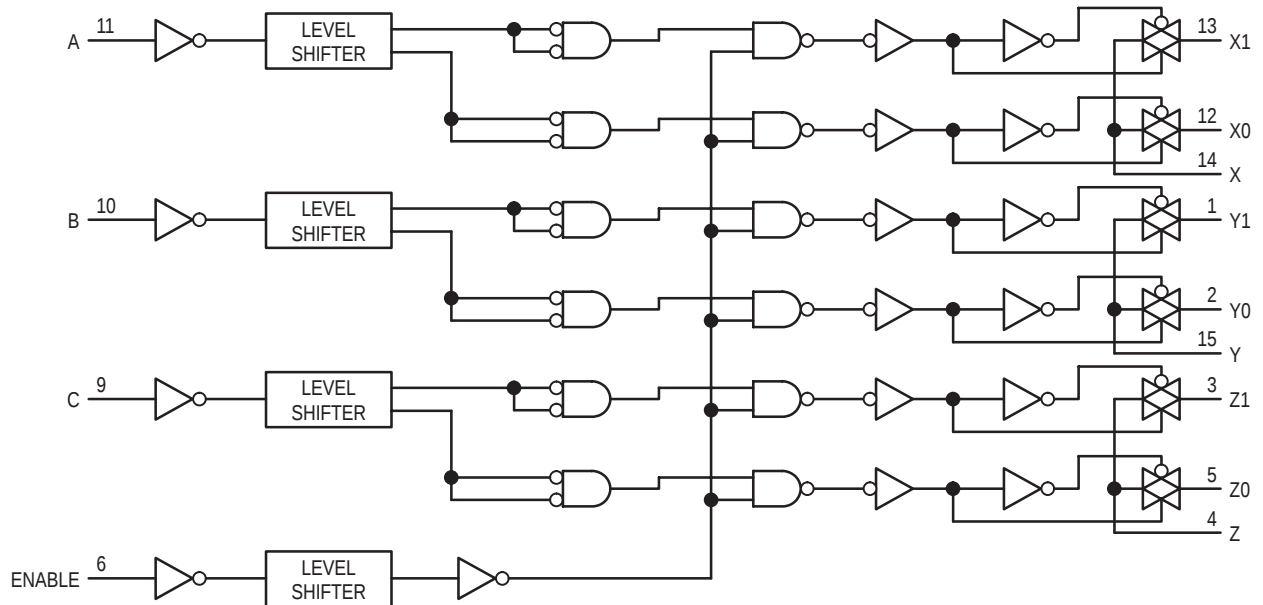


Figure 20. Function Diagram, VHC4053

MC74VHC4051, MC74VHC4052, MC74VHC4053

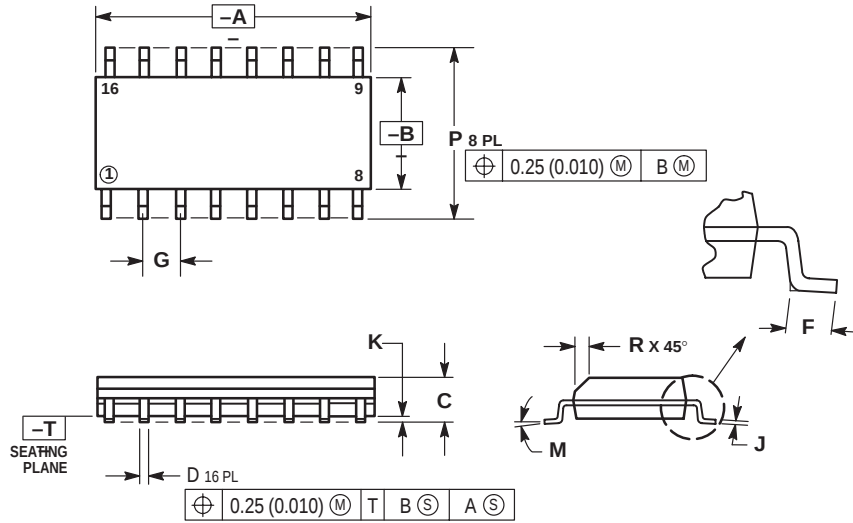
ORDERING & SHIPPING INFORMATION

Device	Package	Shipping
MC74VHC4051D	SOIC–16	48 Units / Rail
MC74VHC4051DR2	SOIC–16	2500 Units / Tape & Reel
MC74VHC4051DT	TSSOP–16	96 Units / Rail
MC74VHC4051DTR2	TSSOP–16	2500 Units / Tape & Reel
MC74VHC4052D	SOIC–16	48 Units / Rail
MC74VHC4052DR2	SOIC–16	2500 Units / Tape & Reel
MC74VHC4052DT	TSSOP–16	96 Units / Rail
MC74VHC4052DTR2	TSSOP–16	2500 Units / Tape & Reel
MC74VHC4053D	SOIC–16	48 Units / Rail
MC74VHC4053DR2	SOIC–16	2500 Units / Tape & Reel
MC74VHC4053DT	TSSOP–16	96 Units / Rail
MC74VHC4053DTR2	TSSOP–16	2500 Units / Tape & Reel

MC74VHC4051, MC74VHC4052, MC74VHC4053

PACKAGE DIMENSIONS

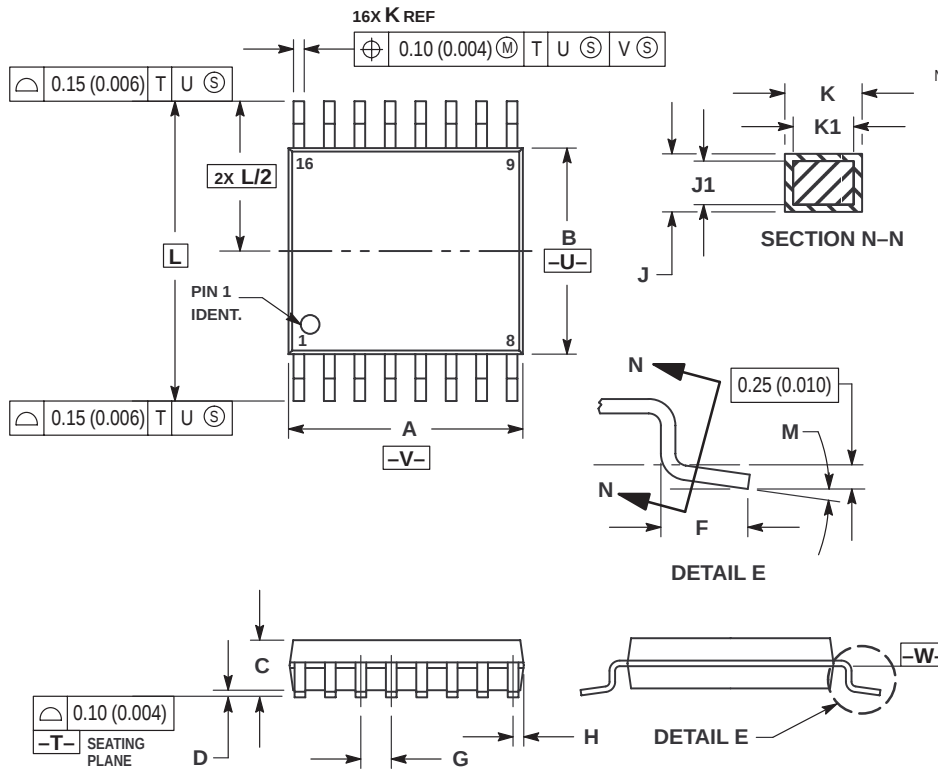
SOIC-16 D SUFFIX CASE 751B-05 ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16 DT SUFFIX CASE 948F-01 ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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