

# MC74VHCT138A

## 3-to-8 Line Decoder

The MC74VHCT138A is an advanced high speed CMOS 3-to-8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

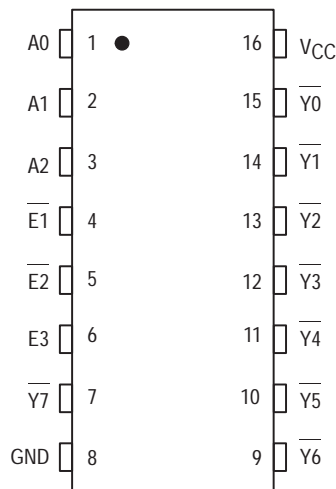
When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs (Y0 – Y7) will go Low. When enable input E3 is held Low or either E2 or E1 is held High, decoding function is inhibited and all outputs go high. E3, E2, and E1 inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because they have full 5V CMOS level output swings.

The VHCT138A input structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. The output structures also provide protection when  $V_{CC} = 0V$ . These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed:  $t_{PD} = 7.6ns$  (Typ) at  $V_{CC} = 5V$
- Low Power Dissipation:  $I_{CC} = 4\mu A$  (Max) at  $T_A = 25^\circ C$
- TTL-Compatible Inputs:  $V_{IL} = 0.8V$ ;  $V_{IH} = 2.0V$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates

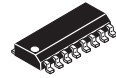
### PIN ASSIGNMENT



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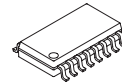
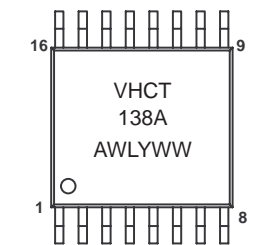
### MARKING DIAGRAMS



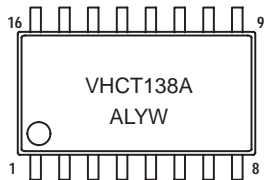
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC EIAJ-16  
M SUFFIX  
CASE 966



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

A = Assembly Location    A = Assembly Location  
WL = Wafer Lot            L = Wafer Lot  
Y = Year                    Y = Year  
WW = Work Week            W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT138AD	SOIC-16	48 Units/Rail
MC74VHCT138ADR2	SOIC-16	2500 Units/Reel
MC74VHCT138ADT	TSSOP-16	96 Units/Rail
MC74VHCT138ADTR2	TSSOP-16	2500 Units/Reel
MC74VHCT138AM	SOIC EIAJ-16	48 Units/Rail
MC74VHCT138AMEL	SOIC EIAJ-16	2000 Units/Reel

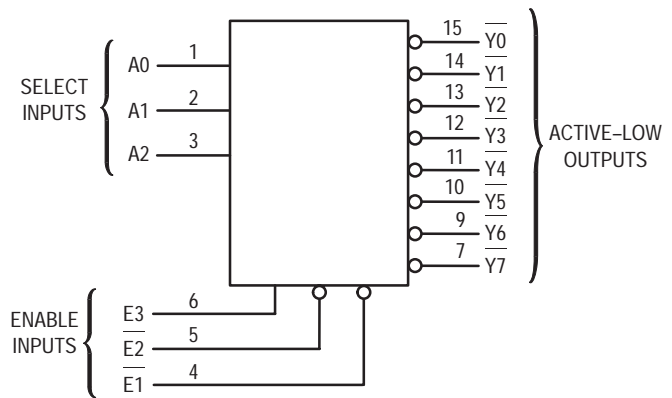
# MC74VHCT138A

**FUNCTION TABLE**

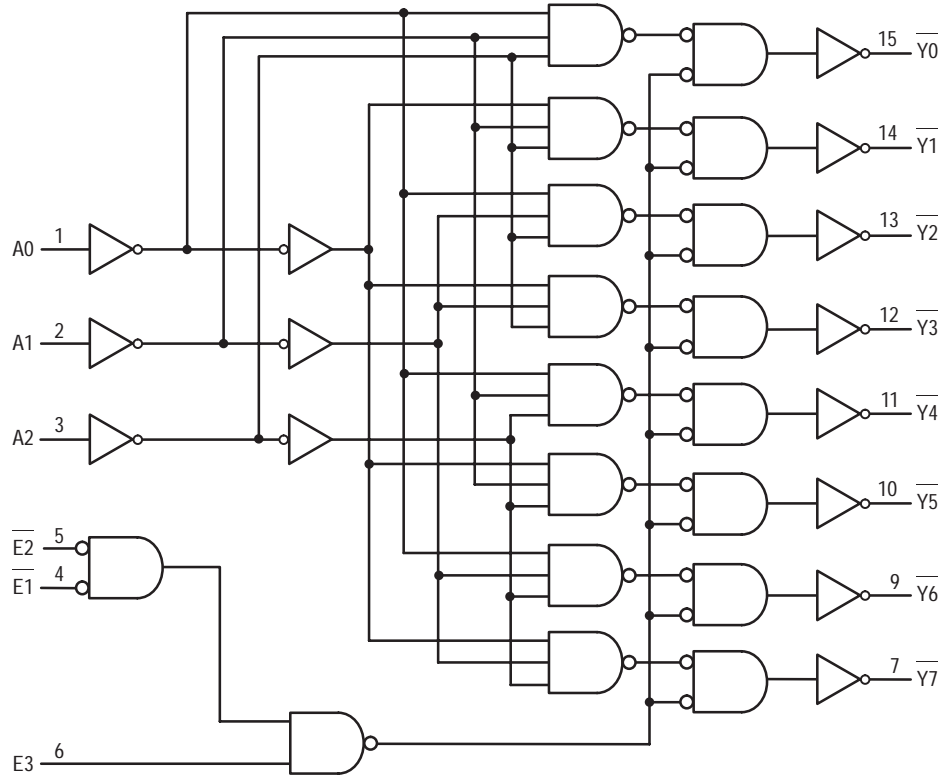
Inputs						Outputs							
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	L

H = high level (steady state); L = low level (steady state);  
X = don't care

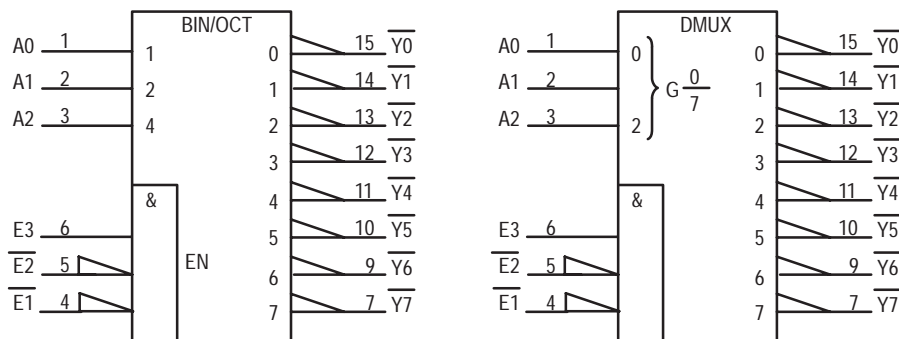
**LOGIC DIAGRAM**



**EXPANDED LOGIC DIAGRAM**



**IEC LOGIC DIAGRAM**



# MC74VHCT138A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage	- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	- 0.5 to + 7.0 - 0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	- 20	mA
I <sub>OK</sub>	Output Diode Current (V <sub>OUT</sub> < GND; V <sub>OUT</sub> > V <sub>CC</sub> )	± 20	mA
I <sub>out</sub>	DC Output Current, per Pin	± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	3.0	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage V <sub>CC</sub> = 0 High or Low State	0 0	5.5 V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	- 55	+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time V <sub>CC</sub> = 5.0V ± 0.5V	0	20	ns/V

The θ<sub>JA</sub> of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

## DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

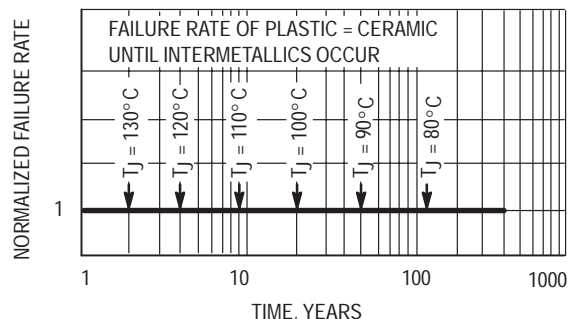


Figure 1. Failure Rate vs. Time Junction Temperature

# MC74VHCT138A

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		T <sub>A</sub> ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		3.0	1.4			1.4		1.4		V
			4.5	2.0			2.0		2.0		
			5.5	2.0			2.0		2.0		
V <sub>IL</sub>	Maximum Low-Level Input Voltage		3.0					0.53		0.53	V
			4.5					0.8		0.8	
			5.5					0.8		0.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -50 μA	3.0	2.9	3.0		2.9		2.9		V
			4.5	4.4	4.5		4.4		4.4		
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA	3.0	2.58			2.48		2.34		V
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 50 μA	3.0		0.0	0.1		0.1		0.1	V
			4.5		0.0	0.1		0.1		0.1	
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0			0.36		0.44		0.52	V
4.5			0.36		0.44		0.52		0.52		
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0		40.0	μA
I <sub>CCT</sub>	Quiescent Supply Current	V <sub>IN</sub> = 3.4 V	5.5			1.35		1.50		1.50	mA
I <sub>OPD</sub>	Output Leakage Current	V <sub>OUT</sub> = 5.5 V	0.0			0.5		5.0		5.0	μA

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> ≤ 85°C		T <sub>A</sub> ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Y	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF		9.5	14.5	1.0	16.0	1.0	16.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF		10.8	15.5	1.0	17.0	1.0	17.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input E3 to Y	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF		9.7	13.0	1.0	14.5	1.0	14.5	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF		9.5	14.0	1.0	15.5	1.0	15.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input E1 or E2 to Y	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF		10.1	14.0	1.0	15.5	1.0	15.5	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF		9.9	15.0	1.0	16.5	1.0	16.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input E1 or E2 to Y	V <sub>CC</sub> = 3.3 ± 0.3V C <sub>L</sub> = 15pF		7.0	9.6	1.0	11.0	1.0	11.0	ns
		V <sub>CC</sub> = 5.0 ± 0.5V C <sub>L</sub> = 50pF		7.5	10.6	1.0	12.0	1.0	12.0	
C <sub>IN</sub>	Maximum Input Capacitance			4	10		10		10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Note 1.)	Typical @ 25°C, V <sub>CC</sub> = 5.0V		pF
		49		

1. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

# MC74VHCT138A

## SWITCHING WAVEFORMS

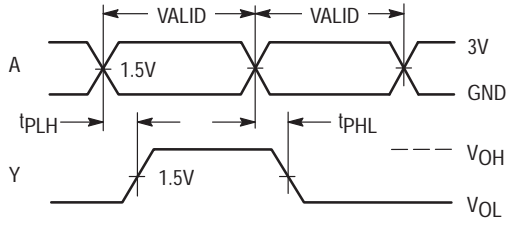


Figure 2.

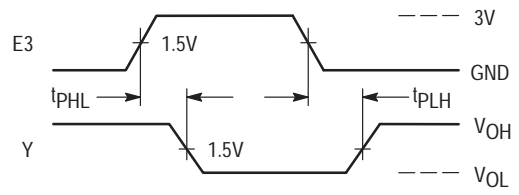


Figure 3.

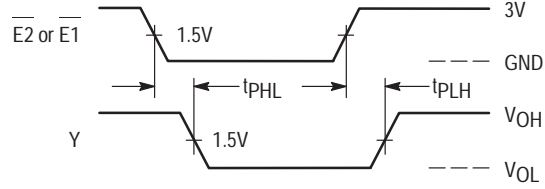
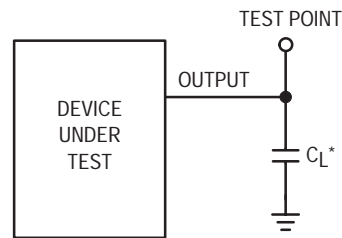


Figure 4.

## TEST CIRCUIT



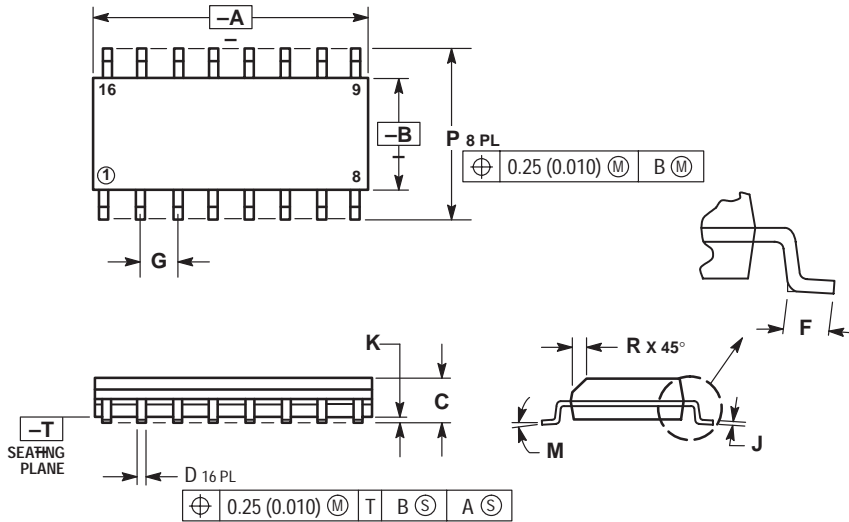
\*Includes all probe and jig capacitance

Figure 5. Test Circuit

# MC74VHCT138A

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J

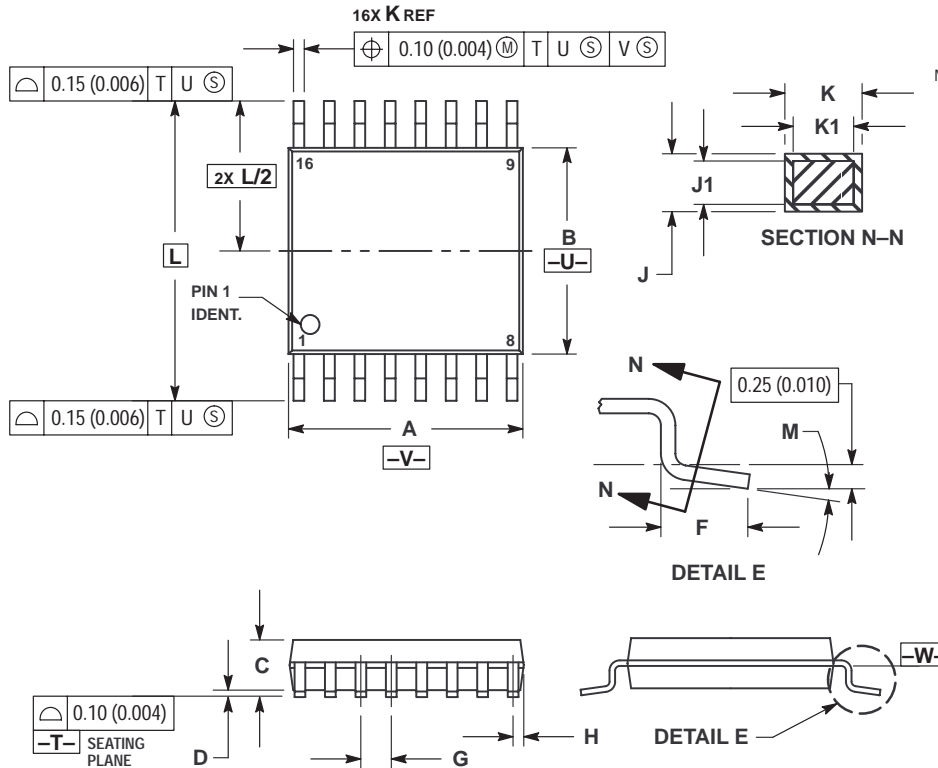


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



NOTES:

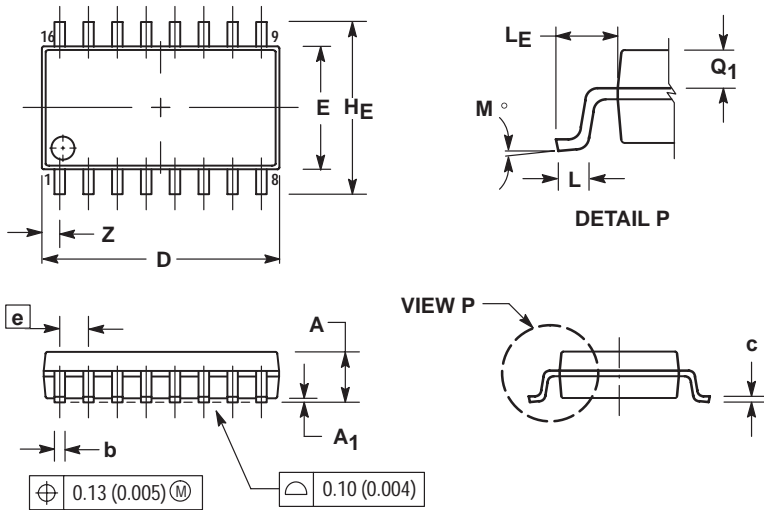
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

# MC74VHCT138A

## PACKAGE DIMENSIONS


SOIC EIAJ-16  
M SUFFIX  
CASE 966-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>F</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>F</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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