

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N-Channel Enhancement-Mode Silicon Gate

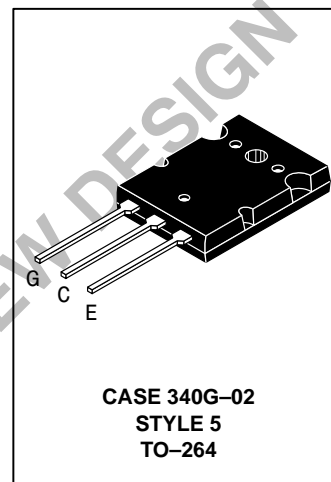
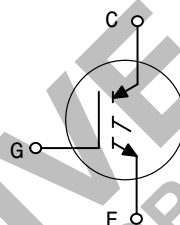
MGY25N120

Motorola Preferred Device

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

IGBT IN TO-264
25 A @ 90°C
38 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

- Industry Standard High Power TO-264 Package (TO-3PBL)
- High Speed E_{off} : 216 μ J/A typical at 125°C
- High Short Circuit Capability – 10 μ s minimum
- Robust High Voltage Termination



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	1200	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V_{CGR}	1200	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$	I_{C25}	38	Adc
— Continuous @ $T_C = 90^\circ\text{C}$	I_{C90}	25	Adc
— Repetitive Pulsed Current (1)	I_{CM}	76	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	212 1.69	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Short Circuit Withstand Time ($V_{CC} = 720 \text{ Vdc}$, $V_{GE} = 15 \text{ Vdc}$, $T_J = 125^\circ\text{C}$, $R_G = 20 \Omega$)	t_{sc}	10	μ s
Thermal Resistance — Junction to Case – IGBT	$R_{\theta JC}$	0.6	°C/W
— Junction to Ambient	$R_{\theta JA}$	35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C
Mounting Torque, 6-32 or M3 screw		10 lbf•in (1.13 N•m)	

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

MGY25N120

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-to-Emitter Breakdown Voltage (V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positive)	V _{(BR)CES}	1200 —	— 960	— —	Vdc mV/°C
Emitter-to-Collector Breakdown Voltage (V _{GE} = 0 Vdc, I _{EC} = 100 mAdc)	V _{(BR)ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current (V _{CE} = 1200 Vdc, V _{GE} = 0 Vdc) (V _{CE} = 1200 Vdc, V _{GE} = 0 Vdc, T _J = 125°C)	I _{CES}	— —	— —	100 2500	μAdc
Gate-Body Leakage Current (V _{GE} = ± 20 Vdc, V _{CE} = 0 Vdc)	I _{GES}	—	—	250	nAdc

ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage (V _{GE} = 15 Vdc, I _C = 12.5 Adc) (V _{GE} = 15 Vdc, I _C = 12.5 Adc, T _J = 125°C) (V _{GE} = 15 Vdc, I _C = 25 Adc)	V _{CE(on)}	— — —	2.37 2.15 2.98	3.24 — 4.19	Vdc
Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V _{CE} = 10 Vdc, I _C = 25 Adc)	g _{fe}	—	12	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	2795	—	pF
Output Capacitance		C _{oes}	—	181	—	
Transfer Capacitance		C _{res}	—	45	—	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{CC} = 720 Vdc, I _C = 25 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω) Energy losses include "tail"	t _{d(on)}	—	91	—	ns
Rise Time		t _r	—	124	—	
Turn-Off Delay Time		t _{d(off)}	—	196	—	
Fall Time		t _f	—	310	—	
Turn-Off Switching Loss		E _{off}	—	2.44	4.69	
Turn-On Delay Time	(V _{CC} = 720 Vdc, I _C = 25 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω, T _J = 125°C) Energy losses include "tail"	t _{d(on)}	—	88	—	ns
Rise Time		t _r	—	126	—	
Turn-Off Delay Time		t _{d(off)}	—	236	—	
Fall Time		t _f	—	640	—	
Turn-Off Switching Loss		E _{off}	—	5.40	—	
Gate Charge	(V _{CC} = 720 Vdc, I _C = 25 Adc, V _{GE} = 15 Vdc)	Q _T	—	97	—	nC
		Q ₁	—	31	—	
		Q ₂	—	40	—	

INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L _E	—	13	—	nH
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(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

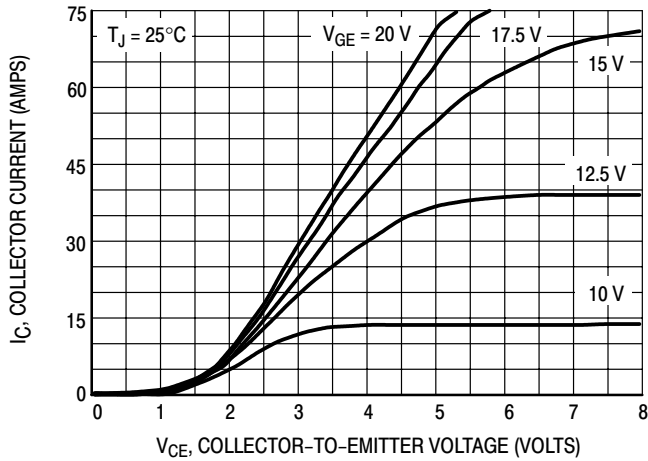


Figure 1. Output Characteristics

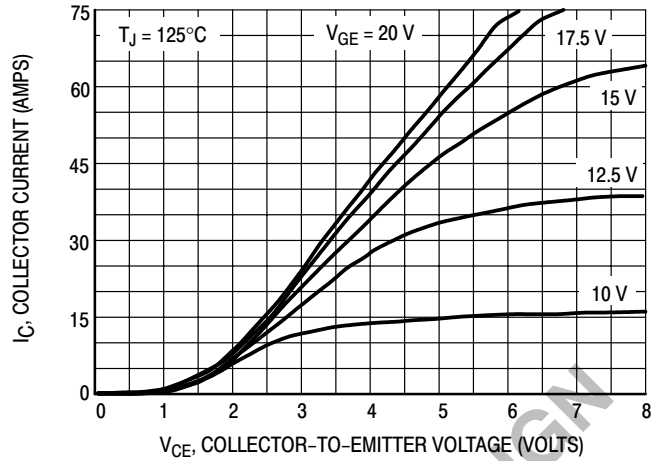


Figure 2. Output Characteristics

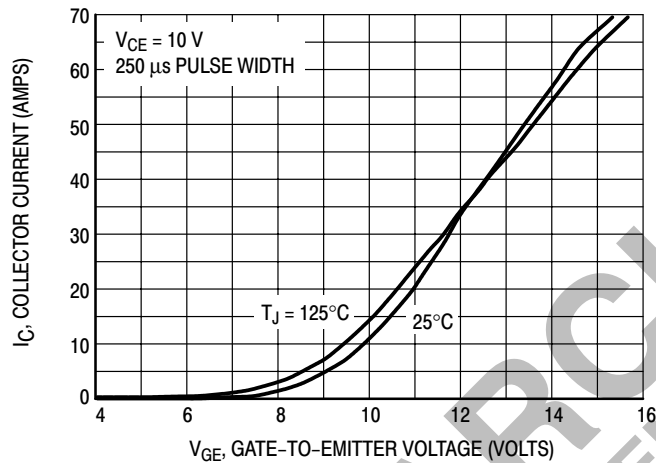


Figure 3. Transfer Characteristics

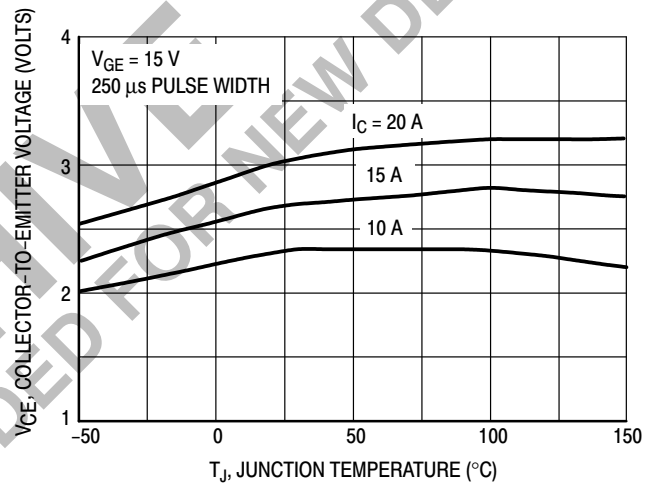


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

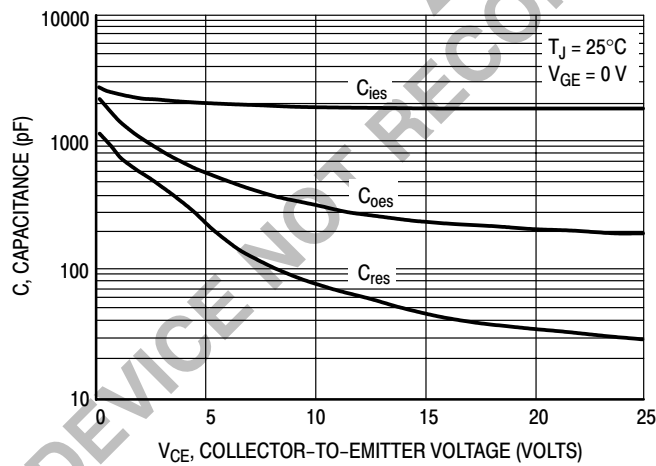


Figure 5. Capacitance Variation

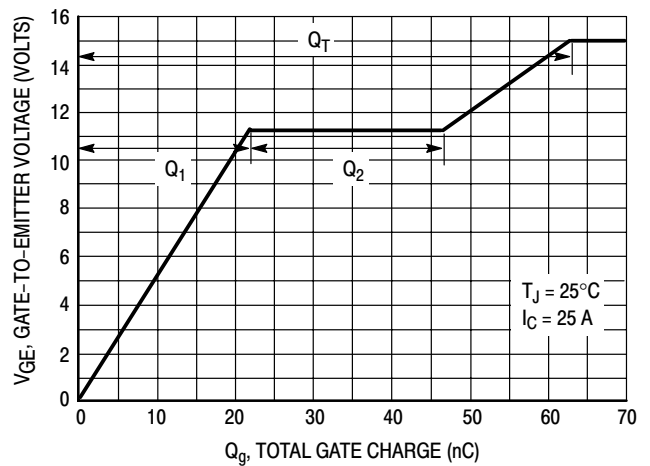


Figure 6. Gate-to-Emitter Voltage versus Total Charge

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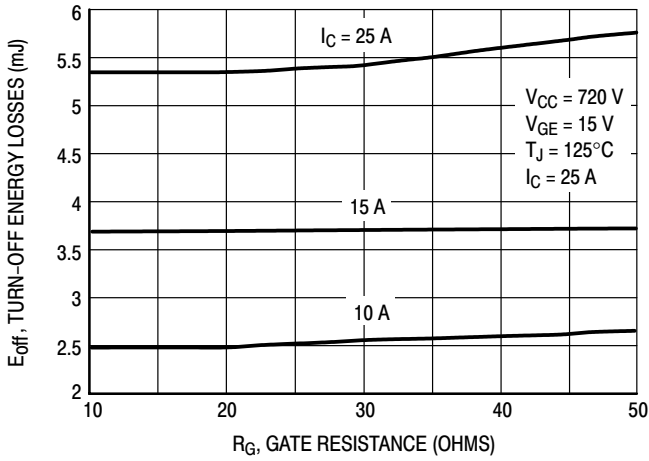


Figure 7. Turn-Off Losses versus Gate Resistance

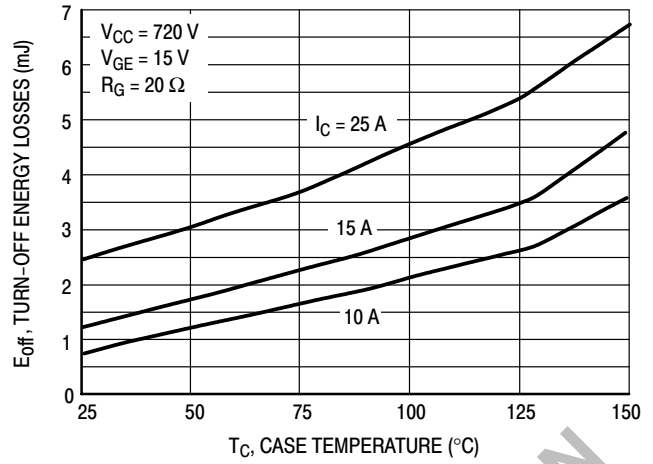


Figure 8. Turn-Off Losses versus Case Temperature

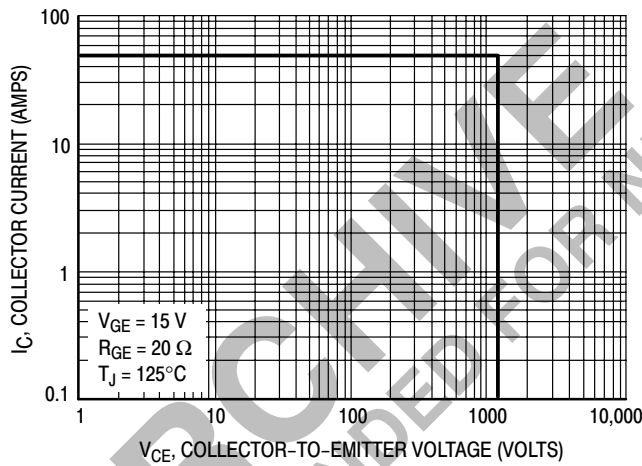


Figure 9. Reverse Biased Safe Operating Area

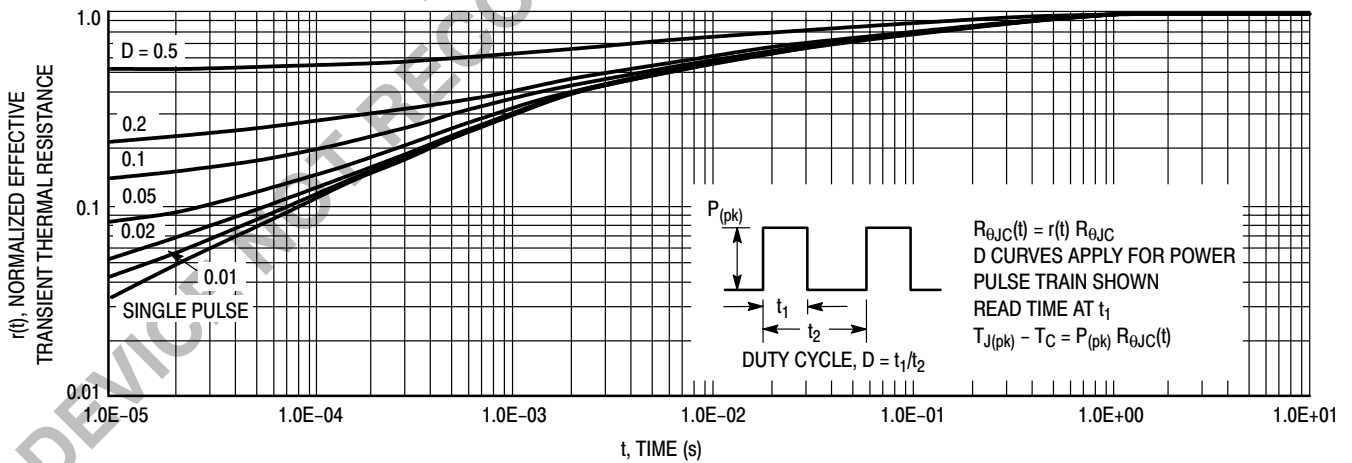
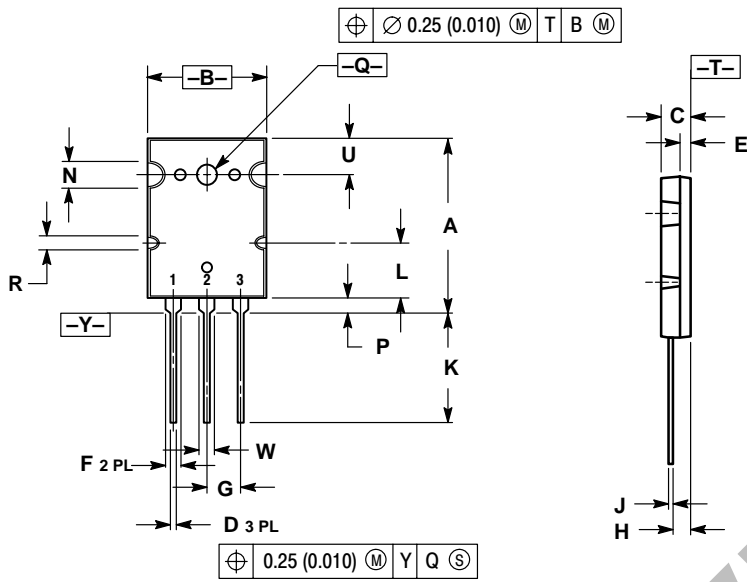


Figure 10. Thermal Response

PACKAGE DIMENSIONS




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

- STYLE 5:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER

CASE 340G-02
 TO-264
 ISSUE F

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RECOMMENDED FOR NEW DESIGN

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